TD351

Advanced IGBT/MOSFET driver

Features

- 1.7 A sink / 1.3 A source (typ) current capability
- Active Miller clamp feature
- Two-level turn-off with adjustable level and delay
- Input compatible with pulse transformer or optocoupler
- UVLO protection
- 2 kV ESD protection

SO-8

The TD351 is compatible with both pulse transformer and optocoupler signals.

Applications

- 1200 V 3-phase inverters
- Motor control systems
- UPS

Description

This device is an advanced gate driver for IGBT and power MOSFETs. Control and protection functions are included and allow the design of high reliability systems.

The innovative active Miller clamp function eliminates the need for negative gate drive in most applications and allows the use of a simple bootstrap supply for the high side driver.

The TD351 includes a two-level turn-off feature with adjustable level and delay. This function protects against excessive overvoltage at turn-off in case of overcurrent or short-circuit conditions. The same delay is applied at turn-on to prevent pulse width distortion.

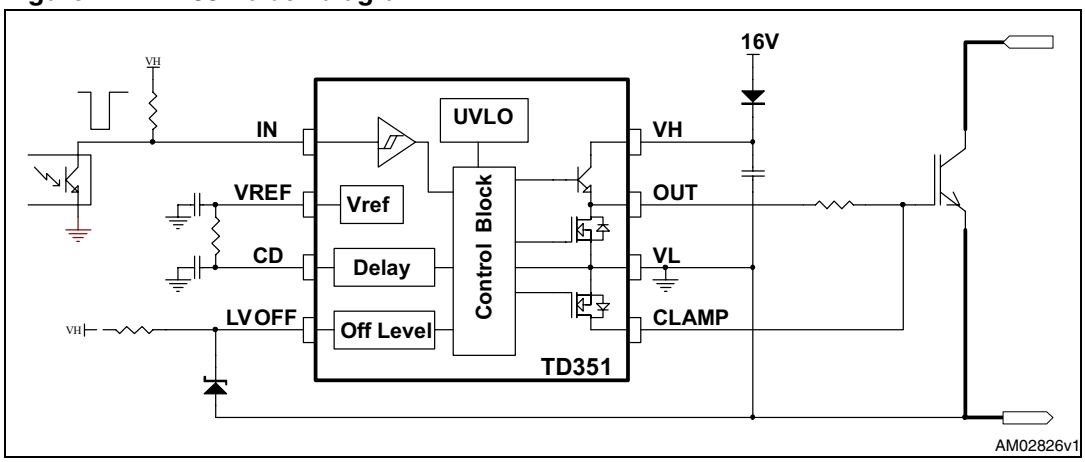
Table 1. Device summary

Order codes	Temperature range	Package	Packaging
TD351ID	-40°C, +125°C	SO-8	Tube
TD351IDT			Tape and reel

Contents

1 Block diagram

Figure 1. TD351 block diagram



2 Pin connections

Figure 2. Pin connections (top view)

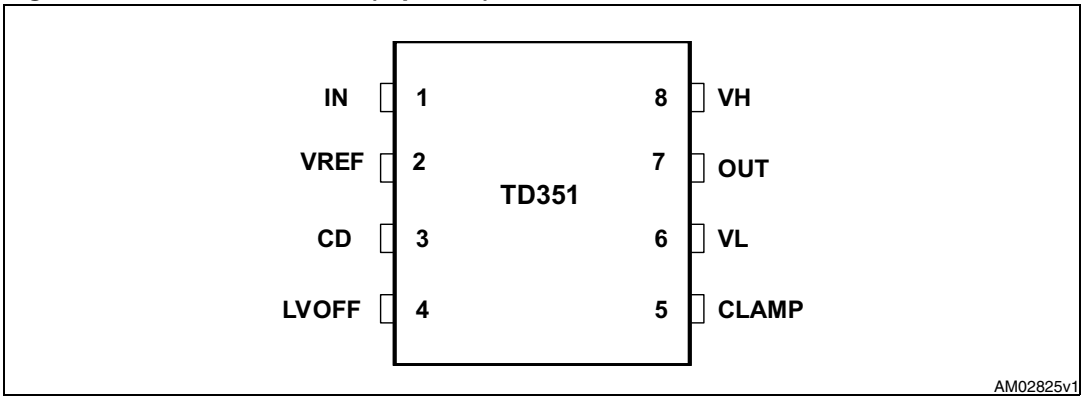


Table 2. Pin description

Pin n°	Name	Type	Function
1	IN	Analog input	Input
2	VREF	Analog output	+5 V reference voltage
3	CD	Timing capacitor	Turn on/off delay
4	LVOFF	Analog input	Turn off level
5	CLAMP	Analog output	Miller clamp
6	VL	Power supply	Signal ground
7	OUT	Analog output	Gate drive output
8	VH	Power supply	Positive supply

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VHL	Maximum supply voltage (VH - VL)	28	V
V_{out}	Voltage on OUT, CLAMP, LVOFF pins	VL-0.3 to VH+0.3	V
V_{other}	Voltage on other pins (IN, CD, VREF)	-0.3 to 7	V
P_d	Power dissipation	500	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Maximum junction temperature	150	°C
R_{thJA}	Thermal resistance junction-ambient	150	°C/W
ESD	Electrostatic discharge (HBM)	2	kV

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
VH	Positive supply voltage vs. VL	UVLO to 26	V
T_{oper}	Operating free air temperature range	-40 to 125	°C

4 Electrical characteristics

T_A = -20 to 125°C, VH = 16 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Input						
V_{ton}	IN turn-on threshold voltage		0.8	1.0		V
V_{toff}	IN turn-off threshold voltage			4.0	4.2	V
t_{onmin}	Minimum pulse width		100	135	220	ns
I_{inp}	IN input current	IN input voltage < 4.5V			1	µA
Voltage reference (1)						
V_{ref}	Voltage reference	T = 25°C	4.85	5.00	5.15	V
I_{ref}	Maximum output current		10			mA
Clamp						
V_{tclamp}	CLAMP pin voltage threshold			2.0		V
V_{CL}	Clamp low voltage	I_{csink} = 500mA			2.5	V
Delay						
V_{tdel}	Voltage threshold			2.5		V
R_{del}	Discharge resistor	I=1mA			500	
Off Level						
I_{blvoff}	LVOFF peak input current (sink)	LVOFF = 12V		90	200	µA
V_{iolv}	Offset voltage	LVOFF = 12V	-0.3	-0.15	0	V
Output						
I_{sink}	Output sink current	V_{out} = 6V	1000	1700		mA
I_{src}	Output source current	V_{out} = VH-6V	750	1300		mA
V_{OL1}	Output low voltage 1	I_{osink} = 20mA			0.35	V
V_{OL2}	Output low voltage 2	I_{osink} = 500mA			2.5	V
V_{OH1}	Output high voltage 1	$I_{osource}$ = 20mA	VH-2.5			V
V_{OH2}	Output high voltage 2	$I_{osource}$ = 500mA	VH-4.0			V
t_r	Rise time	C_L = 1nF, 10% to 90%			100	ns
t_f	Fall time (2)	C_L = 1nF, 90% to 10%			100	ns
t_{don}	Turn on propagation delay	10% OUT change: R_d = 4.7kΩ, no C_d R_d = 10kΩ, C_d = 220 pF	 1.8	 2.0	 600 2.2	 ns µs
t_{doff}	Turn off propagation delay (2)	10% OUT change			550	ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Δt_w	Input to output pulse distortion	10% OUT change, $\Delta t_w = T_{wout} - T_{win}$		50	100	ns
Under voltage lockout (UVLO)						
UVLOH	UVLO top threshold		10	11	12	V
UVLOL	UVLO bottom threshold		9	10	11	V
V_{hyst}	UVLO hysteresis	UVLOH-UVLOL	0.5	1		V
Supply current						
I_{in}	Quiescent current	OUT = 0V; no load			2.5	mA

1. Recommended capacitor range on VREF pin is 10 nF to 100 nF
2. 2 step turn-off disabled.

5 Functional description

5.1 Input stage

The TD351 input is compatible with optocouplers or pulse transformers. The input is triggered by the signal edge and allows the use of low-sized, low-cost pulse transformers. Input is active low and output is driven high when input is driven low. The IN input is internally clamped at about 5 V to 7 V. When using an open collector optocoupler, the resistive pull-up resistor can be connected to either VREF or VH. Recommended pull-up resistor value with VH = 16 V is from 4.7 kΩ to 22 kΩ When driven by a pulse transformer, the input positive and negative pulse widths at the V_{ton} and V_{toff} threshold voltages must be larger than the minimum pulse width t_{onmin} (see *Figure 6*). This feature acts as a filter against invalid input pulses smaller than t_{onmin}.

5.2 Voltage reference

A voltage reference is used to create accurate timing for the turn-on delay with external resistor and capacitor. The same circuitry is also used for the two-level turn-off delay. A decoupling capacitor (10 nF to 100 nF) on the VREF pin is required to ensure good noise rejection.

5.3 Active Miller clamp

The TD351 offers an alternative solution to the problem of Miller current in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, the TD351 uses a dedicated CLAMP pin to control the Miller current. When the IGBT is off, a low impedance path is established between the IGBT gate and emitter to carry the Miller current, and the voltage spike on the IGBT gate is greatly reduced. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2 V (relative to VL). The clamp voltage is VL+4V max for a Miller current up to 500 mA. The clamp is disabled when the IN input is triggered again.

The CLAMP function does not affect the turn-off characteristic, but only keeps the gate at low level throughout the OFF-time. The main benefit is that negative voltage can be avoided in many cases, allowing a bootstrap technique for the high side driver supply.

5.4 Two-level turn-off

During turn-off, the gate voltage can be reduced to a programmable level in order to reduce the IGBT current (in the event of overcurrent). This action prevents both dangerous overvoltages across the IGBT and RBSOA problems, especially at short-circuit turn-off.

The turn-off (T_a) delay is programmable through external resistor R_d and capacitor C_d for accurate timing.

T_a is approximately given by (see *Figure 5*):

$$T_a(\mu s) = 0.7 \cdot R_d(k\Omega) \cdot C_d(nF)$$

The turn-off delay (T_a) is also used to delay the input signal to prevent distortion of input pulse width.

The two-level turn-off sequence can be disabled by connecting the LVOFF pin to VH and connecting the CD pin to VREF with a 4.7 kΩ resistor.

5.5 Minimum input ON-time

Input signals with ON-time smaller than T_a are ignored.

ON-time signals larger than $T_a+2 \cdot R_{del} \cdot C_d$ (R_{del} is the internal discharge switch resistance, C_d is the external timing capacitor) are transmitted to the output stage after the T_a delay, with minimum width distortion ($\Delta T_w = T_{wout} - T_{win}$).

For ON-time input signals close to T_a (between T_a and $T_a+2 \cdot R_{del} \cdot C_d$), the two-level duration is slightly reduced and the total output width can be smaller than the input width (see *Figure 7*).

5.6 Output stage

The output stage is able to sink/source 1.7 A/1.3 A (typical) at 25 °C and 1.0 A/0.75 A min. over the full temperature range. This current capability is specified near the usual IGBT Miller plateau.

5.7 Undervoltage protection

Undervoltage detection protects the application in the event of a low VH supply voltage (during startup or a fault situation). During undervoltage, the OUT pin is driven low (active pull-down for VH>2V, and passive pull-down for VH<2V).

Figure 3. Undervoltage protection

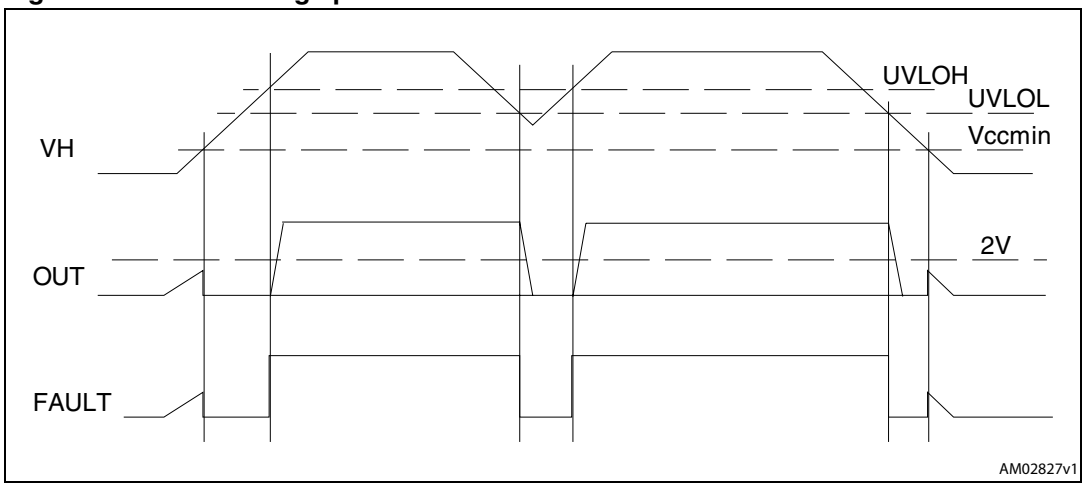
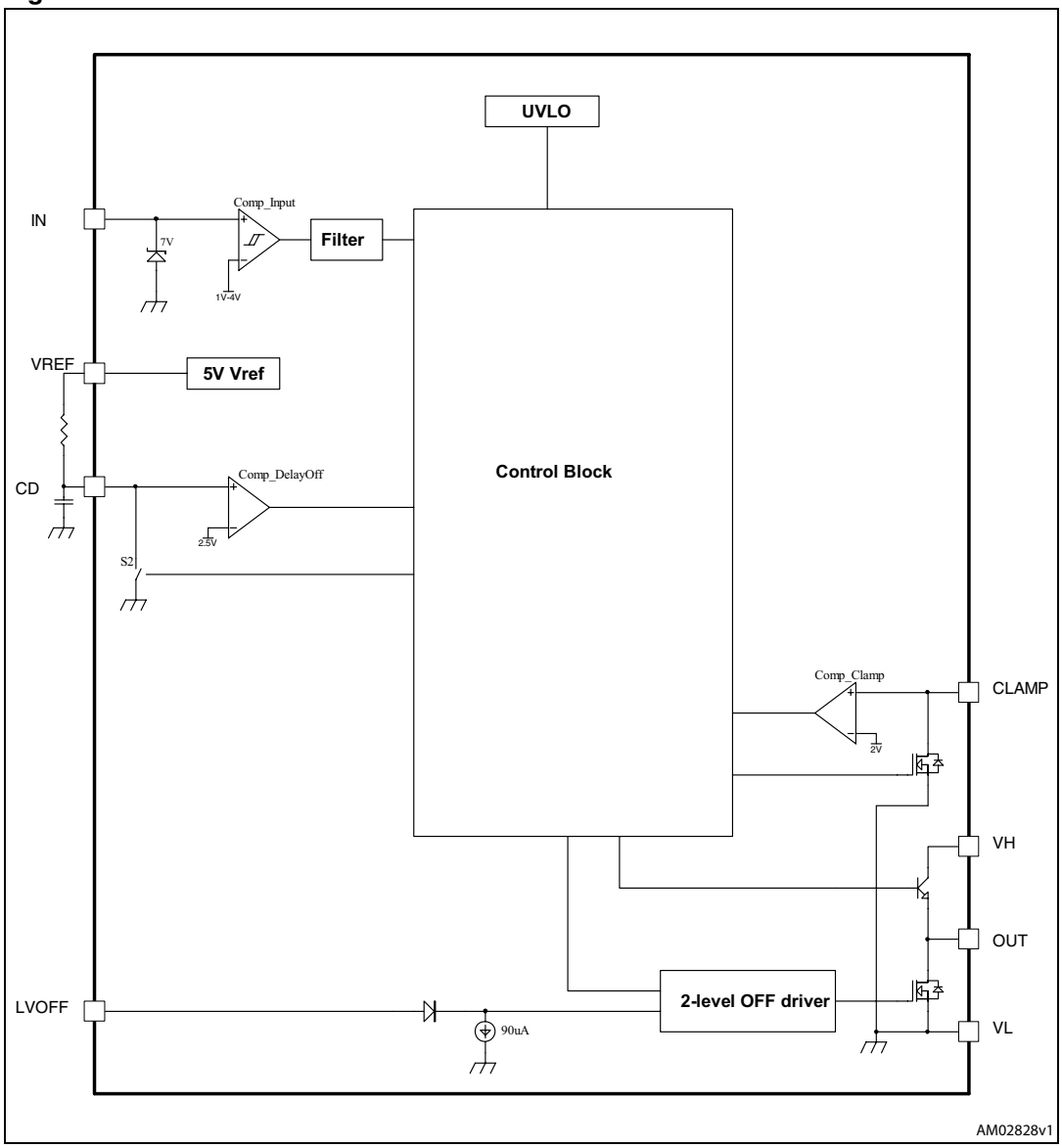


Figure 4. Detailed internal schematic



6 Timing diagrams

Figure 5. General turn-on and two-level turn-off sequence

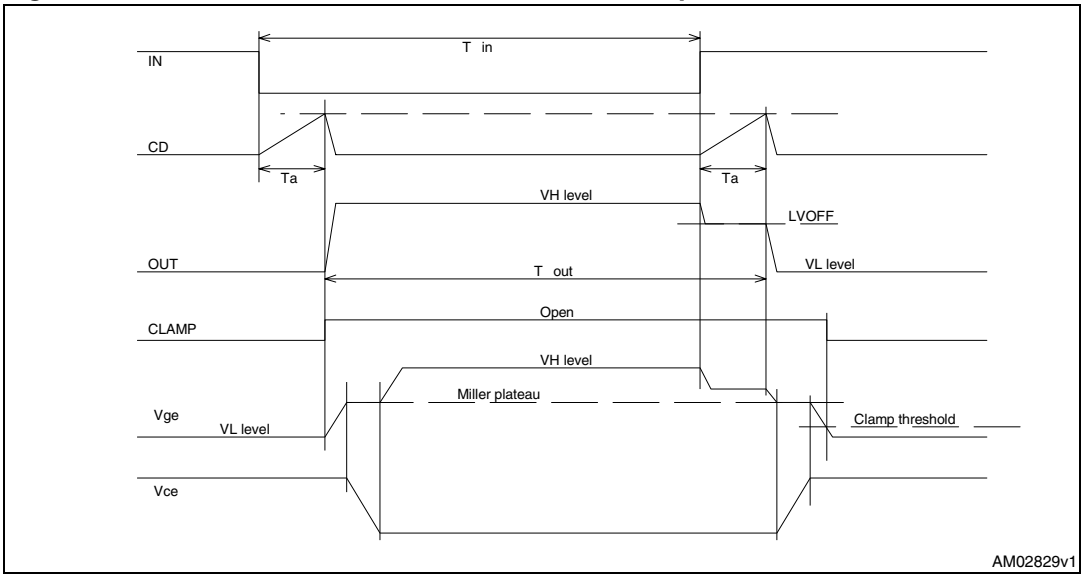


Figure 6. Input and output waveform dynamic parameters

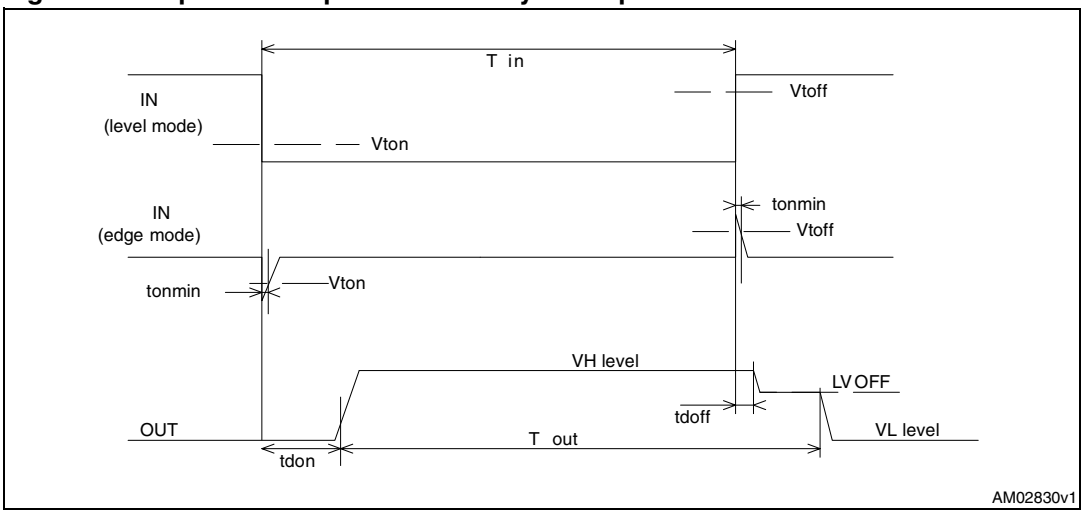
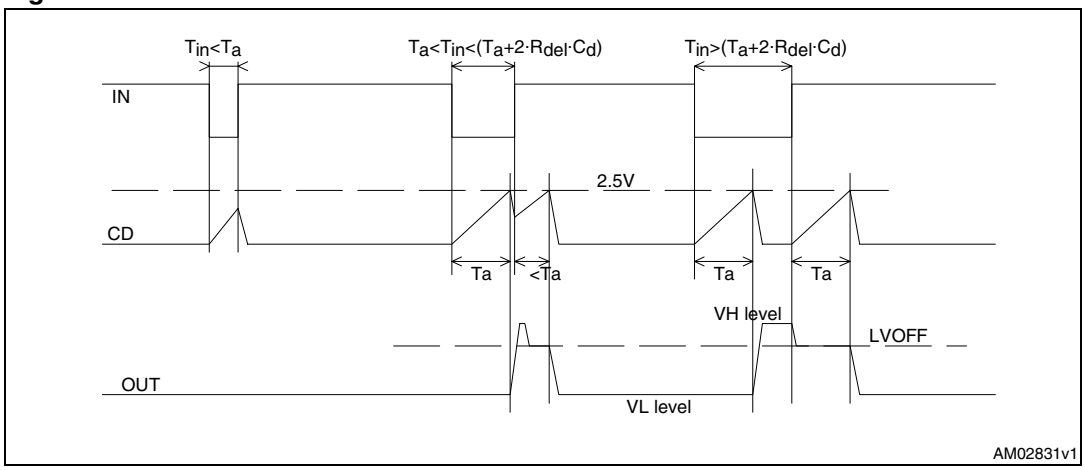


Figure 7. Minimum ON-time



7 Typical performance curves

Figure 8. Quiescent current vs temperature

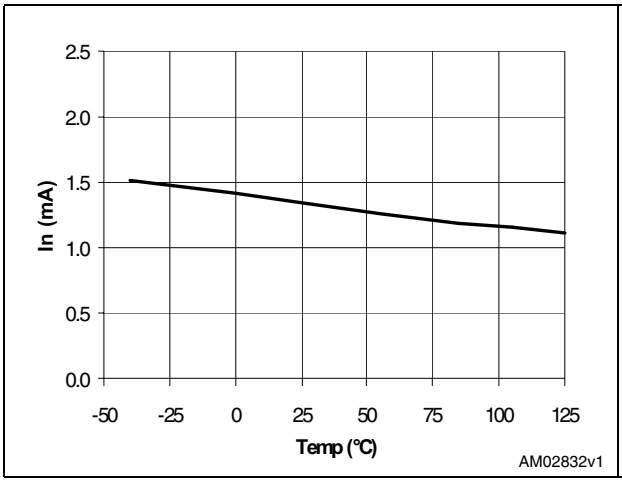


Figure 9. Rdel resistance vs temperature

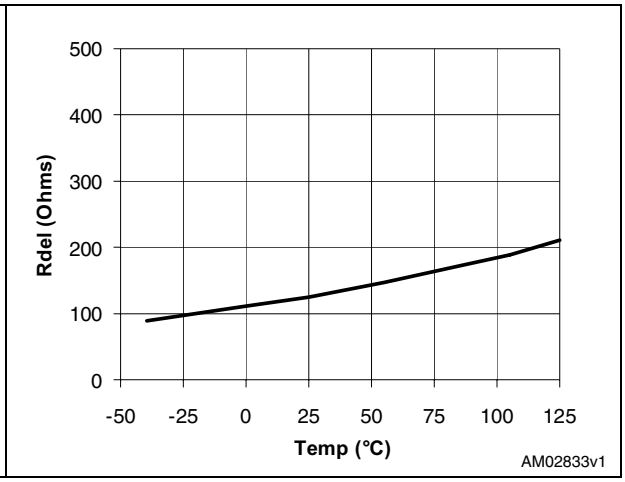


Figure 10. Low level output voltage vs temp.

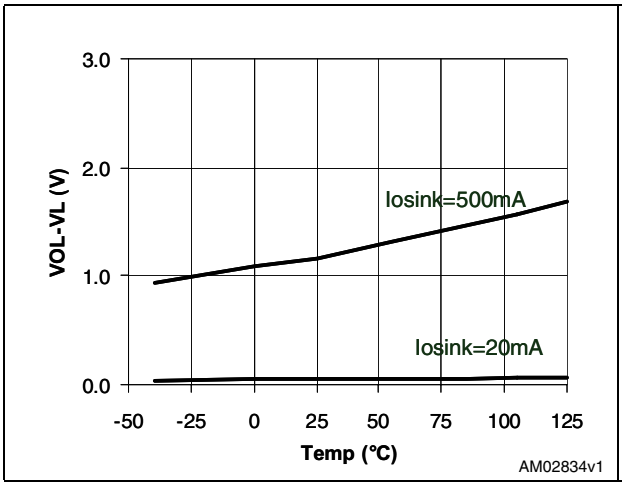


Figure 11. High level output voltage vs temp.

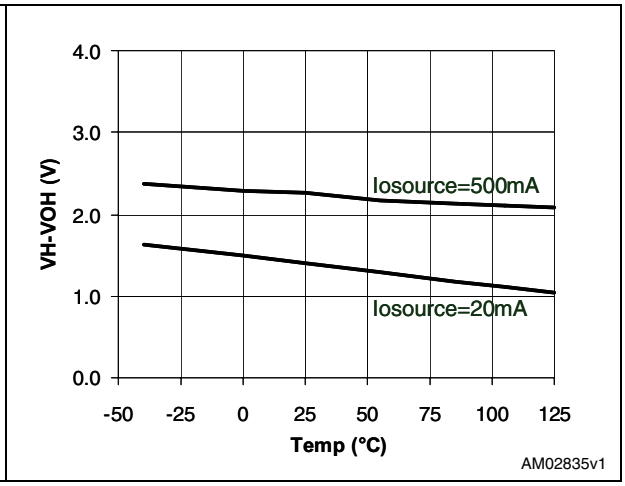


Figure 12. Sink current vs temperature

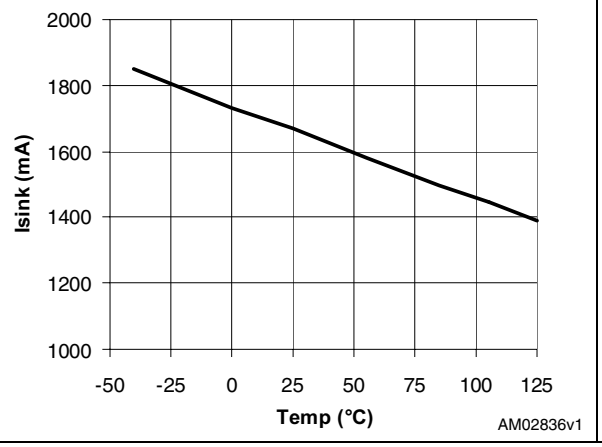
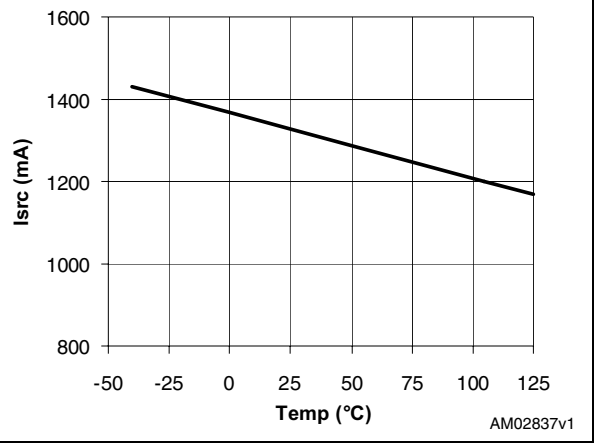


Figure 13. Source current vs temperature



8 Application diagrams

Figure 14. Single supply IGBT drive with active Miller clamp and opto input signal

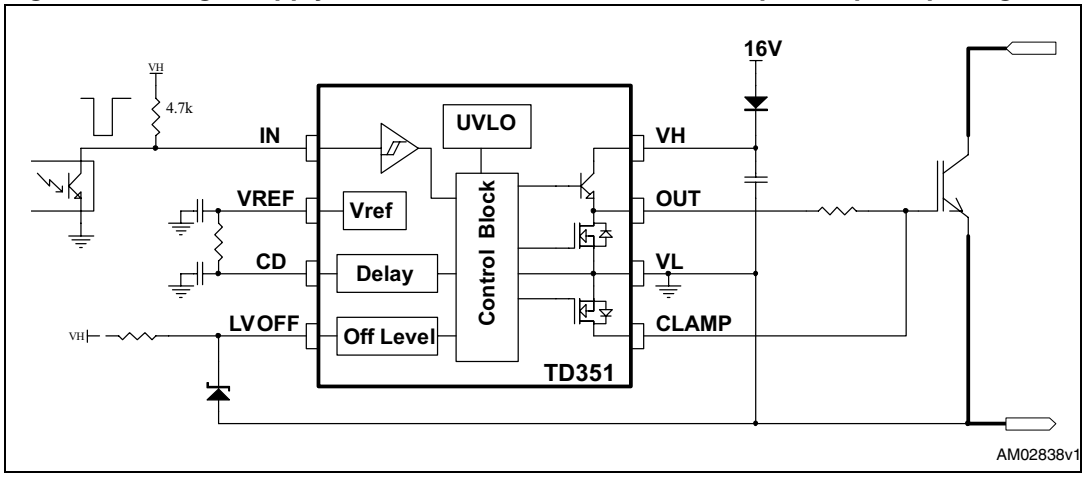


Figure 15. Single supply IGBT drive with active Miller clamp and pulse transformer input signal

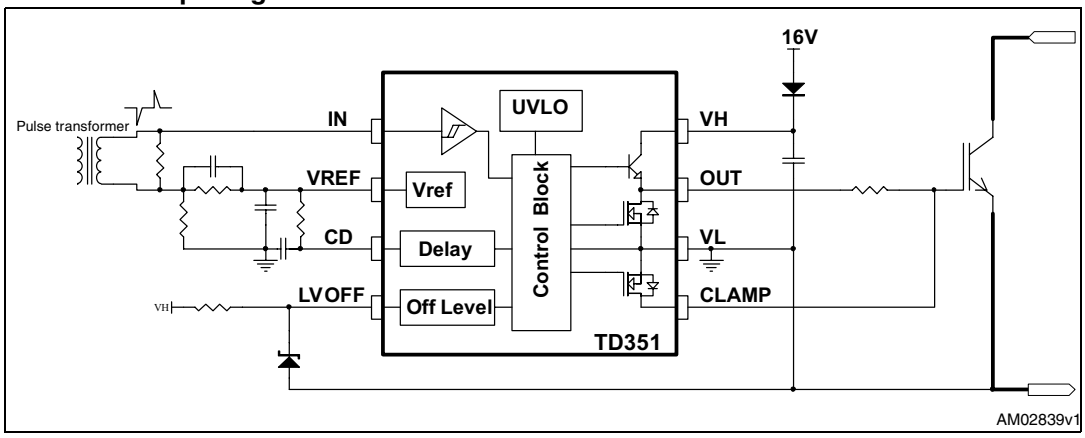
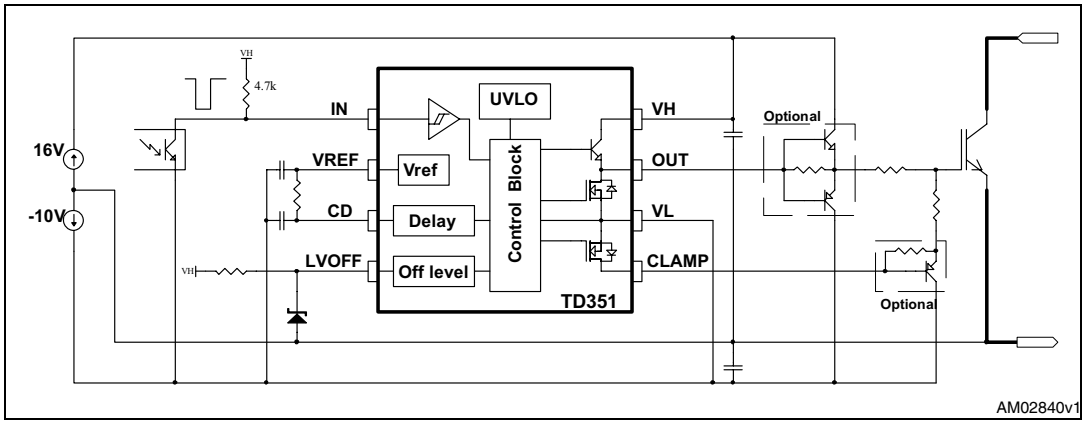


Figure 16. Large IGBT drive with negative voltage gate drive and optional current buffers



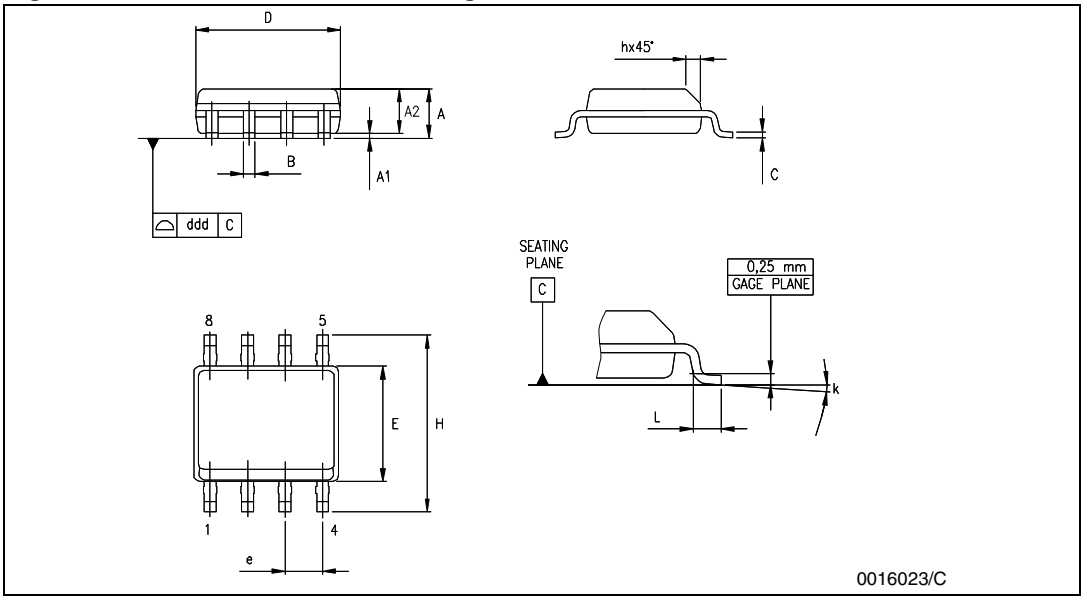
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 6. SO-8 mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	(max.) 8					
ddd			0.1			0.04

Figure 17. SO-8 mechanical drawing



10 Revision history

Table 7. Document revision history

Date	Revision	Changes
01-Nov-2004	1	Initial release
16-Jun-2011	2	Removed order code TD351IN

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