

CD40107B Types

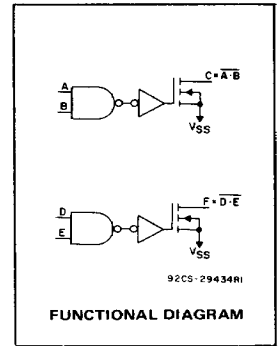
CMOS Dual 2-Input  
NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

The RCA-CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at  $V_{DD} = 10\text{ V}$ ,  $V_{DS} = 1\text{ V}$ ). The CD40107B is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package (E suffix), 14-lead hermetic frit-seal ceramic package (F suffix), and in chip form (H suffix).

Features:

- 32 times standard B-Series output current drive sinking capability — 136 mA typ. @  $V_{DD} = 10\text{ V}$ ,  $V_{DS} = 1\text{ V}$
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1\text{ }\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ\text{C}$
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range,  $R_L$  to  $V_{DD} = 10\text{ k}\Omega$ :
  - 1 V at  $V_{DD} = 5\text{ V}$
  - 2 V at  $V_{DD} = 10\text{ V}$
  - 2.5 V at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications

- Driving relays, lamps, LEDs
- Line driver
- Level shifter (up or down)

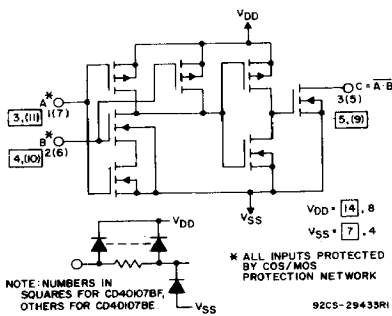


Fig. 1 — Schematic diagram of CD40107B (one of 2 gates)

TRUTH TABLE

| A | B | C  |
|---|---|----|
| 0 | 0 | 1* |
| 0 | 1 | 1* |
| 1 | 0 | 1* |
| 1 | 1 | 0  |

\*Requires external pull-up resistor ( $R_L$ ) to  $V_{DD}$ .

#Without pull-up resistor (3-state).

MAXIMUM RATINGS, Absolute-Maximum Values:

|                                                                               |                                                           |
|-------------------------------------------------------------------------------|-----------------------------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )                                         | -0.5 to +20 V                                             |
| (Voltages referenced to $V_{SS}$ Terminal)                                    |                                                           |
| INPUT VOLTAGE RANGE, ALL INPUTS                                               | -0.5 to $V_{DD} + 0.5\text{ V}$                           |
| DC INPUT CURRENT, ANY ONE INPUT                                               | $\pm 10\text{ mA}$                                        |
| POWER DISSIPATION PER PACKAGE ( $P_D$ )                                       | 500 mW                                                    |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR:                                     |                                                           |
| For $T_A = -40$ to $+62.5^\circ\text{C}$ (PACKAGE TYPE E)                     | 250 mW                                                    |
| For $T_A = +62.5$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)                     | Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 156 mW |
| For $T_A = -55$ to $+87.5^\circ\text{C}$ (PACKAGE TYPES F, H)                 | 250 mW                                                    |
| For $T_A = +87.5$ to $+125^\circ\text{C}$ (PACKAGE TYPES F, H)                | Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 94 mW  |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ):                                        |                                                           |
| PACKAGE TYPES F, H                                                            | -55 to $+125^\circ\text{C}$                               |
| PACKAGE TYPE E                                                                | -40 to $+85^\circ\text{C}$                                |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                                       | -65 to $+150^\circ\text{C}$                               |
| LEAD TEMPERATURE (DURING SOLDERING):                                          |                                                           |
| At distance $1/16 \pm 1/32$ inch (1.59 $\pm$ 0.79 mm) from case for 10 s max. | $+265^\circ\text{C}$                                      |

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC                                                       | LIMITS |      | UNITS |
|----------------------------------------------------------------------|--------|------|-------|
|                                                                      | MIN.   | MAX. |       |
| Supply-Voltage Range (For $T_A =$<br>Full Package-Temperature Range) | 3      | 18   | V     |

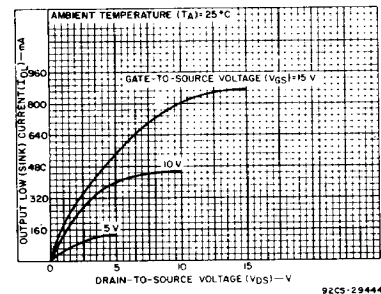


Fig. 2 — Typical output low (sink) current characteristics.

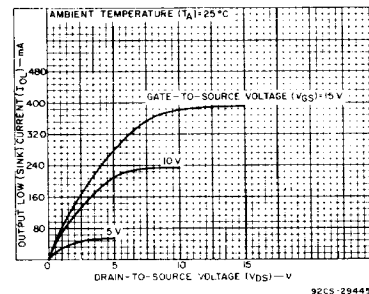


Fig. 3 — Minimum output low (sink) current characteristics.

# CD40107B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , Input  $t_r, t_f = 20\text{ ns}$

| CHARACTERISTIC                               | TEST CONDITIONS       | LIMITS       |      |      | UNITS |
|----------------------------------------------|-----------------------|--------------|------|------|-------|
|                                              |                       | VDD<br>Volts | Typ. | Max. |       |
| Propagation Delay:<br>High-to-Low, $t_{PHL}$ | $R_L^* = 120\ \Omega$ | 5            | 100  | 200  | ns    |
|                                              |                       | 10           | 45   | 90   |       |
|                                              |                       | 15           | 30   | 60   |       |
| Low-to-High, $t_{PLH}$                       | $R_L^* = 120\ \Omega$ | 5            | 100  | 200  | ns    |
|                                              |                       | 10           | 60   | 120  |       |
|                                              |                       | 15           | 50   | 100  |       |
| Transition Time:<br>High-to-Low, $t_{THL}$   | $R_L^* = 120\ \Omega$ | 5            | 50   | 100  | ns    |
|                                              |                       | 10           | 20   | 40   |       |
|                                              |                       | 15           | 10   | 20   |       |
| Low-to-High, $t_{TLH}$                       | $R_L^* = 120\ \Omega$ | 5            | 50   | 100  | ns    |
|                                              |                       | 10           | 35   | 70   |       |
|                                              |                       | 15           | 25   | 50   |       |
| Average Input Capacitance, $C_{IN}$          | Any Input             |              | 5    | 7.5  | pF    |
| Average Output Capacitance, $C_{OUT}$        | Any Output            |              | 30   | —    | pF    |

\*  $R_L$  is external pull-up resistor to  $V_{DD}$ .

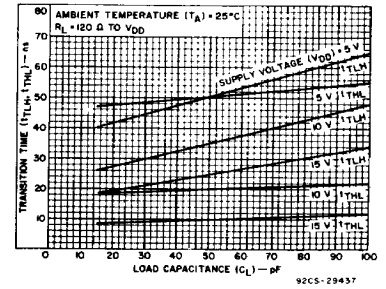


Fig. 4 — Typical transition time as a function of load capacitance.

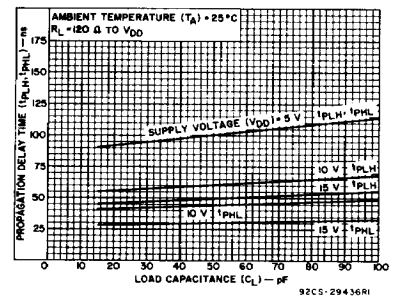


Fig. 5 — Typical propagation delay time as a function of load capacitance.

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                        | CONDITIONS                 |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C)                                                        |      |     |      |     |                   |      | UNITS |
|------------------------------------------------------------|----------------------------|------------------------|------------------------|----------------------------------------------------------------------------------------------|------|-----|------|-----|-------------------|------|-------|
|                                                            | V <sub>O</sub><br>(V)      | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | Values at −55, +25, +125 Apply to F,H Packages<br>Values at −40, +25, +85 Apply to E Package |      |     |      |     |                   |      |       |
|                                                            |                            |                        |                        | −55                                                                                          | −40  | +85 | +125 | +25 |                   |      |       |
| Quiescent Device<br>Current<br>I <sub>DD</sub> Max.        | —                          | 0,5                    | 5                      | 1                                                                                            | 1    | 30  | 30   | —   | 0.02              | 1    | μA    |
|                                                            | —                          | 0,10                   | 10                     | 2                                                                                            | 2    | 60  | 60   | —   | 0.02              | 2    |       |
|                                                            | —                          | 0,15                   | 15                     | 4                                                                                            | 4    | 120 | 120  | —   | 0.02              | 4    |       |
|                                                            | —                          | 0,20                   | 20                     | 20                                                                                           | 20   | 600 | 600  | —   | 0.04              | 20   |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.       | 0.4                        | 0,5                    | 5                      | 21                                                                                           | 20   | 14  | 12   | 16  | 32                | —    | mA    |
|                                                            | 1                          | 0,5                    | 5                      | 44                                                                                           | 42   | 30  | 25   | 34  | 68                | —    |       |
|                                                            | 0,5                        | 0,10                   | 10                     | 49                                                                                           | 46   | 32  | 28   | 37  | 74                | —    |       |
|                                                            | 1                          | 0,10                   | 10                     | 89                                                                                           | 85   | 60  | 51   | 68  | 136               | —    |       |
| 0,5                                                        | 0,15                       | 15                     | 66                     | 63                                                                                           | 44   | 38  | 50   | 100 | —                 |      |       |
| Output High<br>(Source)<br>Current<br>I <sub>OH</sub> Min. | No Internal Pull-Up Device |                        |                        |                                                                                              |      |     |      |     |                   |      |       |
| Input Low<br>Voltage<br>V <sub>IL</sub> Max.*              | 4.5                        | —                      | 5                      | 1.5                                                                                          |      |     | —    |     | —                 | 1.5  | V     |
|                                                            | 9                          | —                      | 10                     | 3                                                                                            |      |     | —    |     | —                 | 3    |       |
|                                                            | 13.5                       | —                      | 15                     | 4                                                                                            |      |     | —    |     | —                 | 4    |       |
| Input High<br>Voltage<br>V <sub>IH</sub> Min.*             | 0.5,4.5                    | —                      | 5                      | 3.5                                                                                          |      |     | 3.5  |     | —                 | —    |       |
|                                                            | 1,9                        | —                      | 10                     | 7                                                                                            |      |     | 7    |     | —                 | —    |       |
|                                                            | 1.5,13.5                   | —                      | 15                     | 11                                                                                           |      |     | 11   |     | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                      | —                          | 0,18                   | 18                     | ±0.1                                                                                         | ±0.1 | ±1  | ±1   | —   | ±10 <sup>−5</sup> | ±0.1 | μA    |
| Output Leakage<br>Current<br>I <sub>OZ</sub> Max.          | 18                         | 0,18                   | 18                     | 2                                                                                            | 2    | 20  | 20   | —   | 10 <sup>−4</sup>  | 2    | μA    |

\* Measured with external pull-up resistor,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}$ .

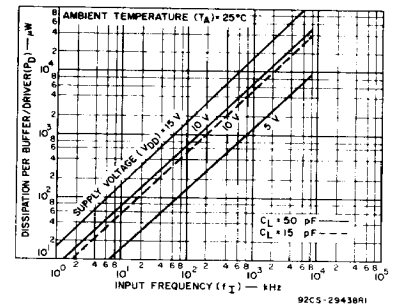


Fig. 6 — Typical power dissipation as a function of input frequency.

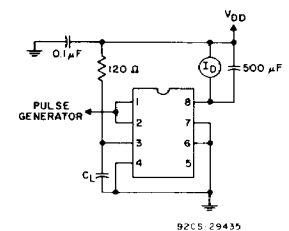
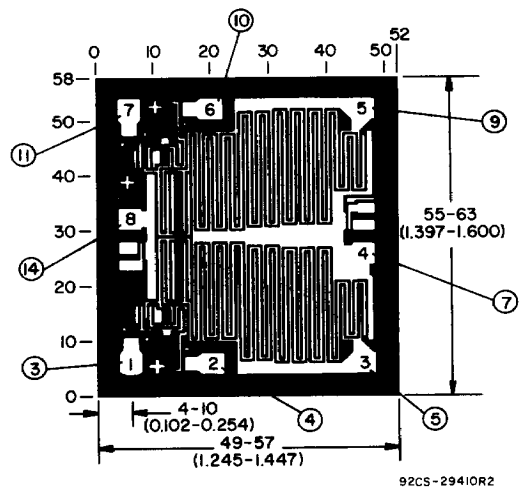


Fig. 7 — Power-dissipation test circuit for CD40107BE.

CD40107B Types

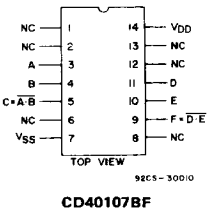
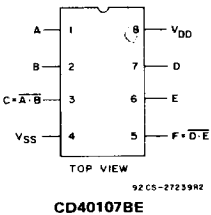


NOTE: NOS. IN PADS FOR CD40107BE  
NOS. OUTSIDE CHIP FOR CD40107BF

Dimensions and Pad Layout for CD40107BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of  $\pm 3$  mils to  $\pm 16$  mils applicable to the nominal dimensions shown.



TERMINAL ASSIGNMENTS

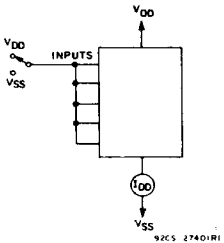


Fig.8 - Quiescent-device current test circuit.

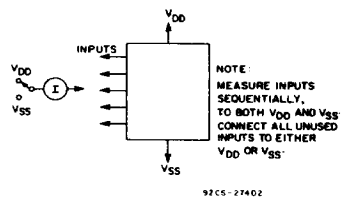


Fig. 9 - Input-current test circuit.

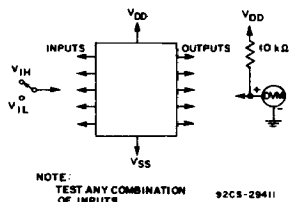


Fig.10 - Input-voltage test circuit.

Special Considerations for CD40107B

- Limiting Capacitive Currents for  $C_L > 500$  pF,  $V_{DD} > 15$  V.**  
For  $V_{DD} > 15$  V, and load capacitance ( $C_L$ ) from output to ground  $> 500$  pF, an external  $25 \Omega$  series limiting resistor should be inserted between the output terminal and  $C_L$ . No external resistor is necessary if  $C_L < 500$  pF or  $V_{DD} < 15$  V.
- Driving Inductive Loads**  
When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.