XLAS080A – MAY 1995

- Second-Generation Video Interface Palette
- Supports System Resolutions of:
  - 1600 × 1280 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate
  - 1280 × 1024 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate
  - 1024 × 768 × 1, 2, 4, 8, 16, 24 Bits/Pixel at 60-Hz and 72-Hz Refresh Rate
  - And lower resolutions
- Direct-Color Modes:
  - 24-Bit/Pixel With 8-Bit Overlay
  - 16-Bit/Pixel (5, 6, 5) XGA® Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1-Bit Overlay (5, 5, 5, 1) TARGA Configuration
  - 12-Bit/Pixel With 4-Bit Overlay (4, 4, 4, 4)
- True-Color Modes:
  - 24-Bit/Pixel With Gamma Correction
  - 16-Bit/Pixel (5, 6, 5) XGA Configuration With Gamma Correction
  - 16-Bit/Pixel (6, 6, 4) Configuration With Gamma Correction
  - 15-Bit/Pixel (5, 5, 5) TARGA® Configuration With Gamma Correction
  - 12-Bit/Pixel (4, 4, 4) With Gamma Correction
- RCLK/SCLK/LCLK Data Latching Allows Flexible Control of VRAM Timing
- Direct Interfacing to Video RAM
- Supports Split Shift-Register Transfers
- 64-Bit-Wide Pixel Bus
- On-Chip Hardware Cursor:
  - 64 × 64 × 2 Cursor (XGA Functionally Compatible)
  - Full-Window Crosshair
  - Dual-Cursor Mode
- 135-, 170-, and 200-MHz Versions
- Supports Overscan for Creation of Custom Screen Borders
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- Windowed Overlay, VGA Capability
- Color-Keyed Switching of Direct Color and Overlay
- On-Chip Clock Selection
- Internal Frequency Doubler
- Triple 8-Bit D/A Converters
- Analog-Output Comparators
- Triple 256 × 8 Color Palette RAMs
- RS-343A-Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette-Page Register
- Horizontal Zooming Capability
- Software Downward Compatible With IMSG176/8 and Bt476/8
- Directly Interfaces to Graphics Processors
- CMOS Technology
- Data Manual Available†

description

The TVP3020 viewpoint palette is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. Maximum flexibility is provided by the pixel multiplexing scheme. The scheme accommodates 64-, 32-, 16-, 8-, and 4-bit pixel buses without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. The device supports selection of little- or big-endian data format for the pixel-bus-frame buffer interface. Data can be split into 1-, 2-, 4-, or 8-bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (5, 5, 5, 1), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. An on-chip, IBM XGA-compatible hardware cursor is incorporated so that further increases in graphics system performance are possible. The device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

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XGA is a trademark of International Business Machines Corporation.

TARGA is a trademark of Truevision Incorporated.

description (continued)

An internal frequency doubler is incorporated, allowing convenient and cost-effective clock source alternatives to be utilized.

An auxiliary windowing function and a pixel-port-select function are provided so that overlay or VGA graphics can be displayed on top of direct color inside or outside a specified auxiliary window. Color-keyed switching of direct color and overlay is also supported.

Clocking is provided through one of three inputs (two TTL- and one ECL/TTL-compatible) and is software selectable. The video clock, shift clock, and reference clock outputs provide a software-selected divide ratio of the chosen clock input.

The TVP3020 has three 256-by-8 color lookup tables with triple, 8-bit video, digital-to-analog converters (DACs) capable of directly driving a doubly terminated, 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync (HSYNC) and vertical sync (VSYNC) are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register provides the additional bits of the palette address when 1-, 2-, or 4-bit planes are used. This allows the screen colors to be changed with only one microprocessor interface unit (MPU) write cycle.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. This allows a replacement graphics board to remain downward compatible by utilizing the existing graphics circuitry often located on the motherboard.

The viewpoint VIP is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. The split shift-register transfer function, which is supported by VRAM, is also supported by the TVP3020.

The system-integration concept is carried to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette, the graphics board, and the graphics system.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			FLAT PACK (MDN)	FLAT PACK (PCE)
0°C to 70°C	135 MHz	8 Bits	–	TVP3020–135PCE
	170 MHz	8 Bits	–	TVP3020–170PCE
	200 MHz	8 Bits	TVP3020–200MDN	–

functional block diagram

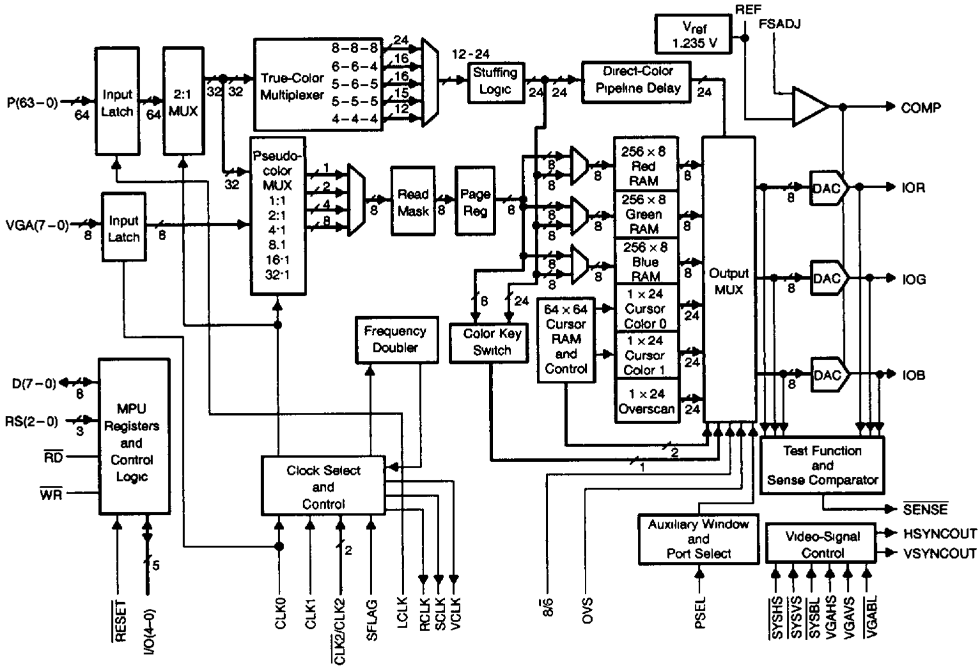

Figure 1. Functional Block Diagram