

## LP3985

# Micropower, 150mA Low-Noise Ultra Low-Dropout CMOS Voltage Regulator

## General Description

The LP3985 is designed for portable and wireless applications with demanding performance and space requirements.

The LP3985 is stable with a small  $1\mu\text{F}$   $\pm 30\%$  ceramic or high-quality tantalum output capacitor. The micro SMD requires the smallest possible PC board area - the total application circuit area can be less than  $2.0\text{mm} \times 2.5\text{mm}$ , a fraction of a 1206 case size.

The LP3985's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Fast start-up time is achieved by utilizing an internal power-on circuit that actively pre-charges the bypass capacitor.

Power supply rejection is better than 50 dB at low frequencies and starts to roll off at 1kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA, from a 2.5V to 6V input. The LP3985 consumes less than  $1.5\mu\text{A}$  in disable mode and has fast turn-on time less than  $200\mu\text{s}$ .

The LP3985 is available in a 5 bump small bump micro SMD, a 5 bump large bump micro SMD, a 5 bump thin micro SMD and a 5 pin SOT-23 package. Performance is specified for  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range and is available in 2.5V,

2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.2V, 3.3V, 4.7V, 4.8V and 5.0V output voltages. For other output voltage options between 2.5V to 5.0V or for a dual LP3985, please contact National Semiconductor sales office.

## Key Specifications

- 2.5 to 6.0V input range
- 150mA guaranteed output
- 50dB PSRR at 1kHz @  $V_{\text{IN}} = V_{\text{OUT}} + 0.2\text{V}$
- $\leq 1.5\mu\text{A}$  quiescent current when shut down
- Fast Turn-On time:  $200\mu\text{s}$  (typ.)
- 100mV maximum dropout with 150mA load
- $30\mu\text{V}_{\text{rms}}$  output noise (typ) over 10Hz to 100kHz
- $-40$  to  $+125^{\circ}\text{C}$  junction temperature range for operation
- 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.2V, 3.3V, 4.7V, 4.8V and 5.0V outputs standard

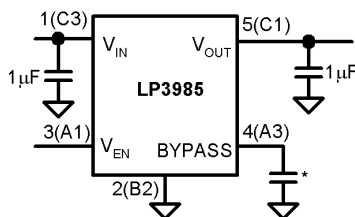
## Features

- Miniature 5-I/O micro SMD and SOT-23-5 package
- Logic controlled enable
- Stable with ceramic and high quality tantalum capacitors
- Fast turn-on
- Thermal shutdown and short-circuit current limit

## Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances

## Typical Application Circuit

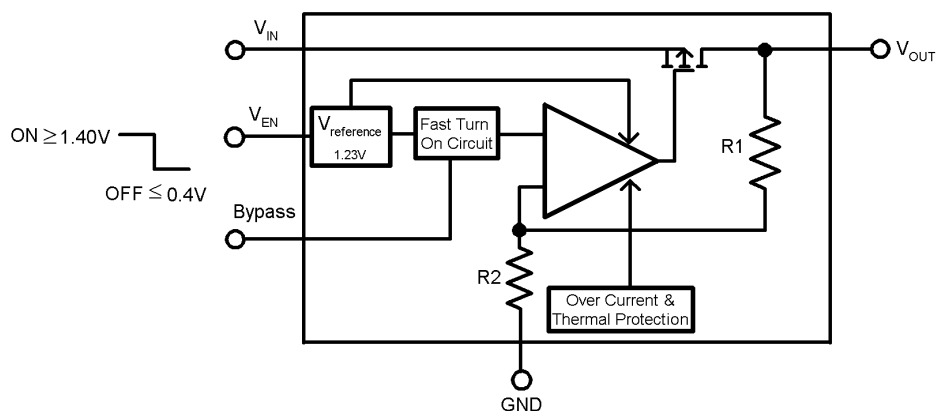


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Note: Pin Numbers in parenthesis indicate micro SMD package.

\* Optional Noise Reduction Capacitor.

## Block Diagram



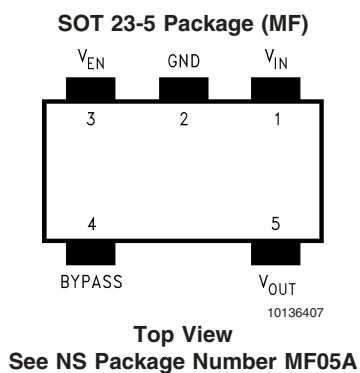
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## Pin Description

Name	* micro SMD	SOT	Function
V <sub>EN</sub>	A1	3	Enable Input Logic, Enable High
GND	B2	2	Common Ground
V <sub>OUT</sub>	C1	5	Output Voltage of the LDO
V <sub>IN</sub>	C3	1	Input Voltage of the LDO
BYPASS	A3	4	Optional Bypass Capacitor for Noise Reduction

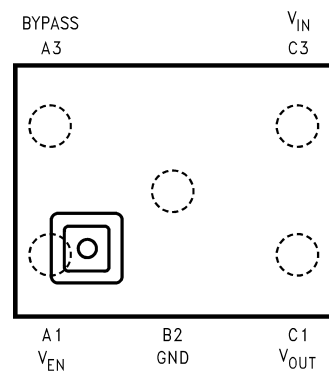
\* The pin numbering scheme for the micro SMD package was revised in April 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had V<sub>EN</sub> as pin 1, GND as pin 2, V<sub>OUT</sub> as pin 3, V<sub>IN</sub> as pin 4, and BYPASS as pin 5.

## Connection Diagrams



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### 5 Bump micro SMD Package (BPA05, BLA05, TLA05)



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## Ordering Information

BP refers to 0.170mm bump size, 0.900mm height for micro SMD Package

Output Voltage (V)	Grade	LP3985 Supplied as 250 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel
2.5	STD	LP3985IBP-2.5	LP3985IBPX-2.5
2.6	STD	LP3985IBP-2.6	LP3985IBPX-2.6
2.7	STD	LP3985IBP-2.7	LP3985IBPX-2.7
2.8	STD	LP3985IBP-2.8	LP3985IBPX-2.8
2.85	STD	LP3985IBP-285	LP3985IBPX-285
2.9	STD	LP3985IBP-2.9	LP3985IBPX-2.9
3.0	STD	LP3985IBP-3.0	LP3985IBPX-3.0
3.1	STD	LP3985IBP-3.1	LP3985IBPX-3.1
3.2	STD	LP3985IBP-3.2	LP3985IBPX-3.2
3.3	STD	LP3985IBP-3.3	LP3985IBPX-3.3
4.7	STD	LP3985IBP-4.7	LP3985IBPX-4.7
5.0	STD	LP3985IBP-5.0	LP3985IBPX-5.0

BL refers to 0.300mm bump size, 0.995mm height for micro SMD Package

Output Voltage (V)	Grade	LP3985 Supplied as 250 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel
2.5	STD	LP3985IBL-2.5	LP3985IBLX-2.5
2.6	STD	LP3985IBL-2.6	LP3985IBLX-2.6
2.7	STD	LP3985IBL-2.7	LP3985IBLX-2.7
2.8	STD	LP3985IBL-2.8	LP3985IBLX-2.8
2.85	STD	LP3985IBL-285	LP3985IBLX-285
2.9	STD	LP3985IBL-2.9	LP3985IBLX-2.9
3.0	STD	LP3985IBL-3.0	LP3985IBLX-3.0
3.1	STD	LP3985IBL-3.1	LP3985IBLX-3.1
3.2	STD	LP3985IBL-3.2	LP3985IBLX-3.2
3.3	STD	LP3985IBL-3.3	LP3985IBLX-3.3
4.8	STD	LP3985IBL-4.8	LP3985IBLX-4.8
5.0	STD	LP3985IBL-5.0	LP3985IBLX-5.0

TL refers to 0.300mm bump size, 0.600mm height for micro SMD Package

Output Voltage (V)	Grade	LP3985 Supplied as 250 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel
2.5	STD	LP3985ITL-2.5	LP3985ITLX-2.5
2.6	STD	LP3985ITL-2.6	LP3985ITLX-2.6
2.7	STD	LP3985ITL-2.7	LP3985ITLX-2.7
2.8	STD	LP3985ITL-2.8	LP3985ITLX-2.8
2.85	STD	LP3985ITL-285	LP3985ITLX-285
2.9	STD	LP3985ITL-2.9	LP3985ITLX-2.9
3.0	STD	LP3985ITL-3.0	LP3985ITLX-3.0
3.1	STD	LP3985ITL-3.1	LP3985ITLX-3.1
3.2	STD	LP3985ITL-3.2	LP3985ITLX-3.2
3.3	STD	LP3985ITL-3.3	LP3985ITLX-3.3
4.8	STD	LP3985ITL-4.8	LP3985ITLX-4.8
5.0	STD	LP3985ITL-5.0	LP3985ITLX-5.0

## Ordering Information (Continued)

### For SOT Package

Output Voltage (V)	Grade	LP3985 Supplied as 1000 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel	Package Marking
2.5	STD	LP3985IM5-2.5	LP3985IM5X-2.5	LCSB
2.6	STD	LP3985IM5-2.6	LP3985IM5X-2.6	LCTB
2.7	STD	LP3985IM5-2.7	LP3985IM5X-2.7	LCUB
2.8	STD	LP3985IM5-2.8	LP3985IM5X-2.8	LCJB
2.85	STD	LP3985IM5-285	LP3985IM5X-285	LCXB
2.9	STD	LP3985IM5-2.9	LP3985IM5X-2.9	LCYB
3.0	STD	LP3985IM5-3.0	LP3985IM5X-3.0	LCRB
3.1	STD	LP3985IM5-3.1	LP3985IM5X-3.1	LCZB
3.2	STD	LP3985IM5-3.2	LP3985IM5X-3.2	LDPB
3.3	STD	LP3985IM5-3.3	LP3985IM5X-3.3	LDQB
4.7	STD	LP3985IM5-4.7	LP3985IM5X-4.7	LDRB
5.0	STD	LP3985IM5-5.0	LP3985IM5X-5.0	LDSB

**Absolute Maximum Ratings** (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{IN}, V_{EN}$	-0.3 to 6.5V
$V_{OUT}$	-0.3 to $(V_{IN}+0.3) \leq 6.5V$
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C
Lead Temp.	235°C
Pad Temp. (Note 3)	235°C
Maximum Power Dissipation	
SOT23-5 (Note 4)	364mW
micro SMD (Note 4)	355mW
ESD Rating(Note 5)	
Human Body Model	2kV
Machine Model	150V

**Operating Ratings** (Notes 1, 2)

$V_{IN}$	2.5 to 6V
$V_{EN}$	0 to $(V_{IN}+0.3) \leq 6V$
Junction Temperature	-40°C to +125°C
Thermal Resistance	
$\theta_{JA}$ (SOT23-5)	220°C/W
$\theta_{JA}$ (micro SMD)	255°C/W
Maximum Power Dissipation	
SOT23-5 (Note 6)	250mW
micro SMD (Note 6)	244mW

**Electrical Characteristics**

Unless otherwise specified:  $V_{IN} = V_{OUT(nom)} + 0.5V$ ,  $C_{IN} = 1 \mu F$ ,  $I_{OUT} = 1mA$ ,  $C_{OUT} = 1 \mu F$ ,  $C_{BYPASS} = 0.01 \mu F$ . Typical values and limits appearing in standard typeface are for  $T_J = 25^\circ C$ . Limits appearing in **boldface type** apply over the entire junction temperature range for operation, -40°C to +125°C. (Note 7) (Note 8)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$\Delta V_{OUT}$	Output Voltage Tolerance	$I_{OUT} = 1mA$		-2 -3	2 3	% of $V_{OUT(nom)}$
	Line Regulation Error	$V_{IN} = (V_{OUT(nom)} + 0.5V)$ to 6.0V, For 4.7 to 5.0 options For all other options		-0.19 -0.1	0.19 0.1	%/V
	Load Regulation Error (Note 9)	$I_{OUT} = 1mA$ to 150 mA LP3985IM5 (SOT23-5)	0.0025		0.005	%/mA
		LP3985 (micro SMD)	0.0004		0.002	
	Output AC Line Regulation	$V_{IN} = V_{OUT(nom)} + 1V$ , $I_{OUT} = 150mA$ (Figure 1)	1.5			mV <sub>P-P</sub>
PSRR	Power Supply Rejection Ratio	$V_{IN} = V_{OUT(nom)} + 0.2V$ , $f = 1kHz$ , $I_{OUT} = 50mA$ (Figure 2)	50			dB
		$V_{IN} = V_{OUT(nom)} + 0.2V$ , $f = 10kHz$ , $I_{OUT} = 50mA$ (Figure 2)	40			
$I_Q$	Quiescent Current	$V_{EN} = 1.4V$ , $I_{OUT} = 0mA$ For 4.7 to 5.0 options For all other options	100 85		165 150	$\mu A$
		$V_{EN} = 1.4V$ , $I_{OUT} = 0$ to 150 mA For 4.7 to 5.0 options For all other options	155 140		250 200	
		$V_{EN} = 0.4V$	0.003		1.5	
	Dropout Voltage (Note 10)	$I_{OUT} = 1mA$	0.4		2	mV
		$I_{OUT} = 50mA$	20		35	
		$I_{OUT} = 100mA$	45		70	
		$I_{OUT} = 150mA$	60		100	
$I_{SC}$	Short Circuit Current Limit	Output Grounded (Steady State)	600			mA
$I_{OUT(PK)}$	Peak Output Current	$V_{OUT} \geq V_{OUT(nom)} - 5\%$	550	300		mA

## Electrical Characteristics (Continued)

Unless otherwise specified:  $V_{IN} = V_{OUT(nom)} + 0.5V$ ,  $C_{IN} = 1\ \mu F$ ,  $I_{OUT} = 1mA$ ,  $C_{OUT} = 1\ \mu F$ ,  $C_{BYPASS} = 0.01\mu F$ . Typical values and limits appearing in standard typeface are for  $T_J = 25^\circ C$ . Limits appearing in **boldface type** apply over the entire junction temperature range for operation,  $-40^\circ C$  to  $+125^\circ C$ . (Note 7) (Note 8)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$T_{ON}$	Turn-On Time (Note 11)	$C_{BYPASS} = 0.01\ \mu F$	200			$\mu s$
$e_n$	Output Noise Voltage (Note 12)	$BW = 10\ Hz\ to\ 100\ kHz$ , $C_{OUT} = 1\ \mu F$	30			$\mu V_{rms}$
	Output Noise Density	$C_{BP} = 0$	230			$nV/\sqrt{Hz}$
$I_{EN}$	Maximum Input Current at EN	$V_{EN} = 0.4$ and $V_{IN} = 6.0$	$\pm 1$			nA
$V_{IL}$	Maximum Low Level Input Voltage at EN	$V_{IN} = 2.5\ to\ 6.0V$			<b>0.4</b>	V
$V_{IH}$	Minimum High Level Input Voltage at EN	$V_{IN} = 2.5\ to\ 6.0V$		<b>1.4</b>		V
$C_{OUT}$	Output Capacitor	Capacitance		<b>1</b>	<b>20</b>	$\mu F$
		ESR		<b>5</b>	<b>500</b>	m $\Omega$
TSD	Thermal Shutdown Temperature		160			$^\circ C$
	Thermal Shutdown Hysteresis		20			$^\circ C$

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pin.

**Note 3:** Additional information on lead temperature and pad temperature can be found in National Semiconductor Application Note (AN-1112).

**Note 4:** The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:  $P_D = (T_J - T_A)/\theta_{JA}$ ,

where  $T_J$  is the junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance. The 364mW rating for SOT23-5 appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature,  $150^\circ C$ , for  $T_J$ ,  $70^\circ C$  for  $T_A$ , and  $220^\circ C/W$  for  $\theta_{JA}$ . More power can be dissipated safely at ambient temperatures below  $70^\circ C$ . Less power can be dissipated safely at ambient temperatures above  $70^\circ C$ . The Absolute Maximum power dissipation can be increased by  $4.5mW$  for each degree below  $70^\circ C$ , and it must be derated by  $4.5mW$  for each degree above  $70^\circ C$ .

**Note 5:** The human body model is  $100pF$  discharged through  $1.5k\Omega$  resistor into each pin. The machine model is a  $200\ pF$  capacitor discharged directly into each pin.

**Note 6:** Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The  $250mW$  rating for SOT23-5 appearing under Operating Ratings results from substituting the maximum junction temperature for operation,  $125^\circ C$ , for  $T_J$ ,  $70^\circ C$  for  $T_A$ , and  $220^\circ C/W$  for  $\theta_{JA}$  into (Note 4) above. More power can be dissipated at ambient temperatures below  $70^\circ C$ . Less power can be dissipated at ambient temperatures above  $70^\circ C$ . The maximum power dissipation for operation can be increased by  $4.5mW$  for each degree below  $70^\circ C$ , and it must be derated by  $4.5mW$  for each degree above  $70^\circ C$ .

**Note 7:** All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with  $T_J = 25^\circ C$  or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 8:** The target output voltage, which is labeled  $V_{OUT(nom)}$ , is the desired voltage option.

**Note 9:** An increase in the load current results in a slight decrease in the output voltage and vice versa.

**Note 10:** Dropout voltage is the input-to-output voltage difference at which the output voltage is  $100mV$  below its nominal value. This specification does not apply for input voltages below  $2.5V$ .

**Note 11:** Turn-on time is time measured between the enable input just exceeding  $V_{IH}$  and the output voltage just reaching 95% of its nominal value.

**Note 12:** The output noise varies with output voltage option. The  $30\mu V_{rms}$  is measured with  $2.5V$  voltage option. To calculate an approximated output noise for other options, use the equation:  $(30\mu V_{rms})(X)/2.5$ , where  $X$  is the voltage option value.

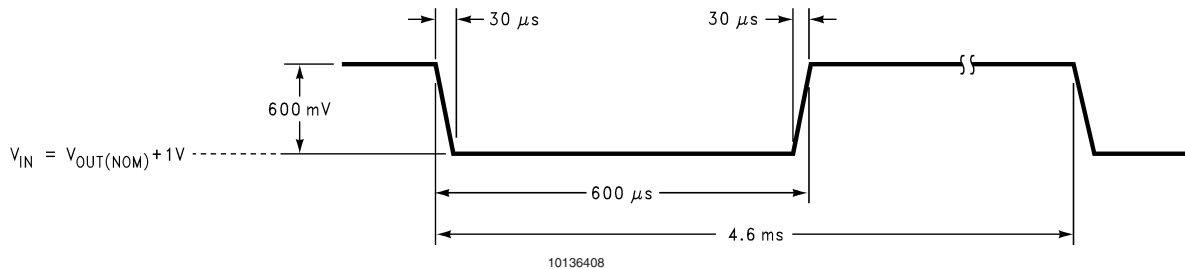


FIGURE 1. Line Transient Input Test Signal

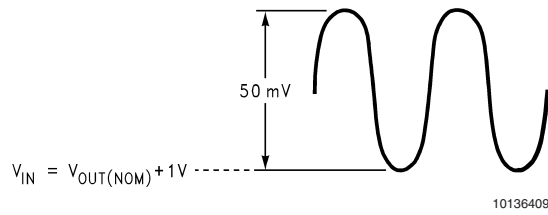
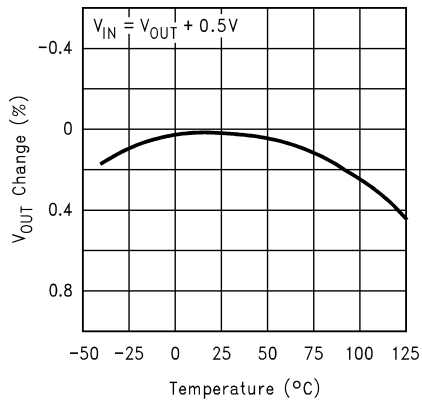


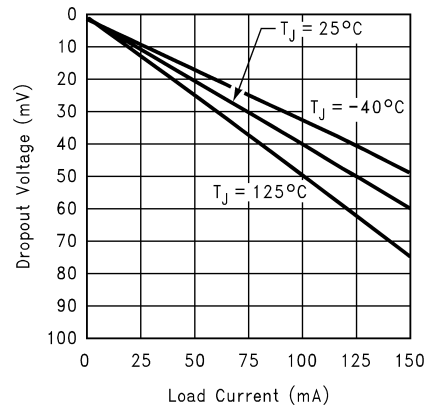
FIGURE 2. PSRR Input Test Signal

**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1 \mu F$  Ceramic,  $C_{BYPASS} = 0.01 \mu F$ ,  $V_{IN} = V_{OUT} + 0.2V$ ,  $T_A = 25^\circ C$ , Enable pin is tied to  $V_{IN}$ .

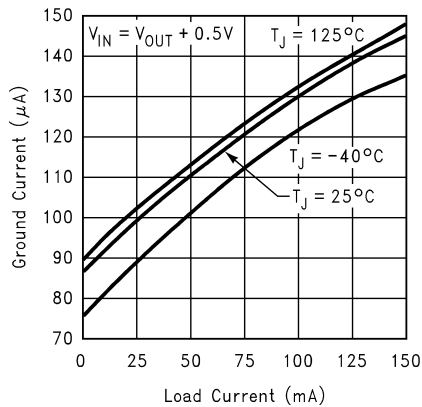
Output Voltage Change vs Temperature



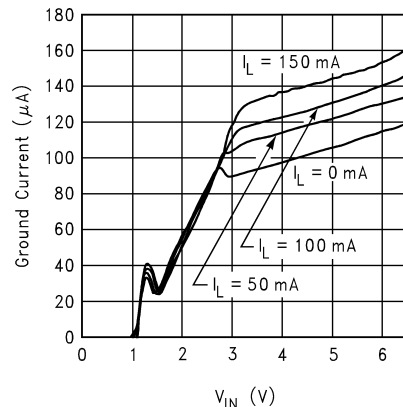
Dropout Voltage vs Load Current



Ground Current vs Load Current

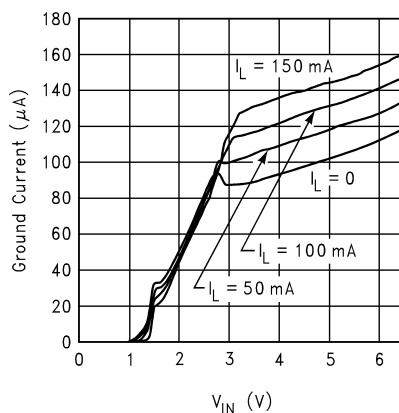


Ground Current vs  $V_{IN}$  @  $25^\circ C$



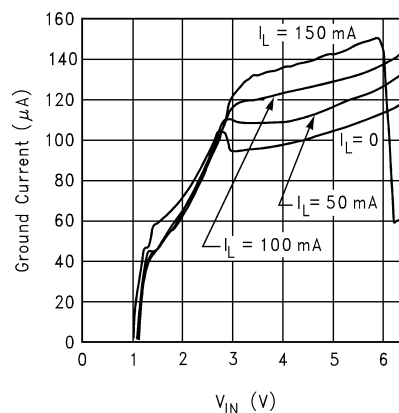
**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  Ceramic,  $C_{BYPASS} = 0.01\ \mu\text{F}$ ,  $V_{IN} = V_{OUT} + 0.2\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ . (Continued)

**Ground Current vs  $V_{IN}$  @  $-40^\circ\text{C}$**



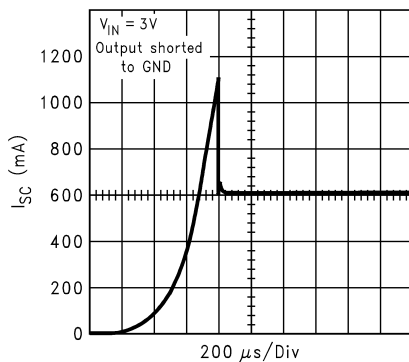
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**Ground Current vs  $V_{IN}$  @  $125^\circ\text{C}$**



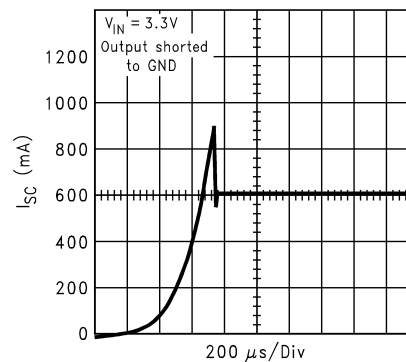
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**Short Circuit Current (micro SMD)**



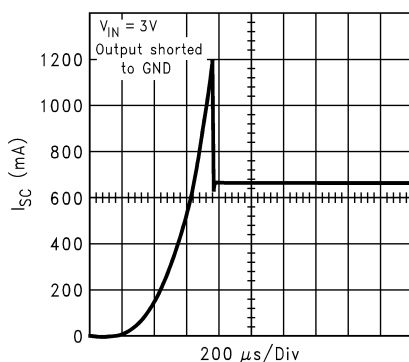
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**Short Circuit Current (micro SMD)**



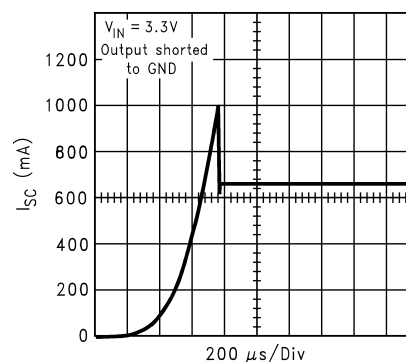
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**Short Circuit Current (SOT)**



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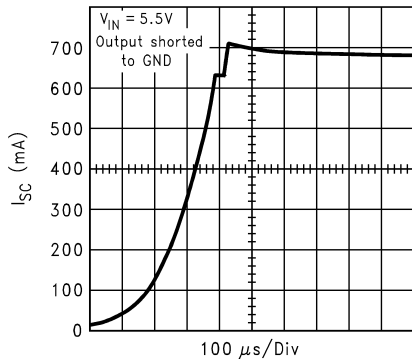
**Short Circuit Current (SOT)**



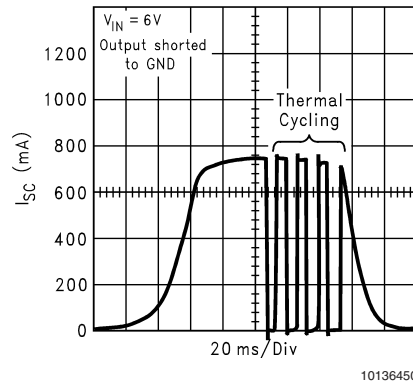
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**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1 \mu F$  Ceramic,  $C_{BYPASS} = 0.01 \mu F$ ,  $V_{IN} = V_{OUT} + 0.2V$ ,  $T_A = 25^\circ C$ , Enable pin is tied to  $V_{IN}$ . (Continued)

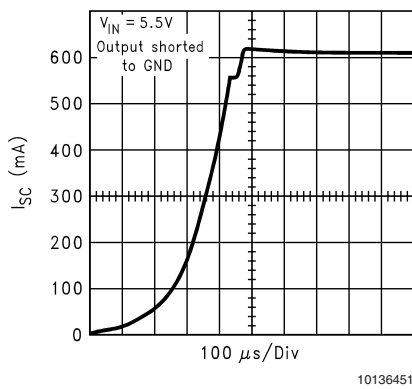
**Short Circuit Current (SOT)**



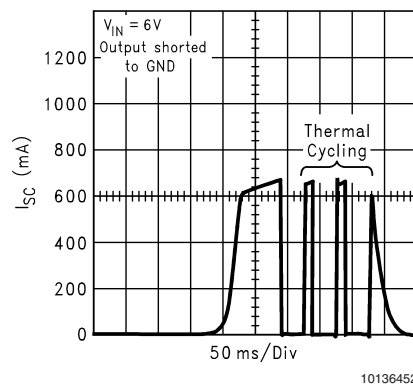
**Short Circuit Current (SOT)**



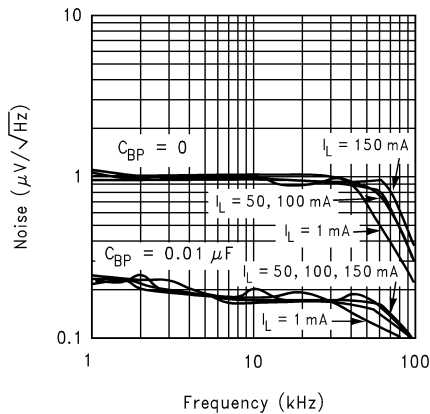
**Short Circuit Current (micro SMD)**



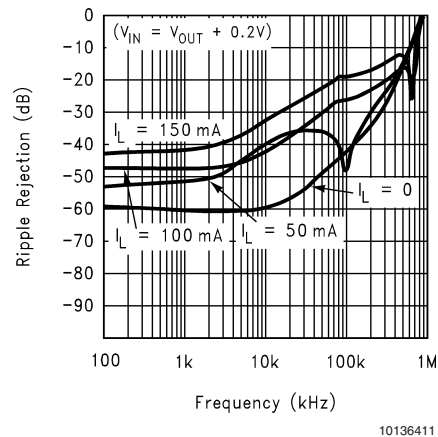
**Short Circuit Current (micro SMD)**



**Output Noise Spectral Density**

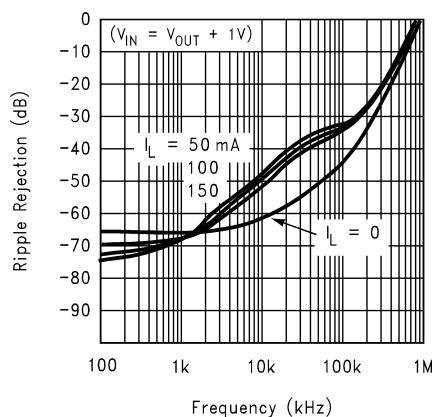


**Ripple Rejection ( $V_{IN} = V_{OUT} + 0.2V$ )**



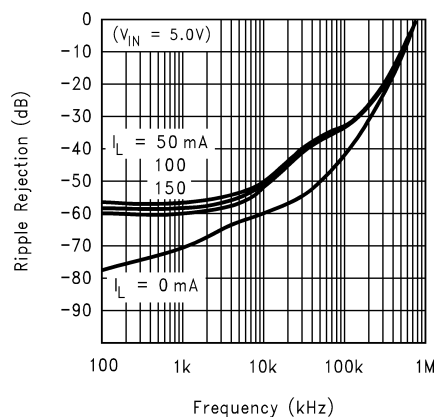
**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  Ceramic,  $C_{BYPASS} = 0.01\ \mu\text{F}$ ,  $V_{IN} = V_{OUT} + 0.2\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ . (Continued)

**Ripple Rejection ( $V_{IN} = V_{OUT} + 1\text{V}$ )**



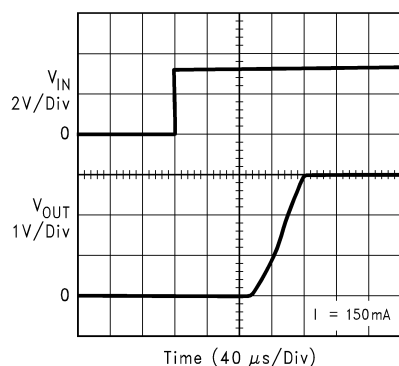
10136412

**Ripple Rejection ( $V_{IN} = 5.0\text{V}$ )**



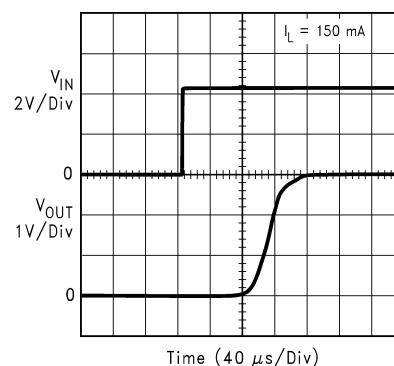
10136413

**Start Up Time ( $V_{IN} = V_{OUT} + 0.2\text{V}$ )**



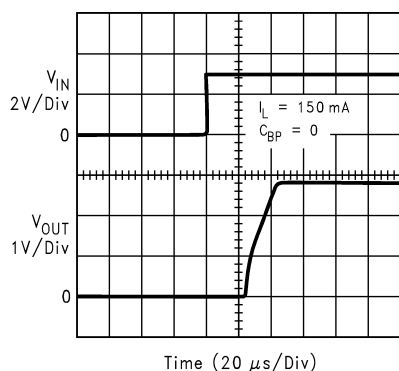
10136414

**Start Up Time ( $V_{IN} = 4.2\text{V}$ )**



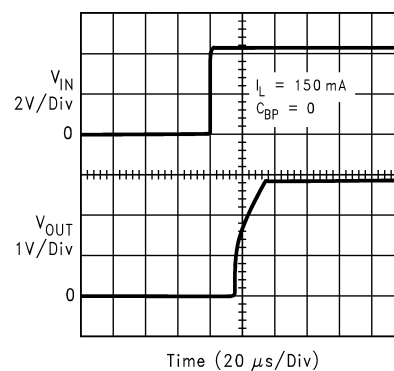
10136415

**Start Up Time ( $V_{IN} = V_{OUT} + 0.2\text{V}$ )**



10136416

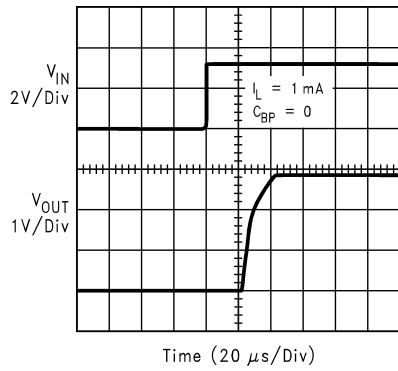
**Start Up Time ( $V_{IN} = 4.2\text{V}$ )**



10136417

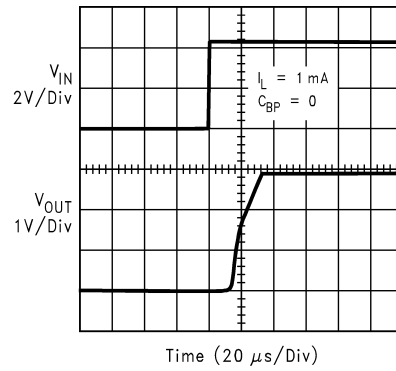
**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1 \mu F$  Ceramic,  $C_{BYPASS} = 0.01 \mu F$ ,  $V_{IN} = V_{OUT} + 0.2V$ ,  $T_A = 25^\circ C$ , Enable pin is tied to  $V_{IN}$ . (Continued)

**Start Up Time ( $V_{IN} = V_{OUT} + 0.2V$ )**



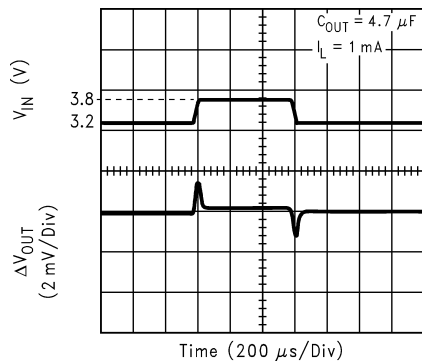
10136418

**Start Up Time ( $V_{IN} = 4.2V$ )**



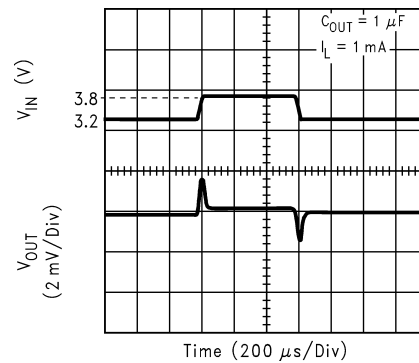
10136419

**Line Transient Response**



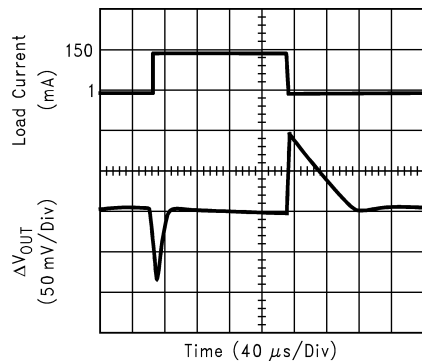
10136420

**Line Transient Response**



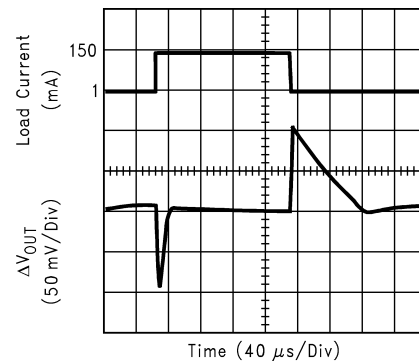
10136421

**Load Transient Response ( $V_{IN} = 3.2V$ )**



10136423

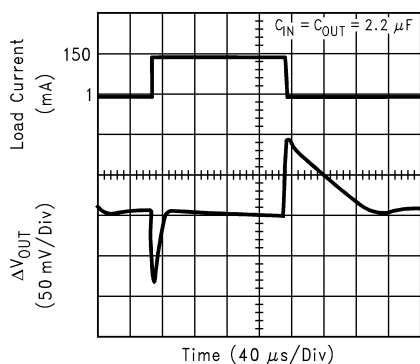
**Load Transient Response ( $V_{IN} = 4.2V$ )**



10136422

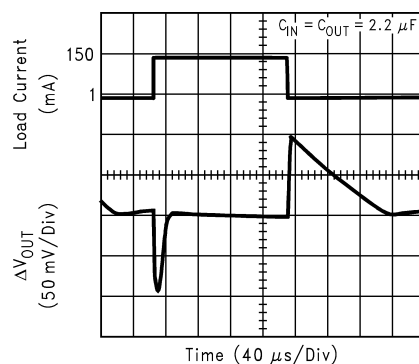
**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  Ceramic,  $C_{BYPASS} = 0.01\ \mu\text{F}$ ,  $V_{IN} = V_{OUT} + 0.2\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ . (Continued)

**Load Transient Response ( $V_{IN} = 3.2\text{V}$ )**



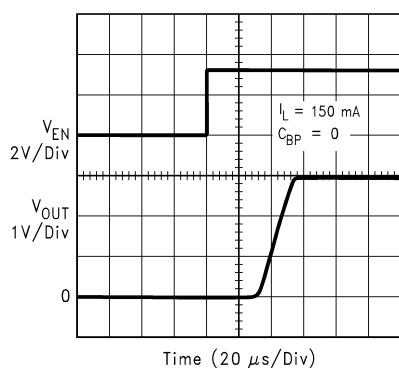
10136424

**Load Transient Response ( $V_{IN} = 4.2\text{V}$ )**



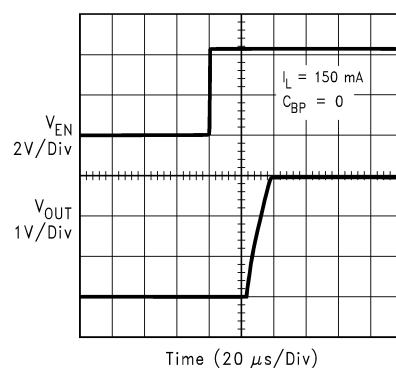
10136425

**Enable Response ( $V_{IN} = V_{OUT} + 0.2\text{V}$ )**



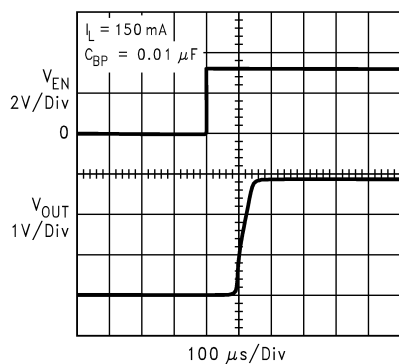
10136453

**Enable Response ( $V_{IN} = 4.2\text{V}$ )**



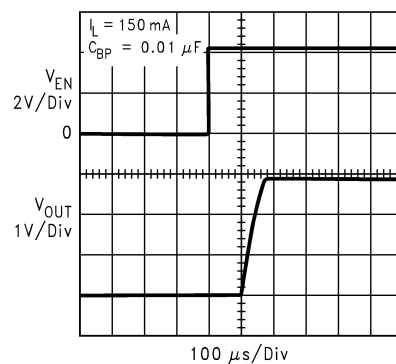
10136454

**Enable Response ( $V_{IN} = V_{OUT} + 0.2\text{V}$ )**



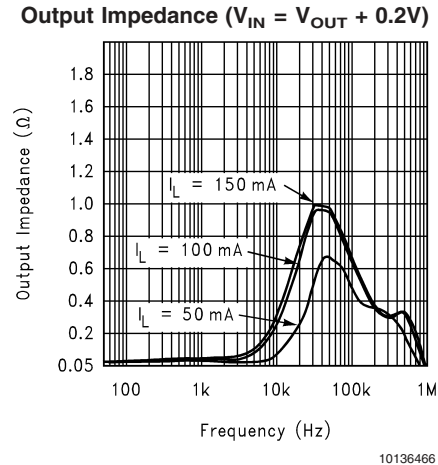
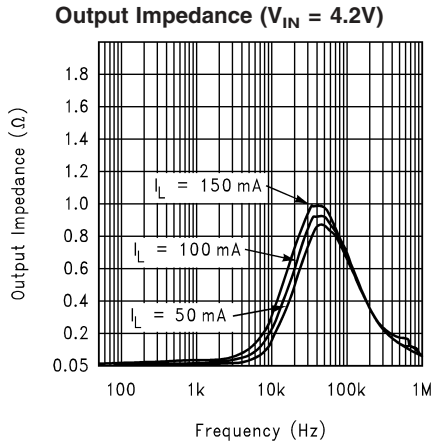
10136455

**Enable Response ( $V_{IN} = 4.2\text{V}$ )**



10136456

**Typical Performance Characteristics** Unless otherwise specified,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  Ceramic,  $C_{BYPASS} = 0.01\ \mu\text{F}$ ,  $V_{IN} = V_{OUT} + 0.2\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ . (Continued)



## Application Hints

### EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3985 requires external capacitors for regulator stability. The LP3985 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### INPUT CAPACITOR

An input capacitance of  $\approx 1\ \mu\text{F}$  is required between the LP3985 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be  $\approx 1\ \mu\text{F}$  over the entire operating temperature range.

### OUTPUT CAPACITOR

The LP3985 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature characteristics X7R, X5R, Z5U, or Y5V) in 1 to 22  $\mu\text{F}$  range with 5m $\Omega$  to 500m $\Omega$  ESR range is suitable in the LP3985 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 m $\Omega$  to 500 m $\Omega$ ).

### NO-LOAD STABILITY

The LP3985 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

### CAPACITOR CHARACTERISTICS

The LP3985 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 $\mu\text{F}$  to 4.7 $\mu\text{F}$  range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 $\mu\text{F}$  ceramic capacitor is in the range of 20 m $\Omega$  to 40 m $\Omega$ , which easily meets the ESR requirement for stability by the LP3985.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ , will only vary the capacitance to within  $\pm 15\%$ . Most large value ceramic capacitors ( $\approx 2.2\ \mu\text{F}$ ) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from  $25^\circ\text{C}$  to  $85^\circ\text{C}$ . Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below  $25^\circ\text{C}$ .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 $\mu\text{F}$  to 4.7 $\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from  $25^\circ\text{C}$  down to  $-40^\circ\text{C}$ , so some guard band must be allowed.

### NOISE BYPASS CAPACITOR

Connecting a 0.01 $\mu\text{F}$  capacitor between the  $C_{BYPASS}$  pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node

## Application Hints (Continued)

in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO's, addition of a noise reduction capacitor does not effect the load transient response of the device.

### ON/OFF INPUT OPERATION

The LP3985 is turned off by pulling the  $V_{EN}$  pin low, and turned on by pulling it high. If this feature is not used, the  $V_{EN}$  pin should be tied to  $V_{IN}$  to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the  $V_{EN}$  input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{IL}$  and  $V_{IH}$ .

### FAST ON-TIME

The LP3985 output is turned on after  $V_{ref}$  voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70uA current source. The current source is turned

off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

### micro SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note (AN-1112). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

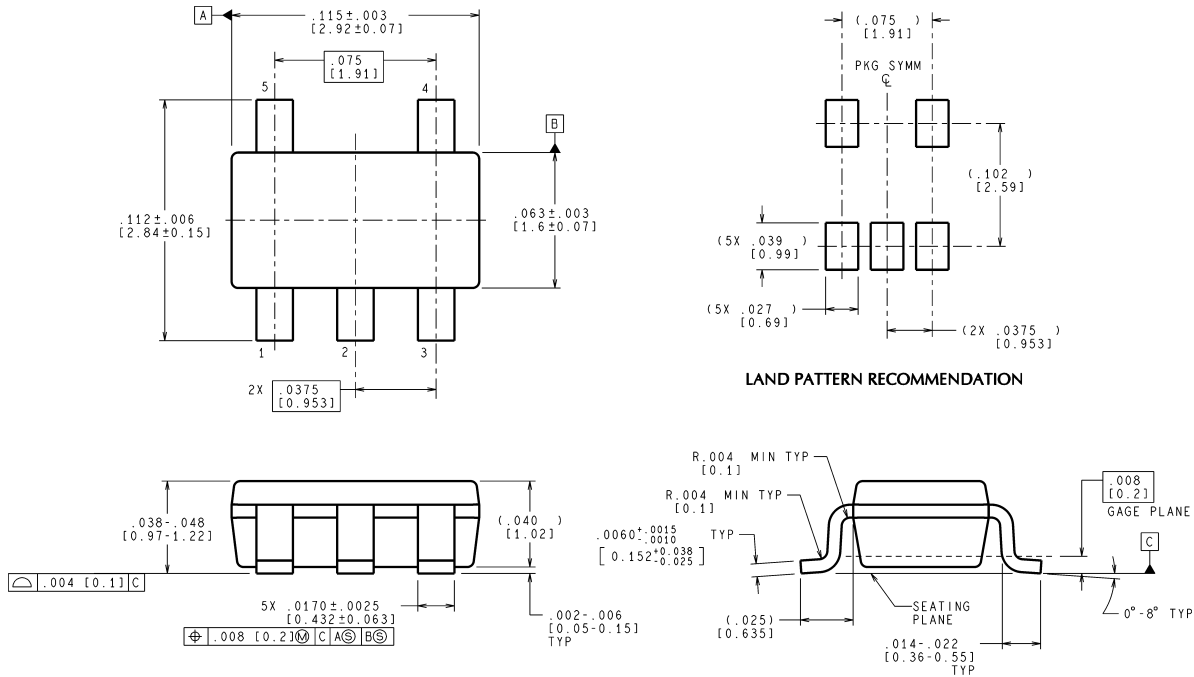
### micro SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A micro SMD test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

# Physical Dimensions inches (millimeters)

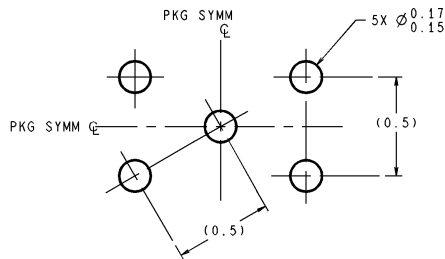
unless otherwise noted



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

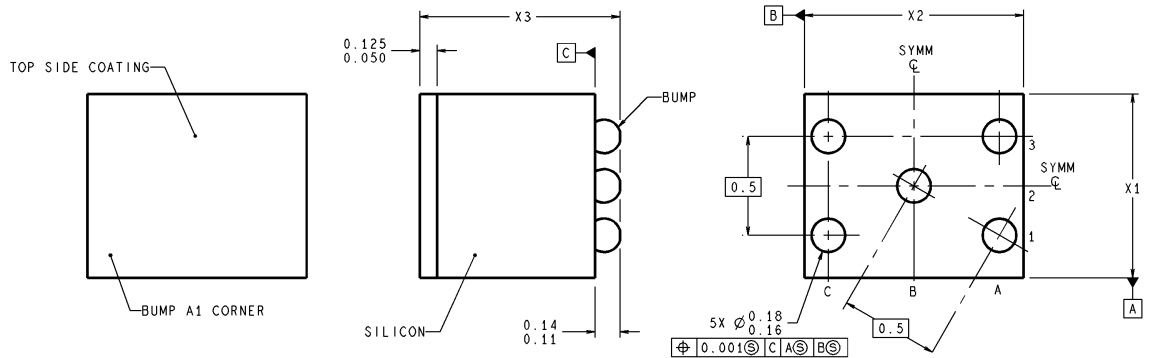
MF05A (Rev B)

## 5-Lead Small Outline Package (MF) NS Package Number MF05A



DIMENSIONS ARE IN MILLIMETERS

### LAND PATTERN RECOMMENDATION

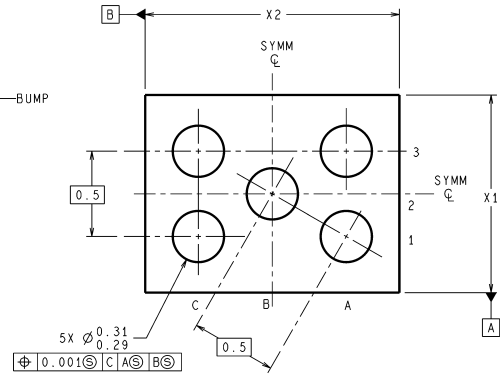


BPA05XXX (Rev C)

**micro SMD, 5 Bump, Package (BPA05)**  
**NS Package Number BPA05CMC**  
The dimensions for X1, X2 and X3 are as given:  
X1 =  $0.828 \pm 0.03$ mm  
X2 =  $1.387 \pm 0.03$ mm  
X3 =  $0.900 \pm 0.10$ mm

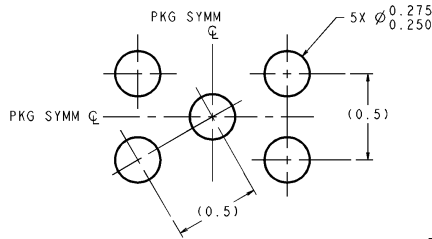


Technical drawing of a square silicon chip. The chip is labeled "SILICON". The overall width is dimensioned as  $X3$ . The overall height is dimensioned as  $0.265$  and  $0.215$ . The chip has a central square area and a smaller square area on the right side labeled "C". The chip is mounted on a substrate with a "BUMP" on the right side. The chip is labeled "SILICON". The chip is labeled "SILICON".



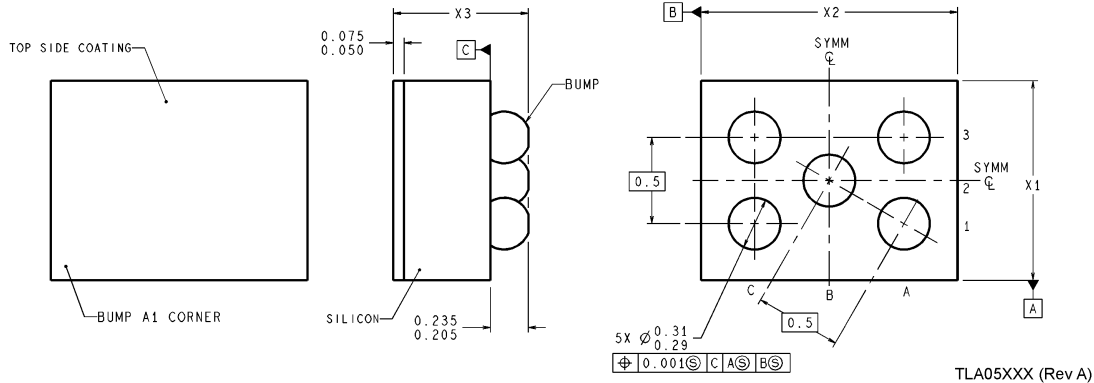
micro SMD, 5 Bump, Package (BLA05)  
NS Package Number BLA05ADC  
The dimensions for X1, X2 and X3 are as given:  
X1 = 1.006 +/- 0.03mm  
X2 = 1.438 +/- 0.03mm  
X3 = 0.995 +/- 0.10mm

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

### LAND PATTERN RECOMMENDATION



thin micro SMD, 5 Bump, Package (TLA05)  
 NS Package Number TLA05ADA  
 The dimensions for X1, X2 and X3 are as given:  
 X1 = 1.006 +/- 0.03mm  
 X2 = 1.438 +/- 0.03mm  
 X3 = 0.6 +/- 0.075mm

TLA05XXX (Rev A)

## LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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