

DATA SHEET

GTL16612

18-bit GTL/GTL⁺ to LVTTL/TTL
bidirectional universal translator (3-State)

Product data
Supersedes data of 2000 Jun 19

2002 Dec 13

18-bit GTL/GTL⁺ to LVTTL/TTL bidirectional universal translator (3-State)

GTL16612

FEATURES

- 18-bit bidirectional bus interface
- Translates between GTL/GTL⁺ logic levels (B ports) and LVTTL/TTL logic levels (A ports)
- 5 V I/O tolerant on the LVTTL/TTL side (A ports)
- No bus current loading when LVTTL/TTL output is tied to 5 V bus
- 3-State buffers
- Output capability: +64 mA/-32 mA on the LVTTL/TTL side (A ports); +40 mA on the GTL/GTL⁺ side (B ports)
- TTL input levels on control pins
- Power-up reset
- Power-up 3-State
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The GTL16612 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V with I/O compatibility up to 5 V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When $\overline{OEAB}$ is Low, the outputs are active. When $\overline{OEAB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CEBA}/\overline{CEAB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25 °C	TYPICAL	UNIT
			3.3 V	
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	C _L = 50 pF	1.9	ns
C _{IN}	Input capacitance (Control pins)	V _I = 0 V or V _{CC}	4	pF
C _{I/O}	I/O pin capacitance	Outputs disabled; V _{I/O} = 0 V or V _{CC}	8	pF
I _{CCZ}	Total supply current	Outputs disabled	12	mA

ORDERING INFORMATION

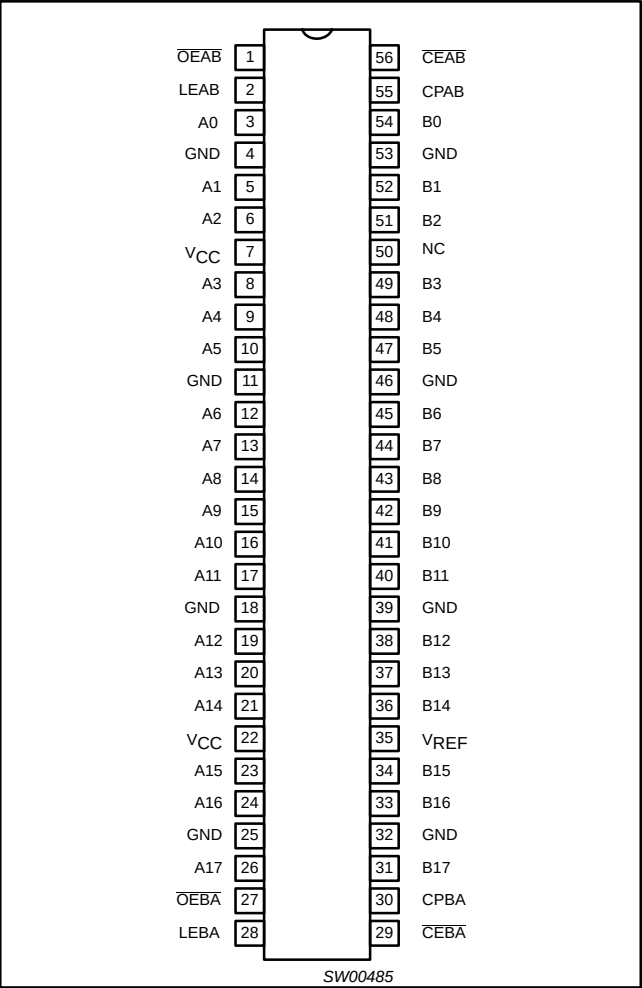
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP	-40 to +85 °C	GTL16612DL	SOT371-1
56-Pin Plastic TSSOP	-40 to +85 °C	GTL16612DGG	SOT364-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional
universal translator (3-State)

GTL16612

PIN CONFIGURATION



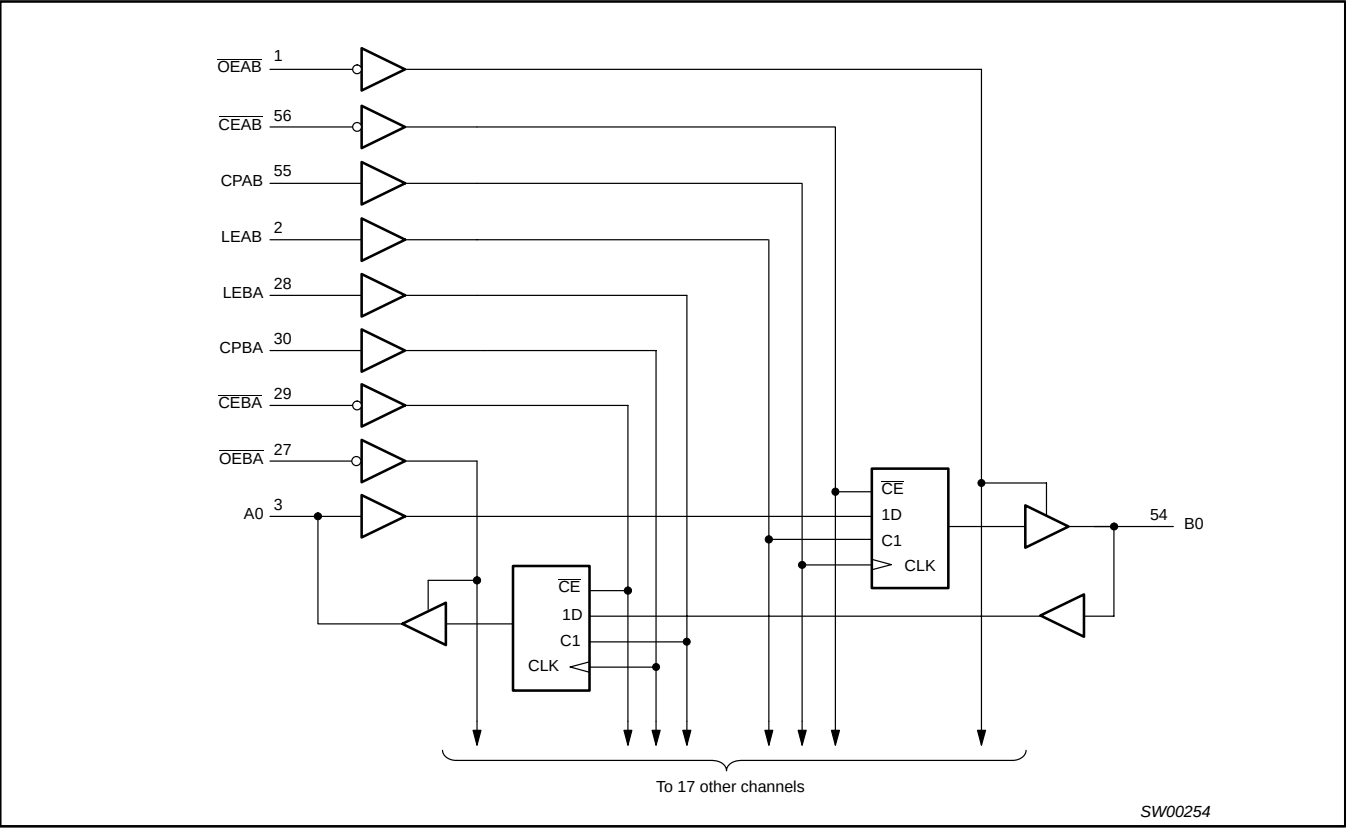
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	OEAB/OEBA	A-to-B/ B-to-A Output enable input (active Low)
29, 56	CEBA/CEAB	B-to-A/A-to-B clock enable
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22	VCC	Positive supply voltage
35	VREF	GTL reference voltage
50	NC	No connection

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

LOGIC SYMBOL (Positive Logic)



FUNCTION TABLE

INPUTS					OUTPUT B
CEAB ¹	OEAB ¹	LEAB ¹	CPAB ¹	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B _O ²
H	L	L	X	X	B _O ²
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	H	X	B _O ²
L	L	L	L	X	B _O ³

- X = Don't care
H = High voltage level
L = Low voltage level
↑ = Low to High
Z = High impedance "off" state
- A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CPBA, and CEBA.
 - Output level before the indicated steady-state input conditions were established.
 - Output level before the indicated steady-state input conditions were established, provided that CPAB was Low before LEAB went Low.

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

ABSOLUTE MAXIMUM RATINGS ^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³	A port	-0.5 to +7.0	V
		B port	-0.5 to +4.6	
I _{OK}	DC output diode current	V _O < 0; A port	-50	mA
V _O	DC output voltage ³	Output in Off or High state; A port	-0.5 to +7.0	V
		Output in Off or High state; B port	-0.5 to +4.6	V
I _{OL}	Current into any output in the LOW state	A port	128	mA
		B port	80	mA
I _{OH}	Current into any output in the HIGH state	A port	-64	mA
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	3.3 V RANGE LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage		3.0	3.6	V
V _{TT}	Termination voltage	GTL	1.14	1.26	V
		GTL ⁺	1.35	1.65	
V _{REF}	GTL reference voltage	GTL	0.74	0.87	V
		GTL ⁺	0.9	1.10	
V _I	Input voltage	B port	0	V _{TT}	V
		Except B port	0	5.5	
V _{IH}	HIGH-level input voltage	B port	V _{REF} +50 mV		V
		Except B port	2.0		
V _{IL}	LOW-level input voltage	B port		V _{REF} -50 mV	V
		Except A port		0.8	
I _{OH}	HIGH-level output current	A port		-32	mA
I _{OL}	LOW-level output current	B port		40	mA
		A port		64	
T _{amb}	Operating free-air temperature range		-40	+85	°C

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

DC ELECTRICAL CHARACTERISTICS (3.3 V $\pm$ 0.3 V RANGE)

SYMBOL	PARAMETER		TEST CONDITIONS		LIMITS			UNIT	
					Temp = -40 to +85 °C				
					MIN	TYP ¹	MAX		
V _{IK}	Input clamp voltage		V _{CC} = 3.0 V; I _{IK} = -18 mA			-0.85	-1.2	V	
V _{OH}	High-level output voltage		V _{CC} = 3.0 to 3.6 V; I _{OH} = -100 μA	A port	V _{CC} -0.2	V _{CC}		V	
			V _{CC} = 3.0 V; I _{OH} = -32 mA		2.0	2.3			
V _{OL}	Low-level output voltage		V _{CC} = 3.0 V; I _{OL} = 100 μA	A port		0.07	0.2	V	
			V _{CC} = 3.0 V; I _{OL} = 16 mA			0.25	0.4		
			V _{CC} = 3.0 V; I _{OL} = 32 mA			0.3	0.5		
			V _{CC} = 3.0 V; I _{OL} = 64 mA			0.4	0.55		
			V _{CC} = 3.0 V; I _{OL} = 40 mA	B port		0.4	0.5	V	
I _I	Input leakage current		V _{CC} = 3.6 V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA	
			V _{CC} = 0 or 3.6 V; V _I = 5.5 V			0.1	10		
			V _{CC} = 3.6 V; V _I = 5.5 V	I/O Data pins ⁴ A port		0.1	20	μA	
			V _{CC} = 3.6 V; V _I = V _{CC}			0.5	10		
			V _{CC} = 3.6 V; V _I = 0			0.1	-5		
			V _{CC} = 3.6 V; V _I = V _{TT} or GND	B port			±5	μA	
I _{OFF}	Output off current		V _{CC} = 0 V; V _I or V _O = 0 to 4.5 V			0.1	±100	μA	
I _{HOLD}	Bus Hold current, A outputs		V _{CC} = 3 V; V _I = 0.8 V		75	130		μA	
			V _{CC} = 3 V; V _I = 2.0 V		-75	-140			
I _{EX}	Current into an output in the High state when V _O > V _{CC}		V _O = 5.5 V; V _{CC} = 3.0 V	A port		10	125	μA	
I _{PU/PD}	Power up/down 3-State output current ³		V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} OE = Don't care			1.0	±100	μA	
I _{CCH}	A-Port	V _{CC} = 3.6 V	Outputs high		V _I = GND or V _{CC} , I _O = 0		5.0	9.0	mA
I _{CCL}			Outputs low				10.5	18.5	
I _{CCZ} ⁵	Disabled			6.0		11.5			
I _{CCH}	B-Port		Outputs high				9.7	17.5	
I _{CCL}			Outputs low				7.0	12.0	
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 3 V to 3.6 V; One input at V _{CC} -0.6 V, Other inputs at V _{CC} or GND			0.04	0.2	mA	

NOTES:

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each LVTTTL input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V $\pm$ 0.3 V a transition time of 100 μ sec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

AC CHARACTERISTICS (A PORT)

GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω ; $T_{amb} = -40$ to $+85$ °C.

GTL16612 An Port			GTL			GTL+			UNIT
			V _{CC} = 3.3 V ±0.3 V			V _{CC} = 3.3 V ±0.3 V			
			V _{REF} = 0.8 V			V _{REF} = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	
t _{PLH}	Bn to An	2	1.6	3.0	5.0	1.6	3.0	5.0	ns
t _{PHL}	Bn to An	2	3.0	4.9	6.3	3.0	4.9	6.3	ns
t _{PLH}	LEBA to An	3	1.6	2.7	4.2	1.6	2.7	4.2	ns
t _{PHL}	LEBA to An	3	1.6	2.8	4.3	1.6	2.8	4.3	ns
t _{PLH}	CPBA to An	1	1.9	3.4	4.7	1.9	3.4	4.7	ns
t _{PHL}	CPBA to An	1	1.8	3.8	5.2	1.8	3.8	5.2	ns
t _{PZH}	$\overline{OEBA}$ to An	5	1.5	2.6	4.2	1.5	2.6	4.2	ns
t _{PHZ}	$\overline{OEBA}$ to An	5	1.4	2.9	4.8	1.4	2.9	4.8	ns
t _{PZL}	$\overline{OEBA}$ to An	6	1.3	2.4	3.8	1.3	2.4	3.8	ns
t _{PLZ}	$\overline{OEBA}$ to An	6	1.2	2.2	3.5	1.2	2.2	3.5	ns

NOTE:

1. Typical values are at $V_{CC} = 3.3$ V, $T_{amb} = +25$ °C.

AC CHARACTERISTICS (B PORT)

GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 30$ pF; $R_L = 25$ Ω ; $T_{amb} = -40$ to $+85$ °C.

GTL16612 Bn Port			GTL			GTL+			UNIT
			V _{CC} = 3.3 V ±0.3 V			V _{CC} = 3.3 V ±0.3 V			
			V _{REF} = 0.8 V			V _{REF} = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	
t _{PLH}	An to Bn	2	1.4	2.4	3.7	1.3	2.4	3.7	ns
t _{PHL}	An to Bn	2	1.3	2.5	4.0	1.4	2.6	4.2	ns
t _{PLH}	LEAB to Bn	3	1.7	3.0	4.4	1.8	3.0	4.6	ns
t _{PHL}	LEAB to Bn	3	2.1	3.5	5.4	2.3	3.6	5.5	ns
t _{PLH}	CPAB to Bn	1	1.8	3.1	4.5	1.9	3.1	4.8	ns
t _{PHL}	CPAB to Bn	1	2.3	3.6	5.4	2.4	3.8	5.8	ns
t _{PLH}	$\overline{OEAB}$ to Bn	7	1.1	2.1	3.3	1.4	2.0	3.5	ns
t _{PHL}	$\overline{OEAB}$ to Bn	7	1.6	2.8	4.4	1.0	2.9	4.5	ns

NOTE:

1. Typical values are at $V_{CC} = 3.3$ V, $T_{amb} = +25$ °C.

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

AC SETUP REQUIREMENTS (3.3 V ±0.3 V RANGE)

A Port: GND = 0 V; Input $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω ; $T_{amb} = -40$ to $+85$ °C; $V_{REF} = 0.8$ V or 1.0 V.

B Port: GND = 0 V; Input $t_r = t_f = 2.5$ ns; $C_L = 30$ pF; $R_L = 25$ Ω ; $V_{REF} = 0.8$ V or 1.0 V.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V _{CC} = 3.3 V ±0.3 V		
			MIN	MAX	
t _s (H)	Setup time, High or Low Bn to CPBA	4	1.5		ns
t _s (L)		4	1.5		ns
t _s (H)	Setup time, High or Low An to CPAB	4	2.0		ns
t _s (L)		4	3.0		ns
t _h (H)	Hold time, High or Low Bn to CPBA, or An to CPAB	4	1.0		ns
t _h (L)		4	1.0		ns
t _s (H)	Setup time, High or Low Bn to LEBA, or An to LEAB	4	1.0		ns
t _s (L)		4	1.0		ns
t _h (H)	Hold time, High or Low Bn to LEBA, or An to LEAB	4	1.5		ns
t _h (L)		4	1.5		ns
t _s (H)	Setup time, High or Low CEAB to CPAB, or CEBA to CPBA	4	1.0		ns
t _s (L)		4	1.0		ns
t _h (H)	Hold time, High or Low CEAB to CPAB, or CEBA to CPBA	4	1.5		ns
t _h (L)		4	1.0		ns
t _w (H)	Pulse width, High or Low CPBA or CPAB	4	2.0		ns
t _w (L)		4	2.0		ns
t _w (H)	Pulse width, High LEBA or LEAB	3	1.5		ns

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

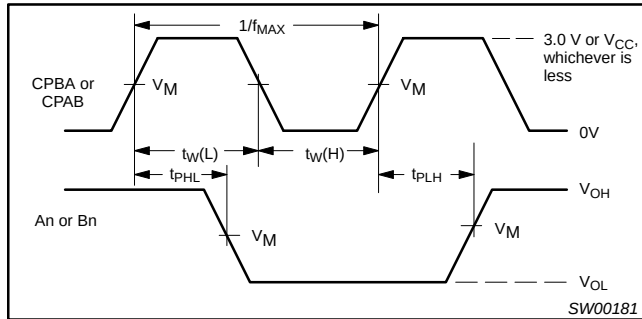
GTL16612

AC WAVEFORMS

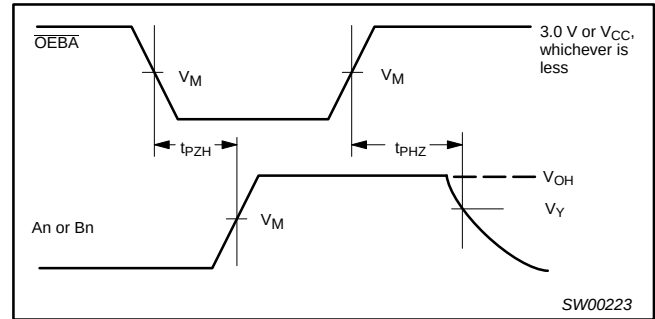
$V_M = 1.5\text{ V}$ at $V_{CC} \geq 3.0\text{ V}$. $V_M = 1.5\text{ V}$ for A ports and control pins; $V_M = 0.8\text{ V}$ for B ports in GTL mode; $V_M = 1.0\text{ V}$ for B ports in GTL+ mode.

$V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 3.0\text{ V}$.

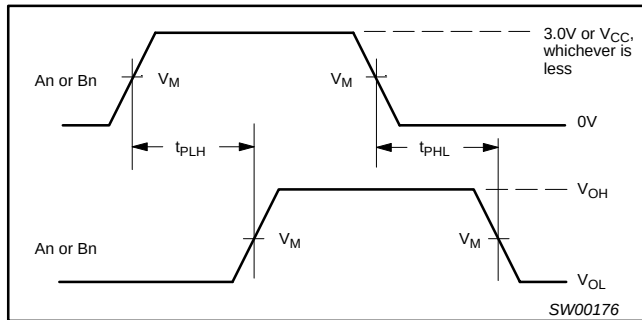
$V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CC} \geq 3.0\text{ V}$.



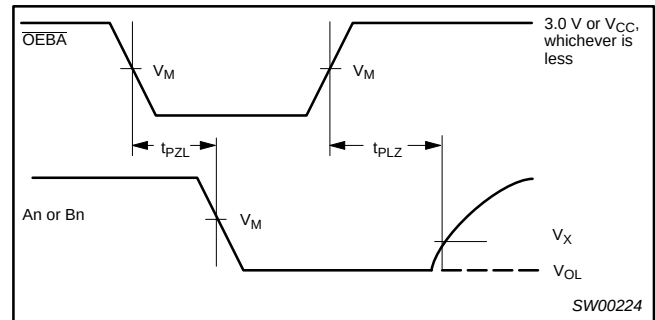
Waveform 1. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



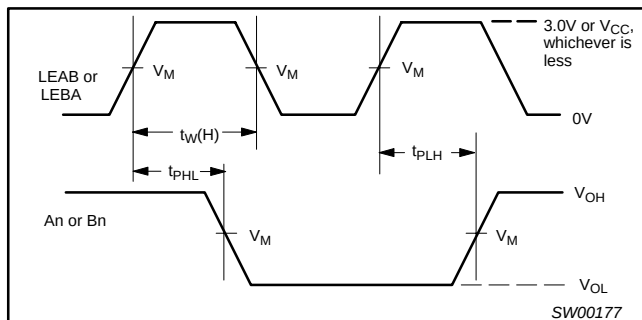
Waveform 5. 3-State output enable time to high level and output disable time from high level



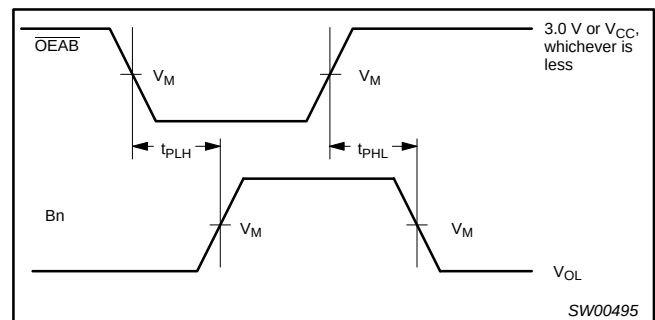
Waveform 2. Propagation delay, transparent mode



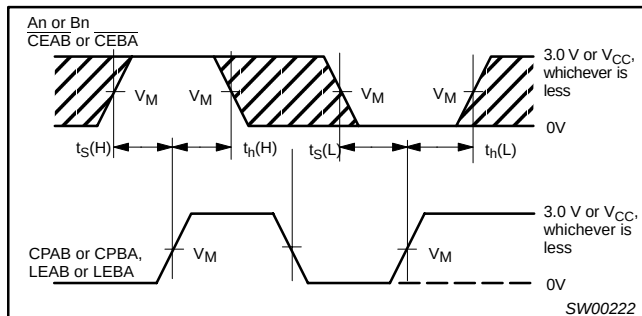
Waveform 6. 3-State output enable time to low level and output disable time from low level



Waveform 3. Propagation delay, enable to output, and enable pulse width



Waveform 7. Output enable time on open collector output with pullup

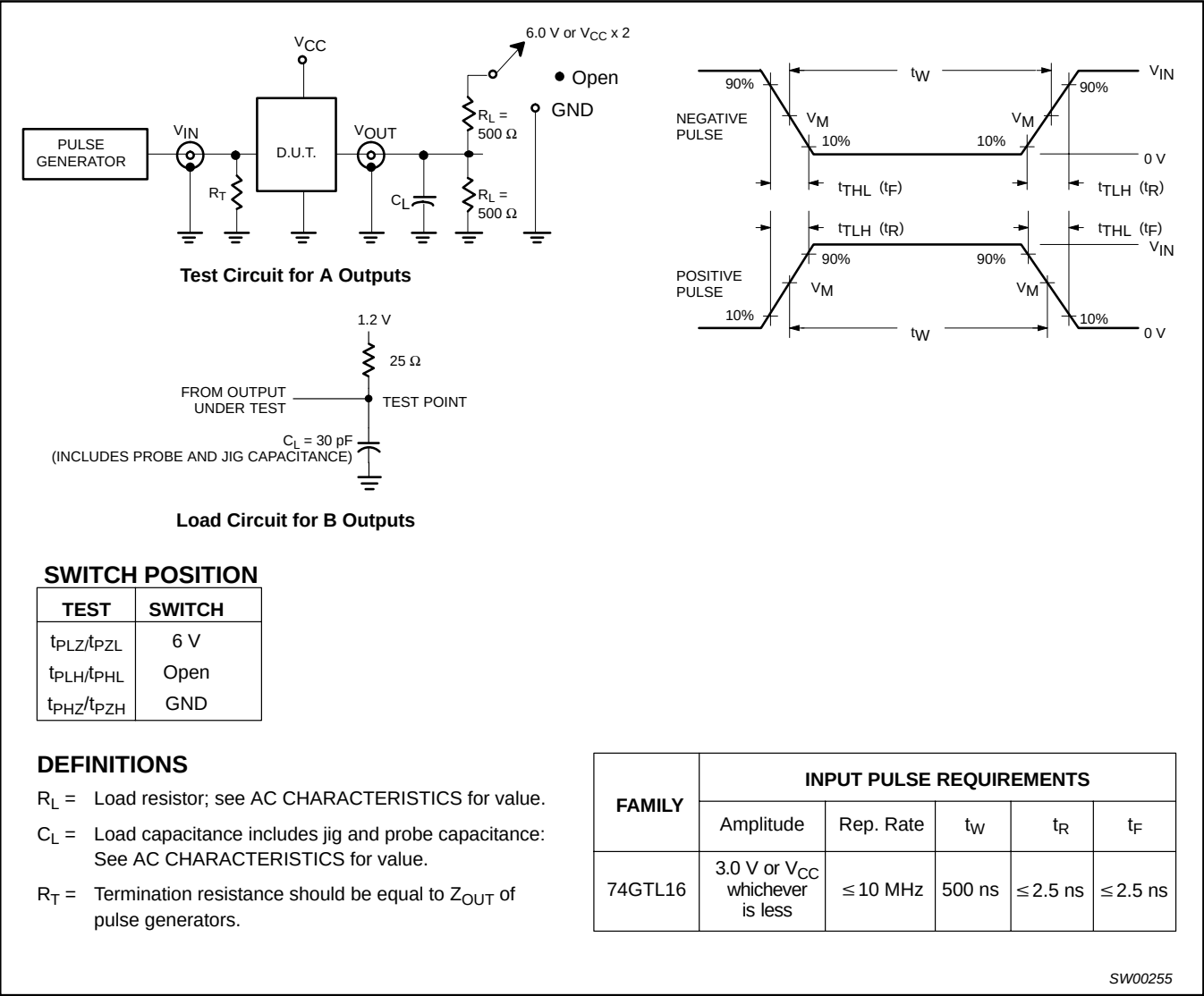


Waveform 4. Data setup and hold times

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

TEST CIRCUIT

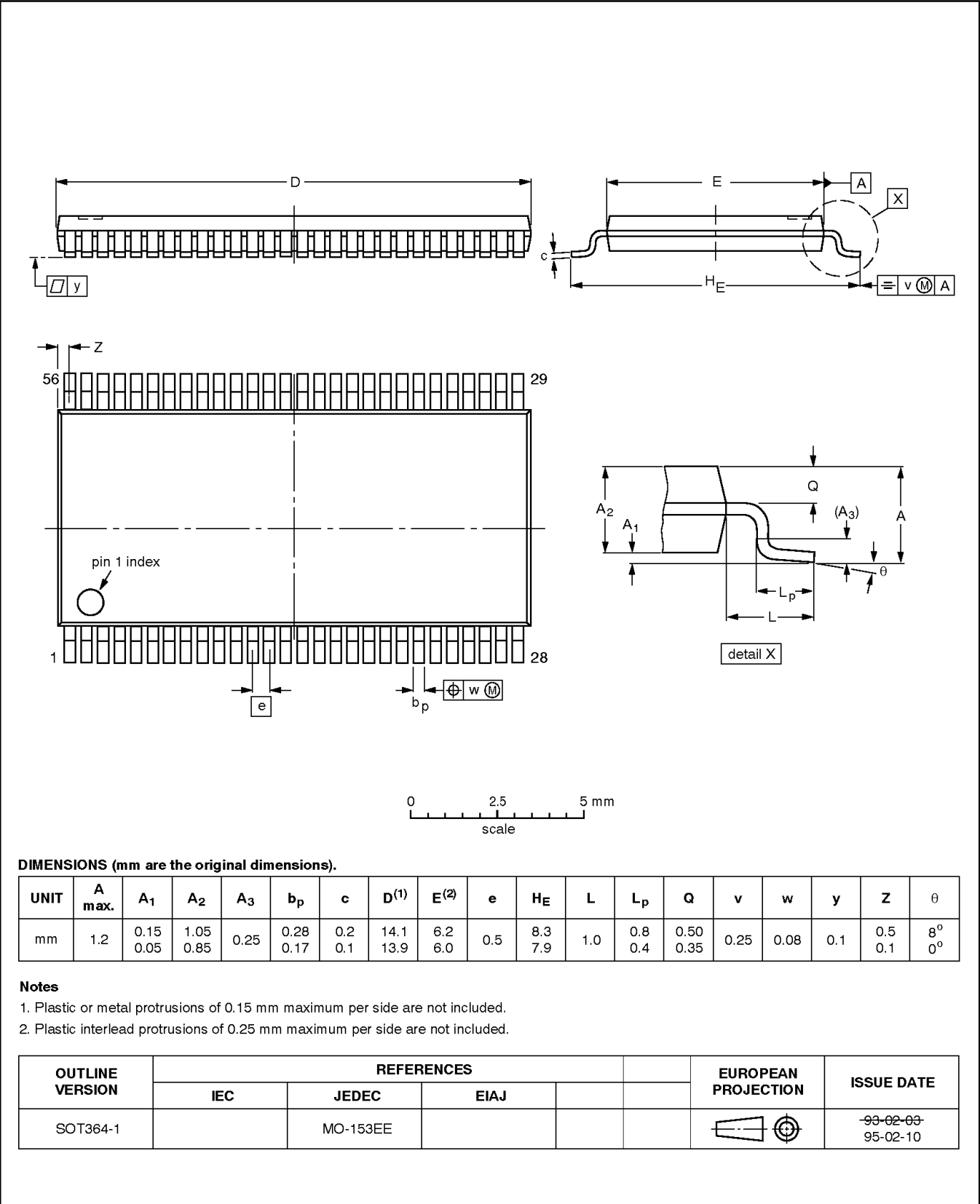


18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



**18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional
universal translator (3-State)**

GTL16612**REVISION HISTORY**

Rev	Date	Description
_4	20021213	Product data (9397 750 10862); ECN 853-2166 29245 of 03 December 2002 Modifications: • New package release.
_3	20000619	Product data (9397 750 07217); ECN 853-2166 23903 of 19 June 2000.

18-bit GTL/GTL⁺ to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit

<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to:

sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2002
All rights reserved. Printed in U.S.A.

Date of release: 12-02

Document order number:

9397 750 10862

Let's make things better.