

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC00FN

Quad 2-Input NAND Gate

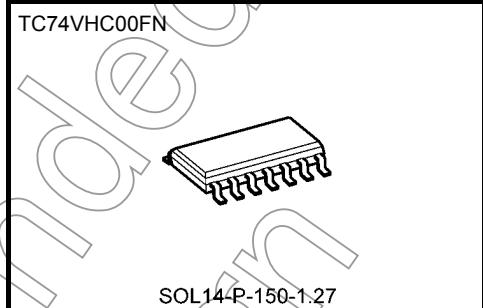
The TC74VHC00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Note: xxxFN (JEDEC SOP) is not available in Japan.



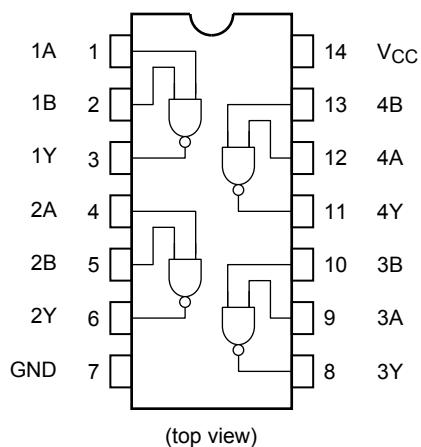
Weight
SOL14-P-150-1.27 : 0.12 g (typ.)

Features

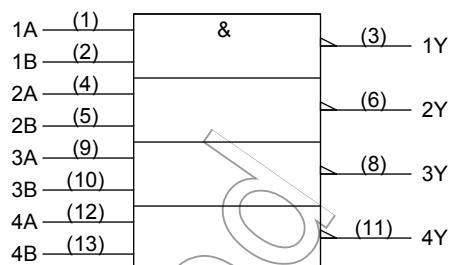
- High speed: $t_{pd} = 3.7$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 2 \mu A$ (max) at $T_a = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC} (\text{opr}) = 2$ to 5.5 V
- Low noise: $VO_{LP} = 0.8$ V (max)
- Pin and function compatible with 74ALS00

NOT FOR NEW DESIGN

Pin Assignment



IEC Logic Symbol



Truth Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{STG}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		$T_a = 25^\circ\text{C}$			$T_a = 40$ to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—	2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V
Low-level input voltage	V_{IL}	—	2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
Input leakage current	I_{IN}	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	—	± 0.1	— ± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	2.0	— 20.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit	
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time	t_{PLH}	—	3.3 ± 0.3	15	—	5.5	7.9	1.0	9.5	ns	
				50	—	8.0	11.4	1.0	13.0		
	t_{PHL}	—	5.0 ± 0.5	15	—	3.7	5.5	1.0	6.5		
				50	—	5.2	7.5	1.0	8.5		
Input capacitance	C_{IN}	—			—	4	10	—	10	pF	
Power dissipation capacitance	C_{PD}	(Note)			—	19	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

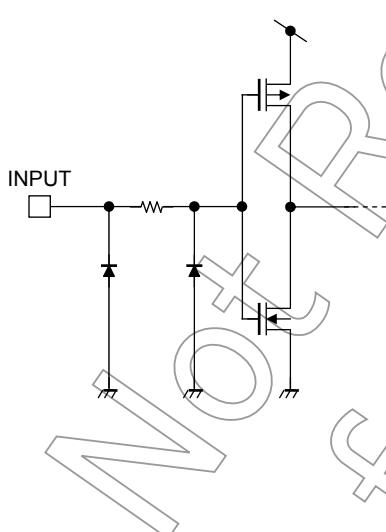
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			$T_a = 25^\circ\text{C}$		Unit
			V_{CC} (V)	Typ.	Limit		
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	5.0	0.3	0.8	V	
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	5.0	-0.3	-0.8	V	
Minimum high level dynamic input voltage	V_{IHD}	$C_L = 50$ pF	5.0	—	3.5	V	
Maximum low level dynamic input voltage	V_{ILD}	$C_L = 50$ pF	5.0	—	1.5	V	

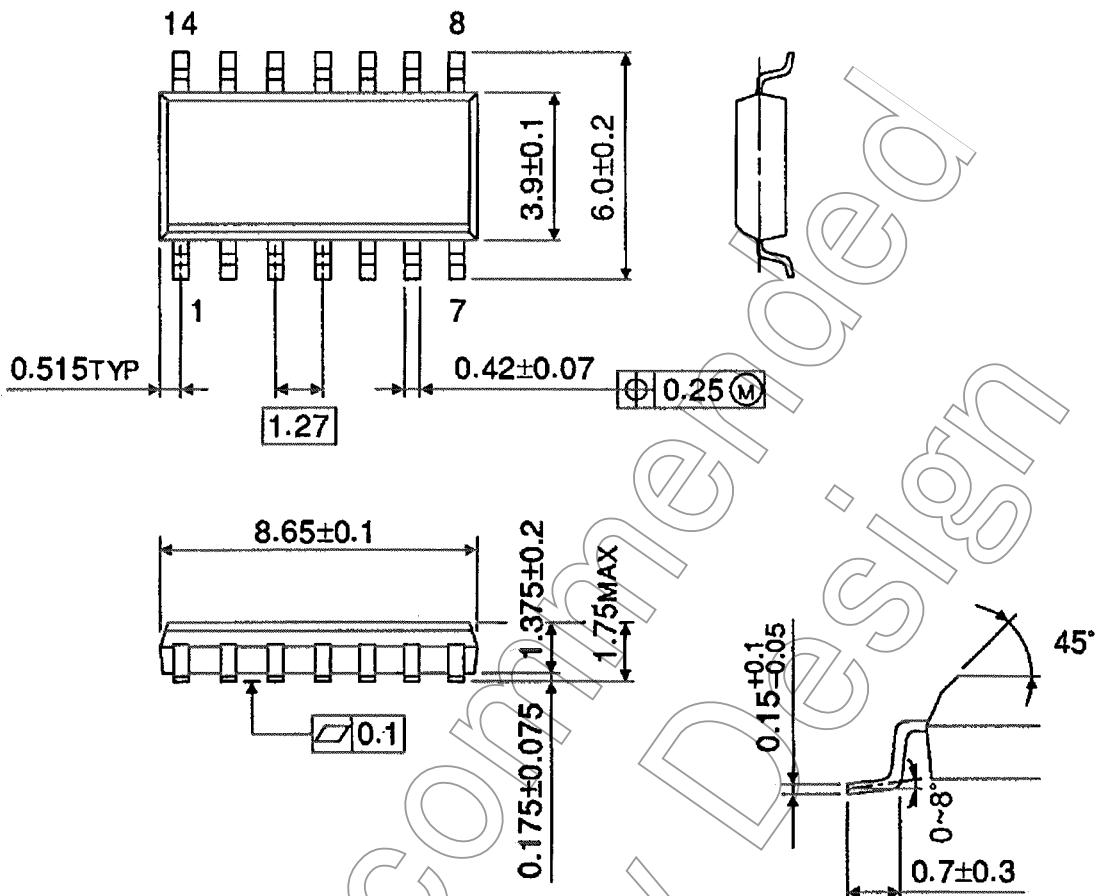
Input Equivalent Circuit



Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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