



CYPRESS

CY7C372

UltraLogic™ 64-Macrocell Flash CPLD

Features

- 64 macrocells in four logic blocks
- 32 I/O pins
- 6 dedicated inputs including 2 clock pins
- No hidden delays
- High speed
 - MAX = 125 MHz
 - PD = 10 ns
 - t_S = 5.5 ns
 - t_{CO} = 6.5 ns
- Electrically alterable Flash technology
- Available in 44-pin PLCC and CLCC packages
- Pin compatible with the CY7C371

Functional Description

The CY7C372 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370t family of high-density, high-speed CPLDs. Like all members of the

FLASH370 family, the CY7C372 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

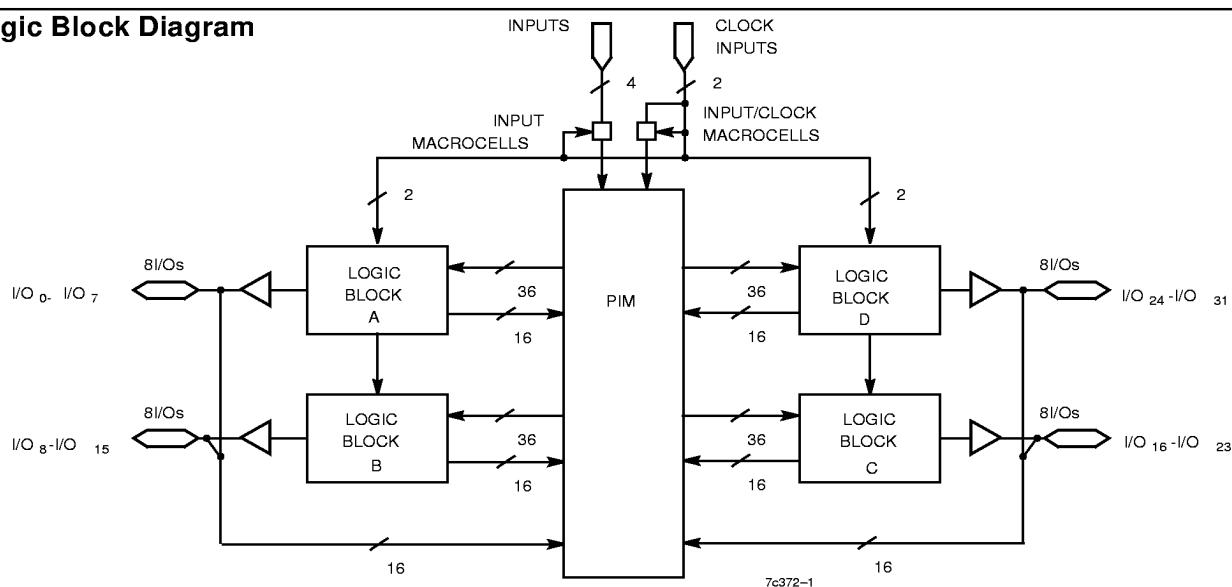
The 64 macrocells in the CY7C372 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C372 is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 32 I/O pins on the CY7C372. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C372 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used, or the type of application, the timing parameters on the CY7C372 remain the same.

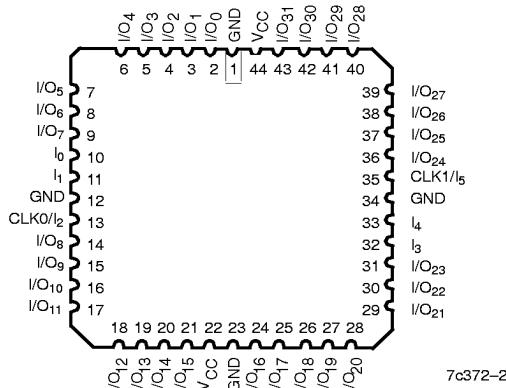
Logic Block Diagram



Selection Guide

	7C372-125	7C372-100	7C372-83	7C372-66	7C372L-66
Maximum Propagation Delay, t_{PD} (ns)	10	12	15	20	20
Minimum Set-up, t_S (ns)	5.5	6	8	10	10
Maximum Clock to Output, t_{CO} (ns)	6.5	6.5	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial Military/Industrial	280 250	250 300	250 300	125 125

Pin Configuration



Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C372 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C372 have separate I/O pins associated with them. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The I/O macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C372 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C372 is available from Cypress's *Warp2*TM and *Warp3*TM software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABELTM, CUPLTM, and LOG/ICTM. Please refer to third-party tool support data sheets for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Program Voltage	12.5V
Output Current into Outputs	16 mA
Static Discharge Voltage	>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V \pm 5%
Industrial	-40°C to +85°C	5V \pm 10%
Military ^[1]	-55°C to +125°C	5V \pm 10%

Notes:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit		
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -3.2 \text{ mA (Com'l/Ind)}$	2.4		V		
			$I_{OH} = -2.0 \text{ mA (Mil)}$			V		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 16 \text{ mA (Com'l/Ind)}$		0.5	V		
			$I_{OL} = 12 \text{ mA (Mil)}$			V		
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs ^[3]			2.0	7.0	V	
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs ^[3]			-0.5	0.8	V	
I_{IX}	Input Load Current	$V_I = \text{Internal GND}, V_I = V_{CC}$			-10	+10	μA	
I_{OZ}	Output Leakage Current	$V_o = \text{Internal GND}, V_o = V_{CC}$			-50	+50	μA	
I_{OS}	Output Short Circuit Current ^[4, 5]	$V_{CC} = \text{Max.}, V_{OUT} = 0.5\text{V}$			-30	-160	mA	
I_{CC}	Power Supply Current ^[6]	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = 1 \text{ mHz}, V_{IN} = \text{GND}, V_{CC}$	Com'l		250	mA		
			Com'l "L" -66		125	mA		
			Com'l -125		280	mA		
			Mil/Industrial		300	mA		

Shaded area contains preliminary information.

Capacitance^[5]

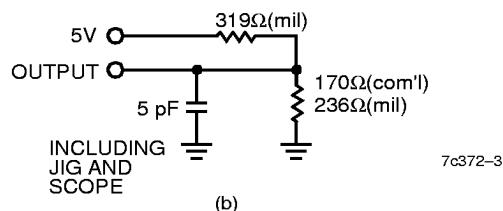
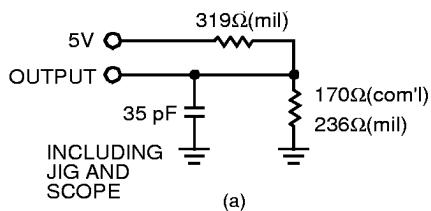
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 5.0\text{V}$ at $f=1 \text{ MHz}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 5.0\text{V}$ at $f = 1 \text{ MHz}$	12	pF

Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. $V_{OUT} = 0.5\text{V}$ has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Measured with 16-bit counter programmed into each logic block.

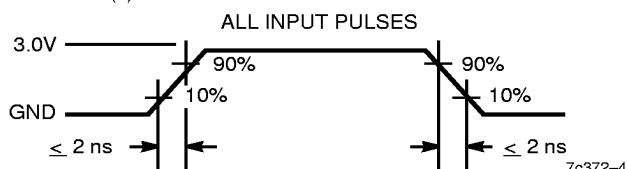
AC Test Loads and Waveforms


7c372-3

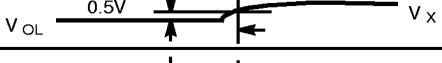
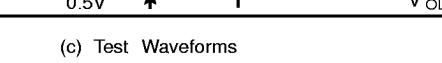
Equivalent to: THÉVENIN EQUIVALENT

99Ω(com'l)
136Ω(mil)
2.08V(com'l)
2.13V(mil)

OUTPUT



7c372-4

Parameter [7]	V_x	Output Waveform Measurement Level
$t_{ER} (-)$	1.5V	
$t_{ER} (+)$	2.6V	
$t_{EA} (+)$	1.5V	
$t_{EA} (-)$	V_{thc}	

(c) Test Waveforms

Switching Characteristics Over the Operating Range^[8]

Parameter	Description	7C372-125		7C372-100		7C372-83		7C372-66		Unit	
		7C372-125		7C372-100		7C372-83		7C372L-66			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Combinatorial Mode Parameters											
t_{PD}	Input to Combinatorial Output			10		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch			13		15		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches			15		16		19		24	ns
t_{EA}	Input to Output Enable			14		16		19		24	ns
t_{ER}	Input to Output Disable			14		16		19		24	ns
Input Registered/Latched Mode Parameters											
t_{WL}	Clock or Latch Enable Input LOW Time ^[5]	3		3		4		5		ns	
t_{WH}	Clock or Latch Enable Input HIGH Time ^[5]	3		3		4		5		ns	
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns	
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns	
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output			14		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch			16		18		21		26	ns

Shaded area contains preliminary information.

Notes:

- t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
- All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[8]

Parameter	Description	7C372-125		7C372-100		7C372-83		7C372-66		Unit	
		7C372-125		7C372-100		7C372-83		7C372L-66			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output Registered/Latched Mode Parameters											
t _{CO}	Clock or Latch Enable to Output		6.5		6.5		8		10	ns	
t _S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns	
t _H	Register or Latch Data Hold Time	0		0		0		0		ns	
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		14		16		19		24	ns	
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns	
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns	
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns	
f _{MAX1}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[5]	125		100		83		66		MHz	
f _{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) ^[5]	153.8		153.8		125		100		MHz	
f _{MAX3}	Maximum Frequency with External Feedback (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH})) ^[5]	83.3		80		62.5		50		MHz	
t _{OH-t_{IH}} 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x ^[9]	0		0		0		0		ns	
Pipelined Mode Parameters											
t _{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns	
f _{MAX4}	Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}), or 1/t _{SCS}) ^[5]	125		100		83.3		66.6		MHz	
Reset/Preset Parameters											
t _{RW}	Asynchronous Reset Width ^[5]	10		12		15		20		ns	
t _{RR}	Asynchronous Reset Recovery Time ^[5]	12		14		17		22		ns	
t _{RO}	Asynchronous Reset to Output		16		18		21		26	ns	
t _{PW}	Asynchronous Preset Width ^[5]	10		12		15		20		ns	
t _{PR}	Asynchronous Preset Recovery Time ^[5]	12		14		17		22		ns	
t _{PO}	Asynchronous Preset to Output		16		18		21		26	ns	
t _{POR}	Power-On Reset ^[5]		1		1		1		1	μs	

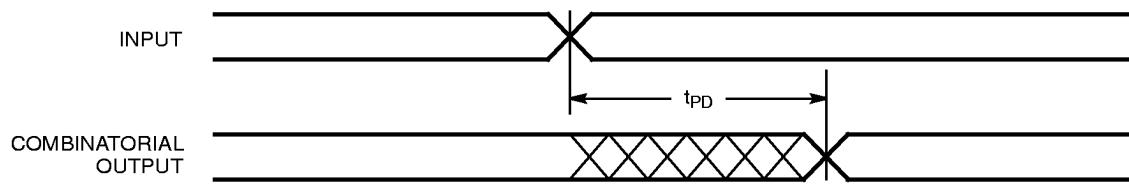
Shaded area contains preliminary information.

Notes:

9. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C372. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

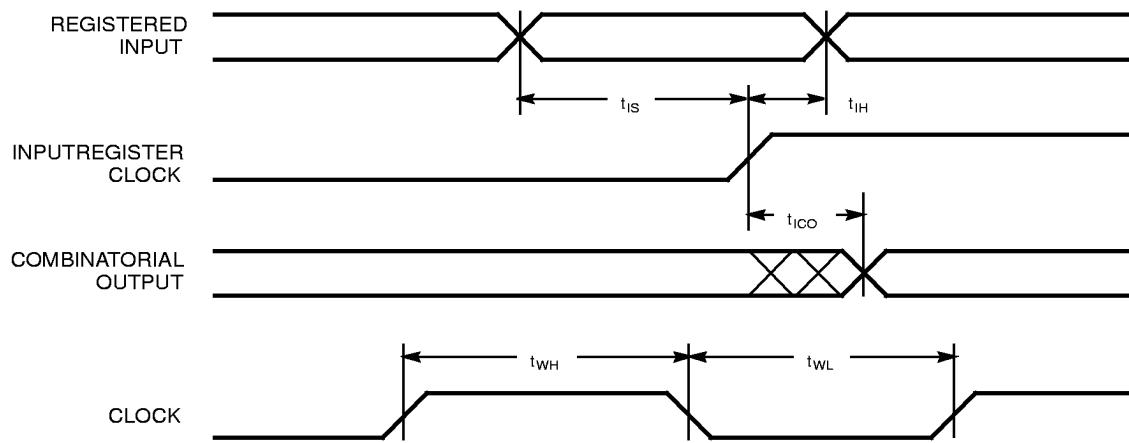
Switching Waveforms

CombinatorialOutput



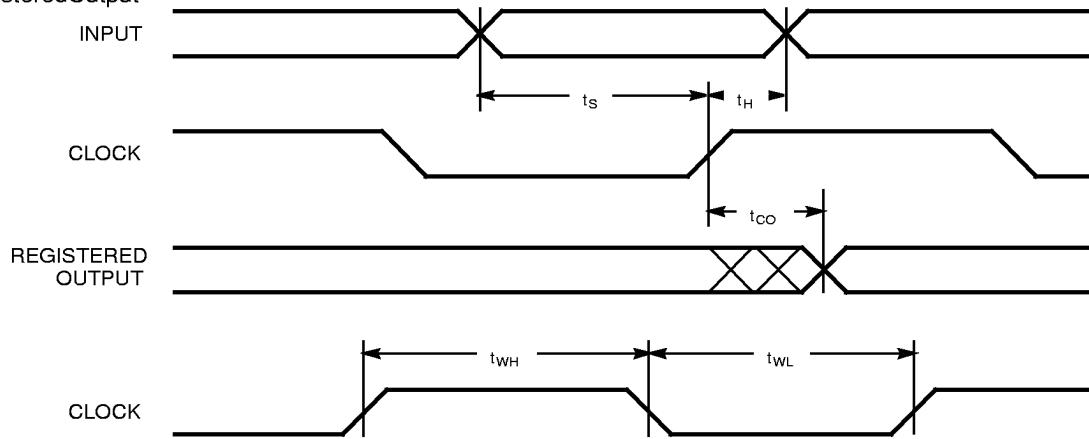
7c372-5

Registered Input

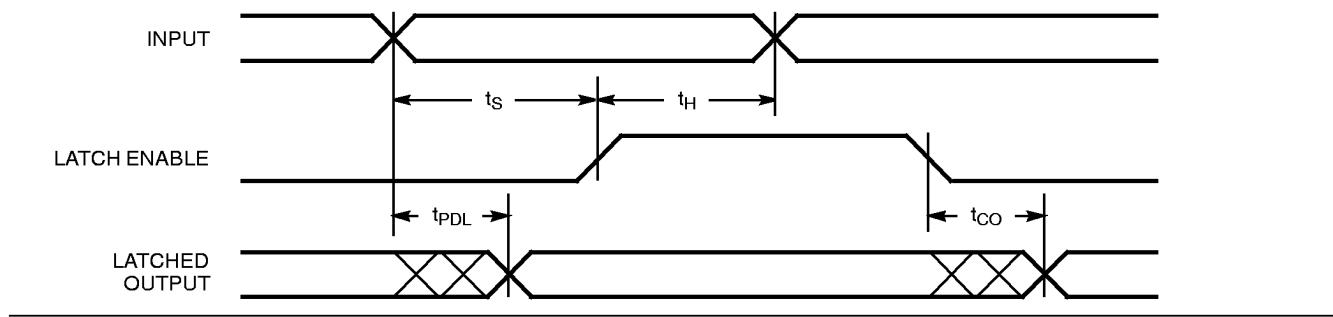
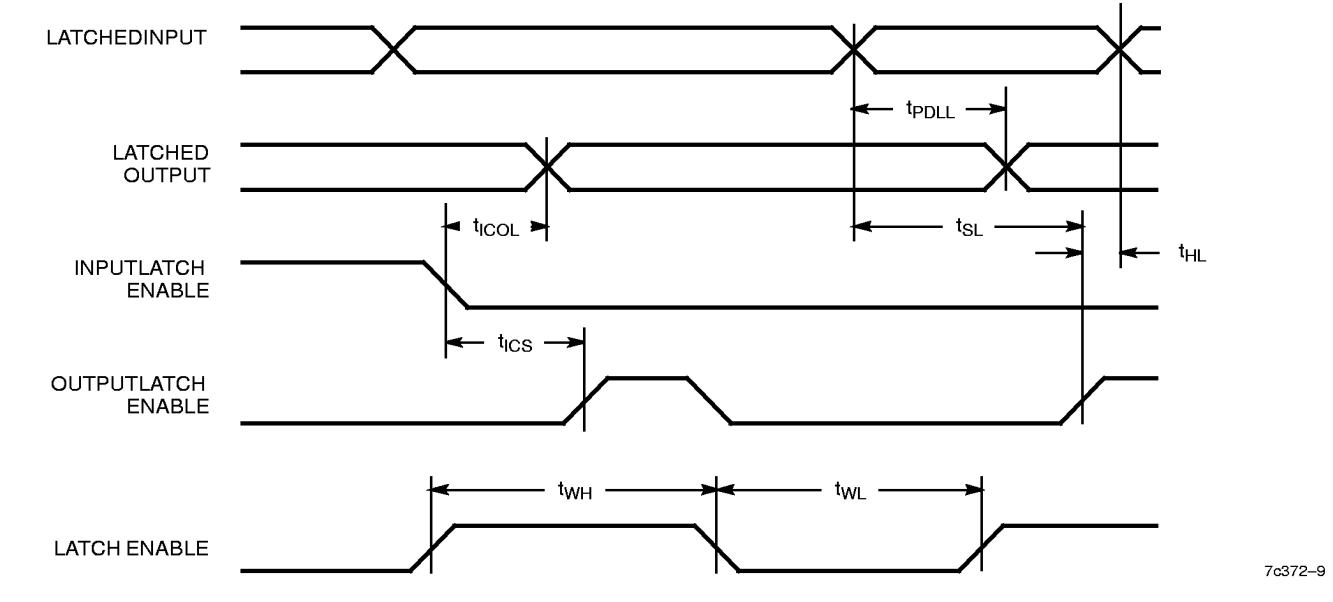


7c372-6

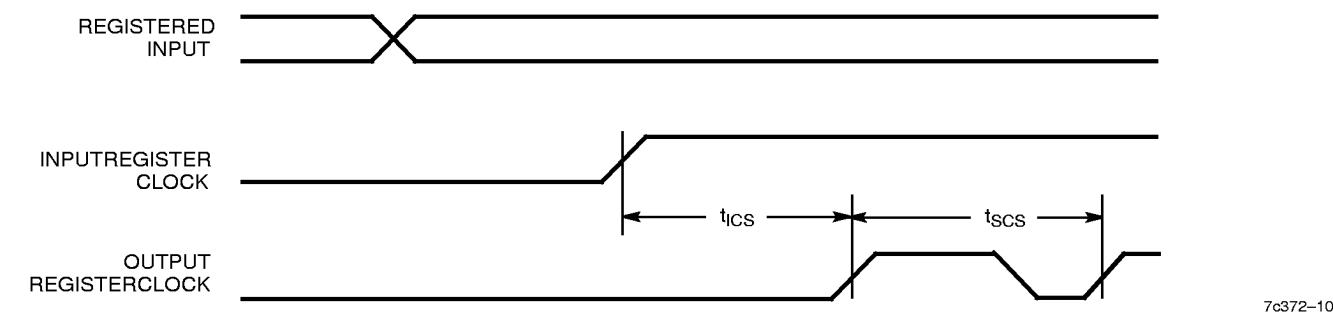
RegisteredOutput



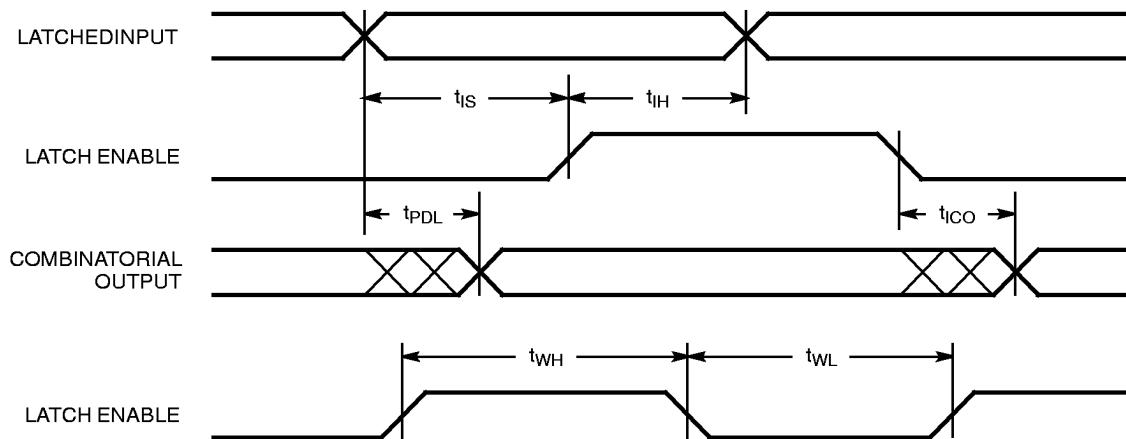
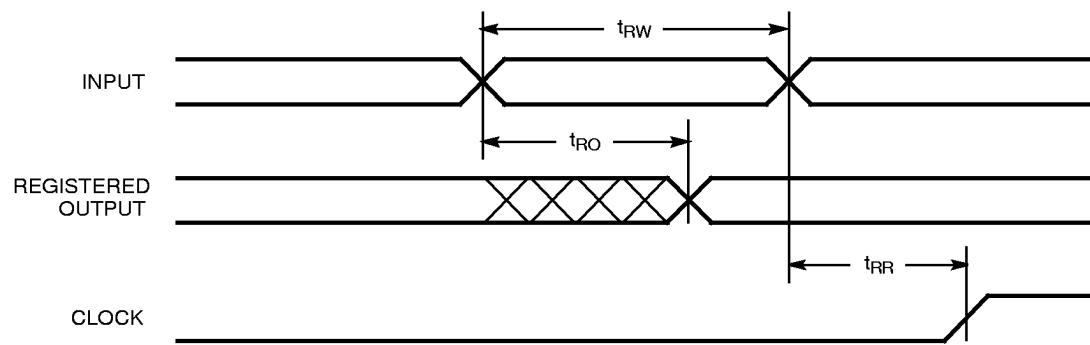
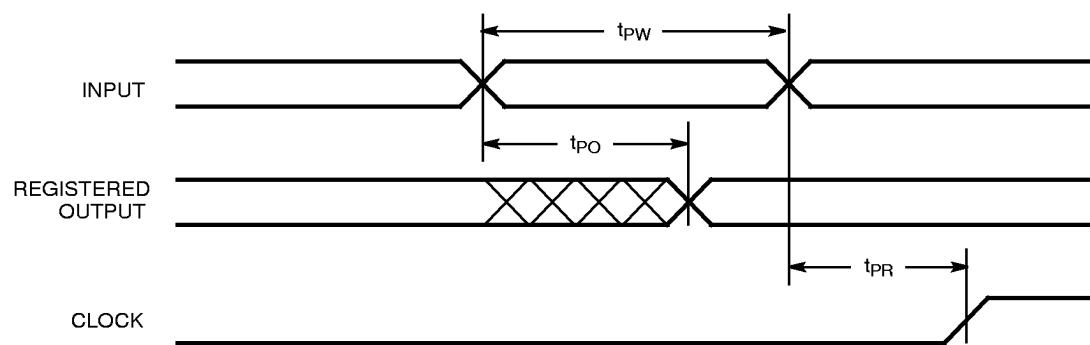
7c372-7

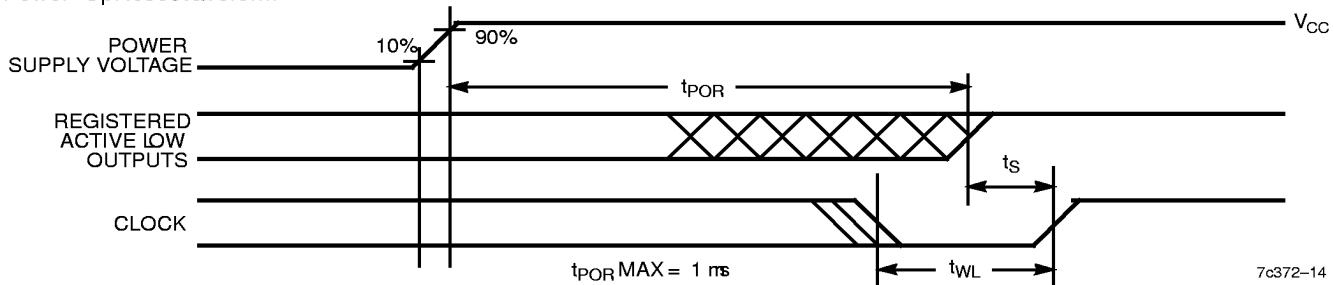
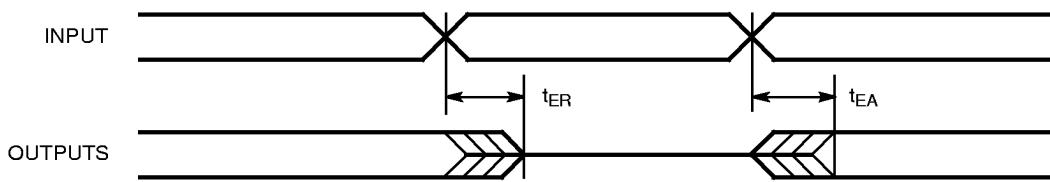
Switching Waveforms (Continued)
Latched Output

Latched Input and Output


7c372-9

Clock to Clock


7c372-10

Switching Waveforms (Continued)
LatchedInput

AsynchronousReset

AsynchronousPreset


Switching Waveforms (Continued)
Power-Up Reset Waveform

Output Enable/Disable

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C372-125JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
100	CY7C372-100JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
83	CY7C372-83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372-83JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C372-83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C372-66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372-66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
	CY7C372-66JI	J67	44-Lead Ceramic Leaded Chip Carrier	Industrial
	CY7C372L-66JC	J67	44-Lead Ceramic Leaded Chip Carrier	Commercial

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

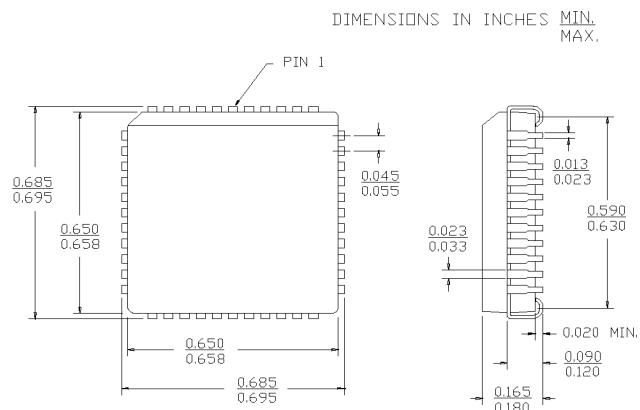
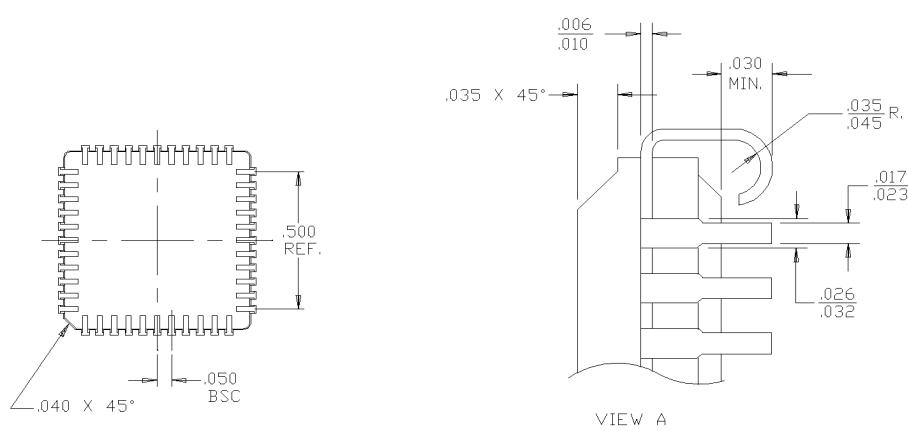
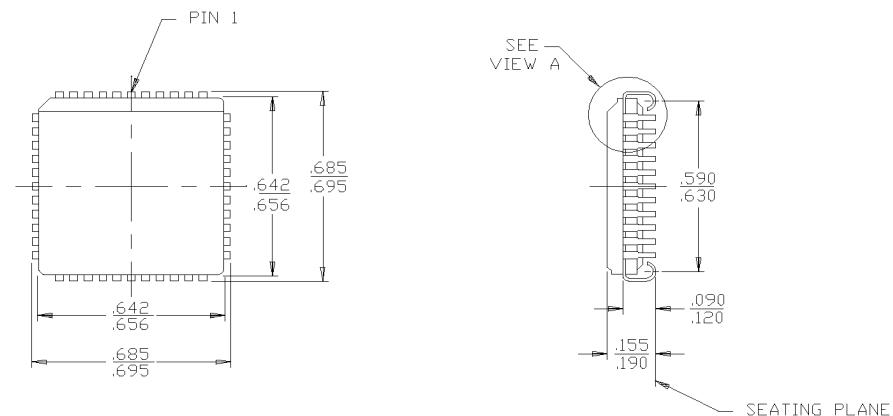
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

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Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_s	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

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LOG/IC is a trademark of Isdata Corporation.
CUPL is a trademark of Logical Devices Incorporated.*

Package Diagrams
44-Lead Plastic Leaded Chip Carrier J67

44-Pin Ceramic Leaded Chip Carrier Y67


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