Advance Information

PowerPC 740™ and Power PC 750™ Embedded Microprocessor: Hardware Specifications

The PowerPC 740 ™ and PowerPC 750 ™ microprocessors are implementations of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. In this document, the term “PPC750” is used as an abbreviation for the phrase “PowerPC 750™ microprocessor”, and the term “PPC740” is used as an abbreviation for the phrase “PowerPC 740™ microprocessor.” This document contains pertinent physical characteristics of the PPC740 and PPC750.

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1.0 Overview

The PPC740 and PPC750 are targeted for high performance, low power systems and support the following power management features - doze, nap, sleep, and dynamic power management. The PPC750 consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus. The PPC740 is the same design as the PPC750, except that the L2 interface pins are not brought out on the package. The PPC740 is meant to be run in applications that do not require an L2.

Figure 1 shows a block diagram of the PPC740 and PPC750.

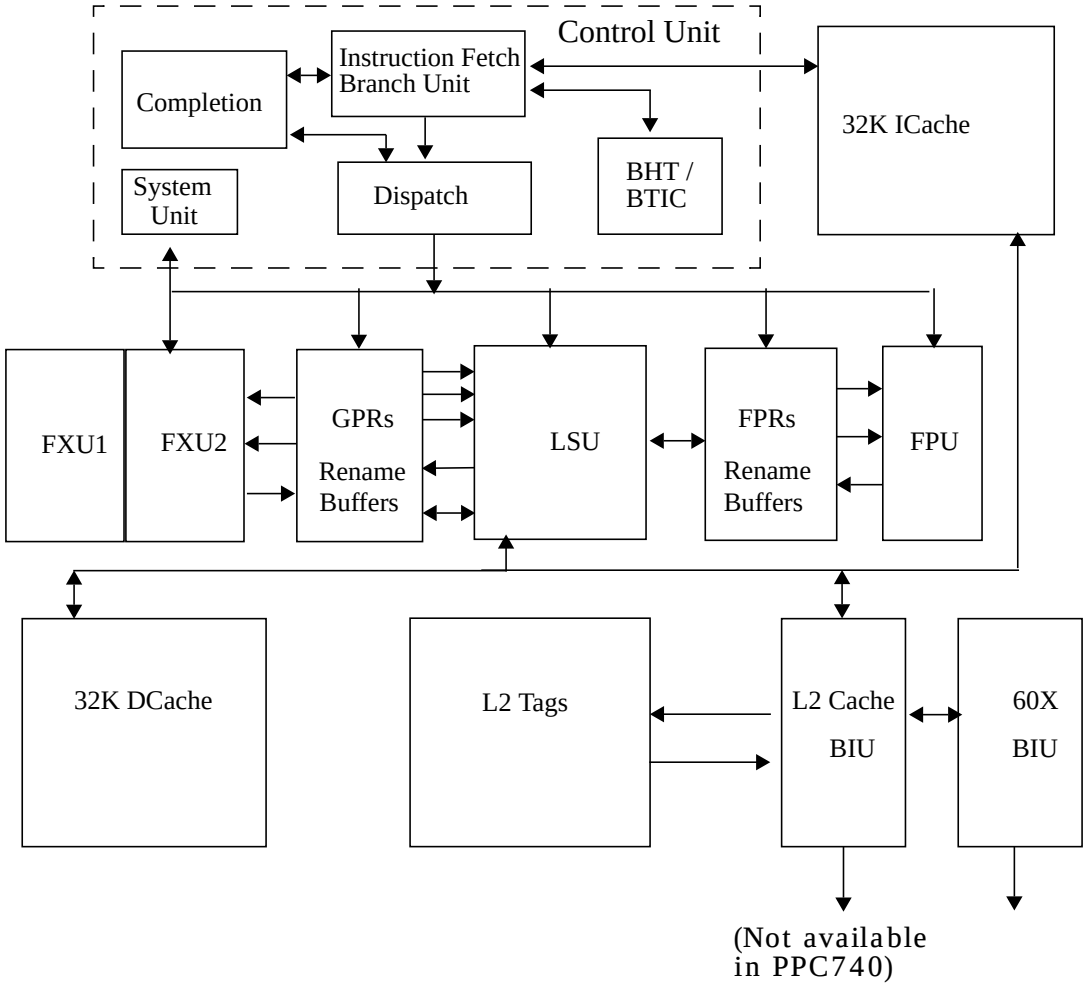


Figure 1. PPC740 and PPC750 Block Diagram

2.0 Features

This section summarizes features of the PPC740's and PPC750's implementation of the PowerPC architecture. Major features are as follows:

- Branch processing unit
  - -- Four instructions fetched per clock
  - -- One branch processed per cycle (plus resolving 2 speculations)
  - -- Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - -- 512-entry branch history table (BHT) for dynamic prediction
  - -- 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - -- Full hardware detection of dependencies (resolved in the execution units)
  - -- Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - -- Serialization control (predispose, post dispatch, execution, serialization)
- Decode
  - -- Register file access
  - -- Forwarding control
  - -- Partial instruction decode
- Load/store unit
  - -- One cycle load or store cache access (byte, half-word, word, double-word)
  - -- Effective address generation
  - -- Hits under misses (one outstanding miss)
  - -- Single-cycle misaligned access within double word boundary
  - -- Alignment, zero padding, sign extend for integer register file
  - -- Floating-point internal format conversion (alignment, normalization)
  - -- Sequencing for load/store multiples and string operations
  - -- Store gathering
  - -- Cache and TLB instructions
  - -- Big- and little-endian byte addressing supported
  - -- Misaligned little-endian support in hardware
- Fixed-point units
  - -- Fixed-point unit 1 (FXU1); multiply, divide, shift, rotate, arithmetic, logical
  - -- Fixed-point unit 2 (FXU2); shift, rotate, arithmetic, logical
  - -- Single-cycle arithmetic, shift, rotate, logical
  - -- Multiply and divide support (multi-cycle)
  - -- Early out multiply
- Floating-point unit
  - -- Support for IEEE-754 standard single- and double-precision floating-point

arithmetic

-- 3 cycle latency, 1 cycle throughput, single-precision multiply-add

-- 3 cycle latency, 1 cycle throughput, double-precision add

-- 4 cycle latency, 2 cycle throughput, double-precision multiply-add

-- Hardware support for divide

-- Hardware support for denormalized numbers

-- Time deterministic non-IEEE mode

•· System unit

-- Executes CR logical instructions and miscellaneous system instructions

-- Special register transfer instructions

•· Cache structure

-- 32K, 32-byte line, 8-way set associative instruction cache

-- 32K, 32-byte line, 8-way set associative data cache

-- Single-cycle cache access

-- Pseudo-LRU replacement

-- Copy-back or write-through data cache (on a page per page basis)

-- Supports all PowerPC memory coherency modes

-- Non-blocking instruction and data cache (one outstanding miss under hits)

-- No snooping of instruction cache

•· Memory management unit

-- 128 entry, 2-way set associative instruction TLB

-- 128 entry, 2-way set associative data TLB

-- Hardware reload for TLB's

-- 4 instruction BAT's and 4 data BATs

-- Virtual memory support for up to 4 exabytes (2^{52}) virtual memory

-- Real memory support for up to 4 gigabytes (2^{32}) of physical memory

•· Level 2 (L2) cache interface (not included on the PPC740)

-- Internal L2 cache controller and 4K-entry tags; external data SRAMs

-- 256K, 512K, and 1 Mbyte 2-way set associative L2 cache support

-- Copy-back or write-through data cache (on a page basis, or for all L2)

-- 64-byte(256K/512K) and 128-byte (l-Mbyte) sectored line size

-- Supports flow-through (reg-buf) synchronous burst SRAMs, pipelined (reg-reg) synchronous burst SRAMs, and pipelined (reg-reg) late-write synchronous burst SRAMs

-- Design supports Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3.

However, this specification supports the L2 frequency range specified in Section 3.1.2.4, “L2 Clock AC Specifications“. For higher L2 frequencies not supported in this document, please contact your IBM marketing representative.

•· Bus interface

-- Compatible with 60x processor interface

-- 32-bit address bus
-- 64-bit data bus
-- Bus-to-core frequency multipliers of 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x,7.5x, and 8x supported

•· Integrated power management
-- Low-power 2.6/3.3-volt design
-- Three static power saving modes: doze, nap, and sleep
-- Automatic dynamic power reduction when internal functional units are idle

•· Integrated Thermal Management Assist Unit
-- On-chip thermal sensor and control logic
-- Thermal Management Interrupt for software regulation of junction temperature

•· Testability
-- LSSD scan design
-- JTAG interface

•· Reliability and serviceability--Parity checking on 60x and L2 cache buses

3.0 General Parameters

The following list provides a summary of the general parameters of the PPC740 and PPC750:

Technology	0.25 µm CMOS, five-layer metal
Die Size	7.56 mm x 8.79 mm (67 mm^2)
Transistor count	6.35 million
Logic design	Fully-static
Packages	PPC740: Surface mount 255-lead ceramic ball grid array (CBGA) without L2 interface.
	PPC750: Surface mount 360-lead ceramic ball grid array (CBGA) with L2 interface.
Core power supply	2.6 ± 100mV dc
I/O power supply	3.3 V ± 5% V dc

3.1 Electrical and Thermal Characteristics

This section provides both AC and DC electrical specifications and thermal characteristics for the PPC740 and PPC750.

3.1.1 DC Electrical Characteristics

The tables in this section describe the PPC740's and PPC750's DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	-0.3 to 2.75	V
PLL supply voltage	AVdd	-0.3 to 2.75	V
L2 DLL supply voltage	L2AVdd	-0.3 to 2.75	V
60x bus supply voltage	OVdd	-0.3 to 3.6	V
L2 bus supply voltage	L2OVdd	-0.3 to 3.6	V
Input voltage	V_{in}	-0.3 to 3.6	V
Storage temperature range	T_{stg}	-55 to 150	°C

Notes:

1. Functional and tested operating conditions are given in Table 2 . Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Vin must not exceed OVdd by more than 0.3V at any time, including during power-on reset.
3. **Caution:** OVdd must not exceed Vdd/AVdd by more than 1.2V at any time, including during power-on reset.
4. **Caution:** Vdd/AVdd must not exceed OVdd by more than 0.4V at any time, including during power-on reset.

Table 2 provides the recommended operating conditions for the PPC740 and PPC750.

Table 2. Recommended Operating Conditions

Note: These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Value		Unit
		166/200 MHz	233/266 MHz	
Core supply voltage[1]	Vdd	2.5 ± 5%	2.5 to 2.7	V
PLL supply voltage	AVdd	2.5 ± 5%	2.5 to 2.7	V
L2 DLL supply voltage	L2AVdd	2.5 ± 5%	2.5 to 2.7	V
60x bus supply voltage	OVdd	3.135 to 3.465		V
L2 bus supply voltage	L2OVdd	3.135 to 3.465		V
Input voltage	V_{in}	GND to OVdd		V
Die-junction temperature[1]	Tj	0 to 105		°C

Note:
1. Default values for these characteristics can be overridden by values specified by the application conditions digit of the part number (see Section 8.0, "Ordering Information").

Table 3 provides the package thermal characteristics for the PPC740 and PPC750.

Table 3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.03	°C/W
CBGA package thermal resistance, junction-to-lead thermal resistance (typical)	θ_{JB}	3.8	°C/W

Note: Refer to Section 7.7, “Thermal Management Information“ for more information about thermal management

The PPC740 and PPC750 incorporate a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *PowerPC 740™ PowerPC 750™ RISC Microprocessor User’s Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 4.

Table 4. Thermal Sensor Specifications

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Num	Characteristic	Min	Max	Unit	Notes
1	Temperature range	0	128	°C	1
2	Comparator settling time	20	—	ms	2
3	Resolution	4	—	°C	3

Notes:

1. The temperature is the junction temperature of the die. The thermal assist unit's (TAU) raw output does not indicate an absolute temperature, but it must be interpreted by software to derive the absolute junction temperature. For information on how to use and calibrate the TAU, contact your local IBM sales office. This specification reflects the temperature span supported by the design.
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. This value is guaranteed by design and is not tested.

Table 5 provides DC electrical characteristics for the PPC740 and PPC750.

Table 5. DC Electrical Specifications

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	3.465	V	1,2
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	OVdd	V	1
SYSCLK input low voltage	CV_{IL}	GND	0.4	V	

Table 5. DC Electrical Specifications (Continued)

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Characteristic	Symbol	Min	Max	Unit	Notes
Input leakage current, V_{in} = OVdd	I_{in}	—	30	µA	1,2
Hi-Z (off state) leakage current, Vin = OVdd	I_{TSI}	—	30	µA	1,2
Output high voltage, I_{OH} = –6mA	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	V_{OL}	—	0.4	V	
Capacitance, V_{in} =0 V, f = 1 MHz	C_{in}	—	5.0	pF	2,3

Notes:

1. For 60x bus signals, the reference is OVdd, while L2OVdd is the reference for the L2 bus signals.
2. Excludes test signals LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and IEEE 1149.1 signals.
3. Capacitance values are guaranteed by design and characterization, and are not tested.

Table 6 provides the power consumption for the PPC740 and PPC750.

Table 6. Power Consumption

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

	Processor CPU Frequency			Unit	Notes
	166/200 MHz	225/233 MHz	266 MHz		
Full-On Mode					
Typical	4.2	5.0	5.7	W	1,3,4,5
Maximum	6.0	7.0	7.9	W	1,2,4,5
Doze Mode					
Typical	1.6	1.8	2.1	W	1,2,5
Nap Mode					
Typical	250	250	250	mW	1,2,5
Sleep Mode					
Typical	100	100	100	mW	1,2,5
Sleep Mode - PLL and DLL Disabled					
Typical	30	30	30	mW	1,3,5,6

Notes:

1. These values apply for all valid 60x bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW
2. Maximum power is measured at maximum Vdd specified in Section Table 2., "Recommended Operating Conditions"
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.5 v (2.6 v at 233/266 MHz), OVdd = L2OVdd = 3.3 V in a system executing typical applications and benchmark sequences.

4. Full-on mode uses a worst case instruction mix.
5. Guaranteed by design and characterization, and is not tested.
6. Guaranteed and tested in Low Power Applications only, see Section 8.0, “Ordering Information“

3.1.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PPC740 and PPC750. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 3.1.2.1, “Clock AC Specifications“ and tested for conformance to the AC specifications for that frequency. These specifications are for 166, 200, 225, 233, and 266 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG(0-3) signals. Parts are sold by maximum processor core frequency; see Section 1.9, "Ordering Information".

3.1.2.1 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Figure 2 .

Table 7. Clock AC Timing Specifications

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Num	Characteristic	166/200 MHz*		225/233 MHz		266 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Processor frequency	150	200	150	233	150	266	MHz	
	VCO frequency	300	400	300	466	300	533	MHz	
	SYSCLK frequency	25	100	25	100	25	100	MHz	1
1	SYSCLK cycle time	12	40	12	40	12	40	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	—	2.0	ns	2,3
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	40	60	%	3
	SYSCLK jitter	—	±150	—	±150	—	±150	ps	4,3
	Internal PLL relock time	—	100	—	100	—	100	µs	5

Notes:

1. Caution: The SYSCLK frequency and the PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Section 7.1, “PLL Configuration“ for valid PLL_CFG[0-3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4 to 2.4 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. The total input jitter (short term and long term combined) must be under ±150 ps.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

* **Subject to availability** - see your marketing representative.

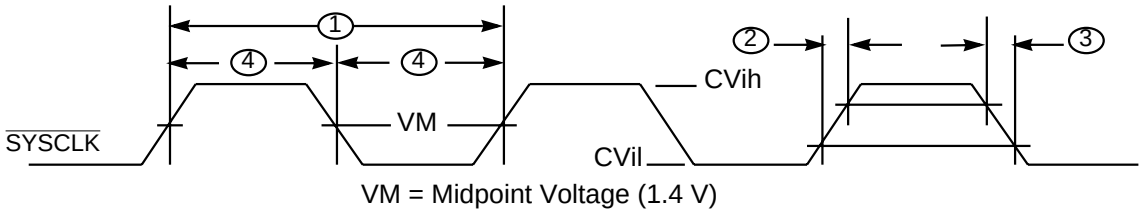


Figure 2. SYSCLK Input Timing Diagram

3.1.2.2 60x Bus Input AC Specifications

Table 8 provides the 60X bus input AC timing specifications for the PPC740 and PPC750 as defined in Figure 3 and Figure 4 . Input timing specifications for the L2 bus are provided in Section 3.1.2.5, “L2 Bus Input AC Specifications“.

Table 8. 60X Bus Input Timing Specifications[1]

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Num	Characteristic	Min	Max	Unit	Notes
10a	Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup)	2.5	—	ns	2
10b	All Other Inputs Valid to SYSCLK (Input Setup)	3.0	—	ns	3
10c	Mode Select Input Setup to $\overline{\text{HRESET}}$ ($\overline{\text{DRTRY}}$,$\overline{\text{TLBISYNC}}$)	8	—	t_{sysclk}	4,5,6,7
11a	SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold)	1.0	—	ns	2
11b	SYSCLK to All Other Inputs Invalid (Input Hold)	1.0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	0	—	ns	4,6,7

Notes:

1. Input specifications are measured from the TTL level (0.8 to 2.0 V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 3).
2. Address/Data Transfer Attribute inputs are composed of the following--A[0-31], AP[0-3], TT[0-4],$\overline{\text{TBST}}$, TSIZ[0-2], $\overline{\text{GBL}}$, DH[0-31), DL[0-31], DP[0-7].
3. All other signal inputs are composed of the following--$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TBEN}}$, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
5. t_{sysclk}, is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.

Figure 3 provides the input timing diagram for the PPC740 and PPC750.

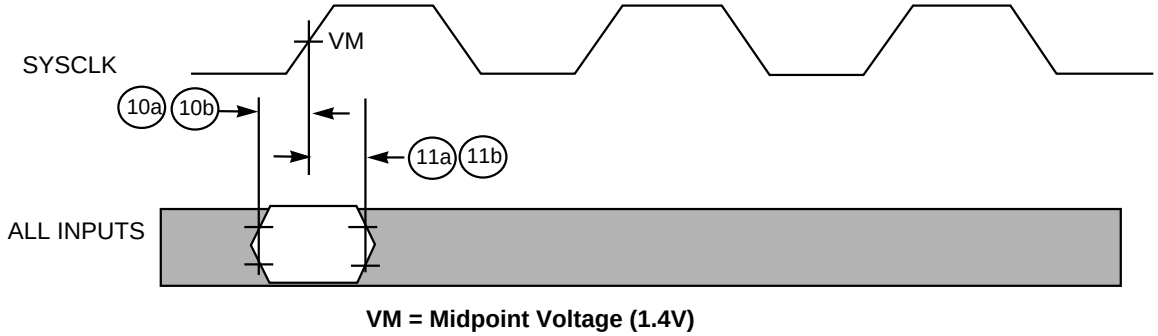


Figure 3. Input Timing Diagram

Figure 4 provides the mode select input timing diagram for the PPC740 and 750.

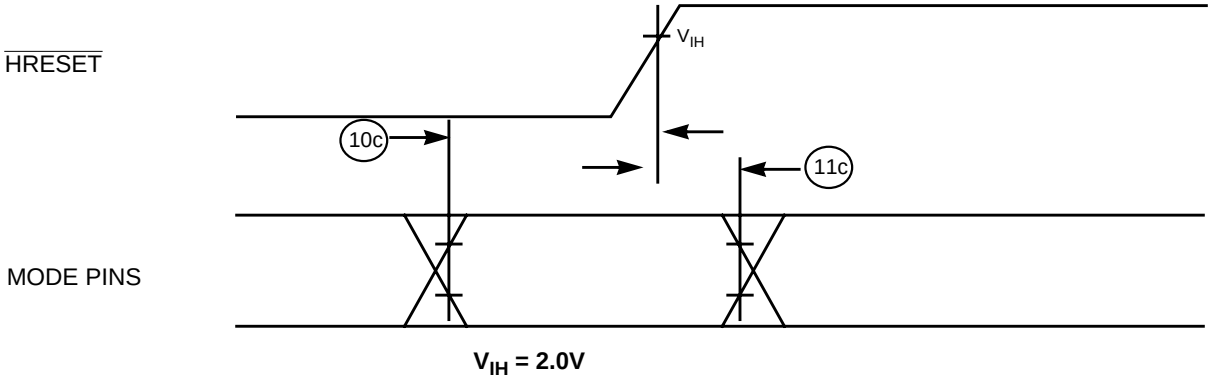


Figure 4. Mode Select Input Timing Diagram

3.1.2.3 60x Bus Output AC Specifications

Table 9 provides the 60x bus output AC timing specifications for the PPC740 and PPC750 as defined in Figure 5 . Output timing specification for the L2 bus are provided in Section 3.1.2.6, “L2 Bus Output AC Specifications“.

Table 9. 60X Bus Output AC Timing Specifications[1]

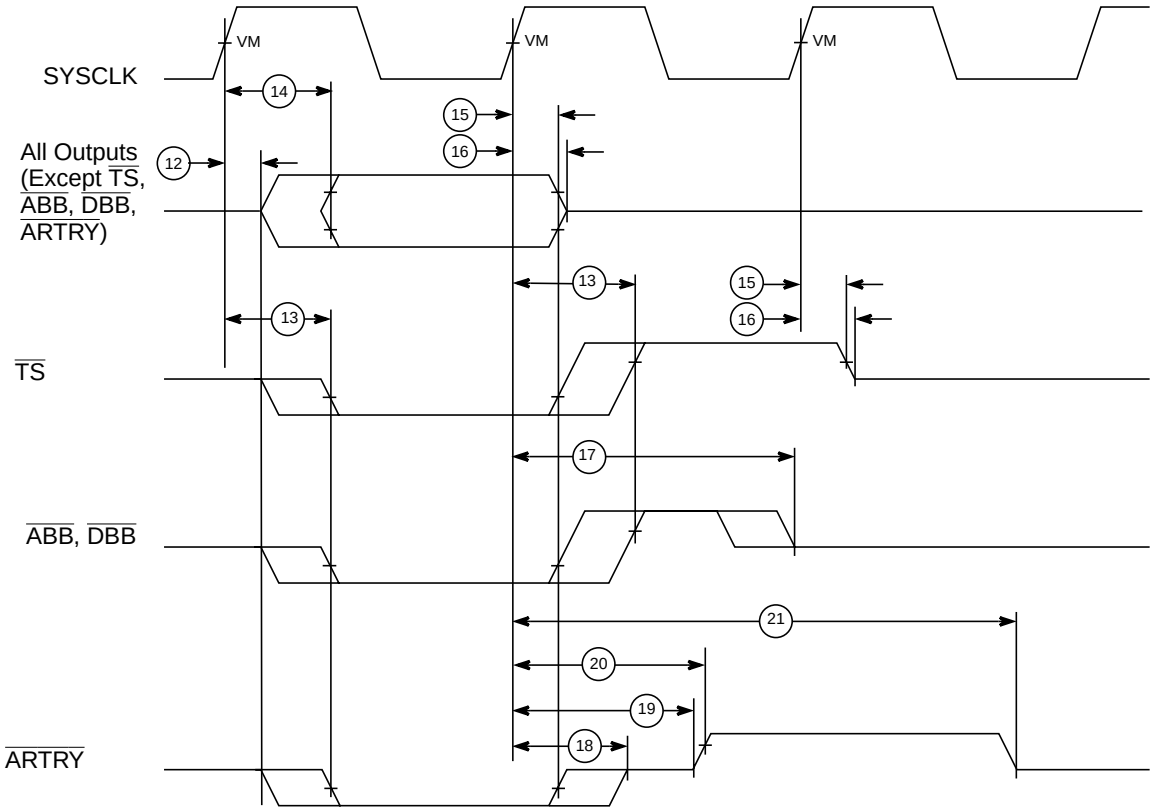
Operating conditions are specified in Section Table 2., "Recommended Operating Conditions" C_L = 50 pF[2]

Num	Characteristic	Min	Max	Unit	Notes
12	SYSCLK to Output Driven (Output Enable Time)	0.5	—	ns	
13	SYSCLK to Output Valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, and $\overline{DBB}$)	—	6.5	ns	5
14	SYSCLK to all other Output Valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, and $\overline{DBB}$)	—	6.5	ns	5
15	SYSCLK to Output Invalid (Output Hold)	1.0	—	ns	3
16	SYSCLK to Output High Impedance (all signals except $\overline{ABB}$, $\overline{ARTRY}$, and $\overline{DBB}$)	—	6.0	ns	8
17	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after pre-charge	—	1.0	t_{sysclk}	4,6,8
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	—	5.5	ns	8
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2* t_{sysclk} + 1.0	—	ns	3,4,7
20	Maximum delay to $\overline{ARTRY}$ precharge	—	1	t_{sysclk}	4,7
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	—	2	t_{sysclk}	4,7,8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes CL = 0 pF.
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
5. Output signal transitions from GND to 2.0 V or OVdd to 0.8 V.
6. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
7. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.
8. Guaranteed by design and characterization, and not tested.

Figure 5 provides the output timing diagram for the PPC740 and PPC750.



VM = Midpoint Voltage (1.4 V)

Figure 5. Output Timing Diagram

3.1.2.4 L2 Clock AC Specifications

Table 10 provides the L2CLK output AC timing specifications for the PPC740 and PPC750 as defined in Figure 6 .

Table 10. L2CLK Output AC Timing Specifications

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

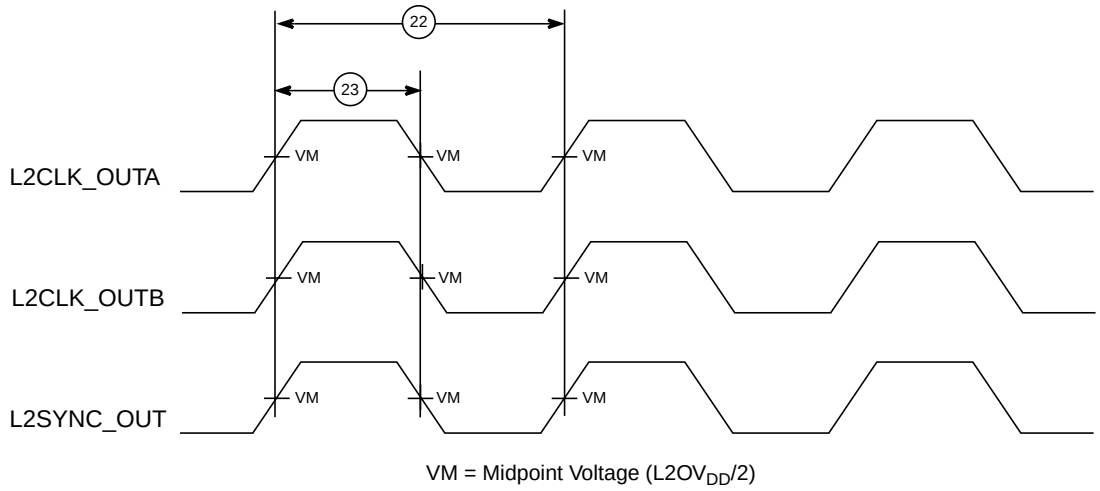
Num	Characteristic	Min	Max	Unit	Notes
	L2CLK frequency	80	133	MHz	1,5
22	L2CLK cycle time	7.5	12.5	ns	
23	L2CLK duty cycle	50		%	2
	L2CLK jitter		±150	ps	3,6
	Internal DLL-relock time	640	—	L2CLK	4

Notes:

1. L2CLK outputs are L2CLKOUTA, L2CLKOUTB and L2SYNC_OUT pins. The internal design supports higher L2CLK frequencies; however, the L2 I/O drivers have been designed to support a 133 MHz L2 bus loaded with 4 off-the-shelf pipelined synchronous burst SRAMs. Running the L2 bus beyond 133 MHz would require tightly coupled customized SRAMs or a multi-chip module (MCM) implementation. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. L2CLKOUTA and L2CLKOUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The total input jitter (short term and long term combined) must be under ± 150 ps.
4. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization, and is not tested.
5. The L2CR [L2SL] bit should be set for L2CLK frequencies less than 110 MHz.
6. Guaranteed by design and characterization, and not tested.

The L2CLK_OUT timing diagram is shown in Figure 6 .

L2 SIngle-Ended Clock Mode



L2 Differential Clock Mode

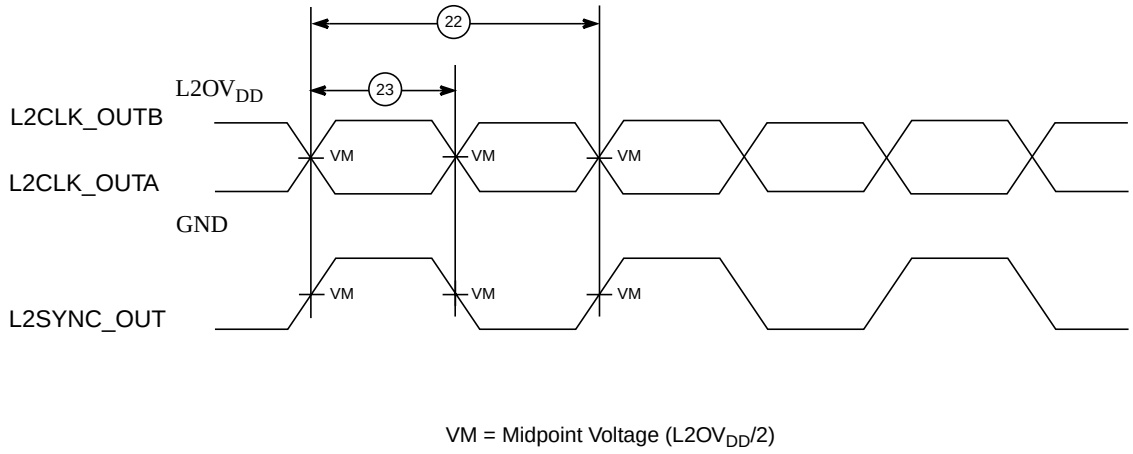


Figure 6. L2CLK_OUT Output Timing Diagram

3.1.2.5 L2 Bus Input AC Specifications

The L2 bus input interface AC timing specifications are found in Table 11 .

Table 11. L2 Bus Input Interface AC Timing Specifications[1]

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Num	Characteristic	Min	Max	Unit	Notes
29,30	L2SYNC_IN rise and fall time	—	1.0	ns	2,3
24	Data and parity input setup to L2SYNC_IN	2.0	—	ns	
25	L2SYNC_IN to data and parity input hold	0.5	—	ns	

Notes:

1. All input specifications are measured from the midpoint voltage (1.4V) of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN. Input timings are measured at the pins (see Figure 7).
2. Rise and fall times for the L2SYNC_IN input are measured from 0.4 to 2.4V.
3. Guaranteed by design and characterization, and not tested.

Figure 7 shows the L2 bus input timing diagrams for the PPC750.

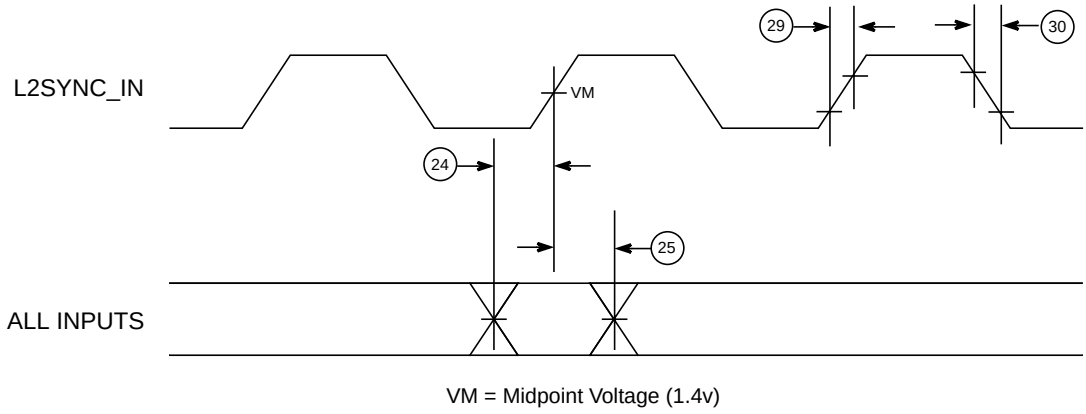


Figure 7. L2 Bus Input Timing Diagrams

3.1.2.6 L2 Bus Output AC Specifications

Table 12 provides the L2 bus output interface AC timing specifications for the PPC750 as defined in Figure 8 .

Table 12. L2 Bus Output Interface AC Timing Specifications[1]

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions" C_L = 20 pF[3]

Num	Characteristic	L2CR[14-15] is equivalent to:								Unit	Notes
		00[2]		01		10		11			
		Min	Max	Min	Max	Min	Max	Min	Max		
26	L2SYNC_IN to output valid	—	5.0	—	5.5	—	Rsv[5]	—	Rsv[5]	ns	
27	L2SYNC_IN to output hold	0.5	—	1.0	—	Rsv[5]	—	Rsv[5]	—	ns	4
28	L2SYNC_IN to high impedance	—	4.0	—	4.5	—	Rsv[5]	—	Rsv[5]	ns	6

Notes:

1. All outputs are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint voltage (1.4 V) of the signal in question. The output timings are measured at the pins.
2. The outputs are valid for both single-ended and differential L2CLK modes. For flow-thru and pipelined reg-reg synchronous burst SRAMs, L2CR[14-15] = 00 is recommended. For pipelined late-write synchronous burst SRAMs, L2CR[14-15] = 01 is recommended.
3. All maximum timing specifications assume CL = 20 pF.
4. This measurement assumes CL= 5 pF.
5. Reserved for future use.
6. Guaranteed by design and characterization, and not tested.

Figure 8 shows the L2 bus output timing diagrams for the PPC750.

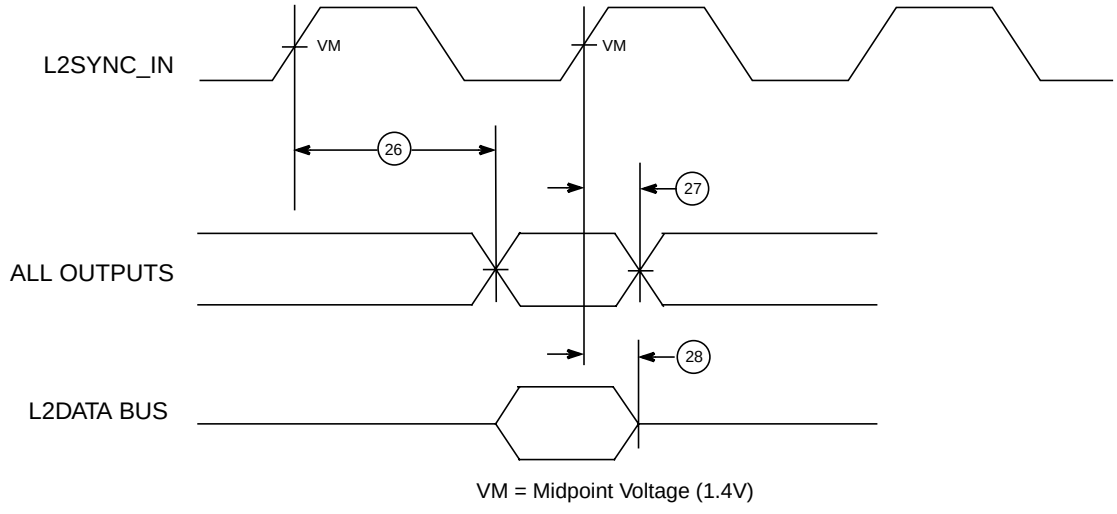


Figure 8. L2 Bus Output Timing Diagrams

3.1.3 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 9 , Figure 10 , Figure 11 , and Figure 12 . The five JTAG signals are; TDI, TDO, TMS, TCK, and $\overline{\text{TRST}}$.

Table 13. JTAG AC Timing Specifications (Independent of SYSCLK)

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions" C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	33.3	MHz	
1	TCK cycle time	30	—	ns	
2	TCK clock pulse width measured at 1.4V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	spec obsolete, intentionally omitted				
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	4	—	ns	2
7	Boundary-scan input data hold time	15	—	ns	2
8	TCK to output data valid	4	20	ns	3,5
9	TCK to output high impedance	3	19	ns	3,4
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	12	—	ns	
12	TCK to TDO data valid	2.5	12	ns	5
13	TCK to TDO high impedance	3	9	ns	4

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum spec guaranteed by characterization and not tested.

Figure 9 provides the JTAG clock input timing diagram.

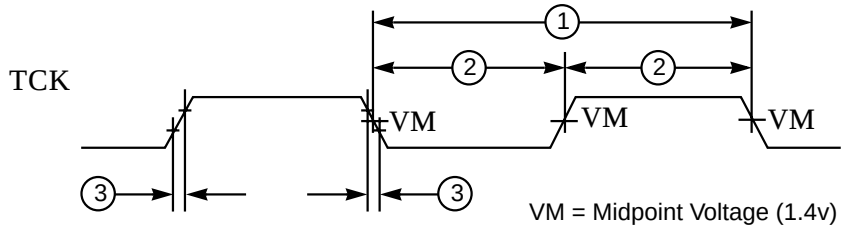


Figure 9. JTAG Clock Input Timing Diagram

Figure 10 provides the $\overline{\text{TRST}}$ timing diagram.

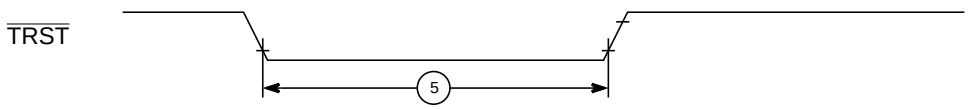


Figure 10. $\overline{\text{TRST}}$ Timing Diagram

Figure 11 provides the boundary-scan timing diagram.

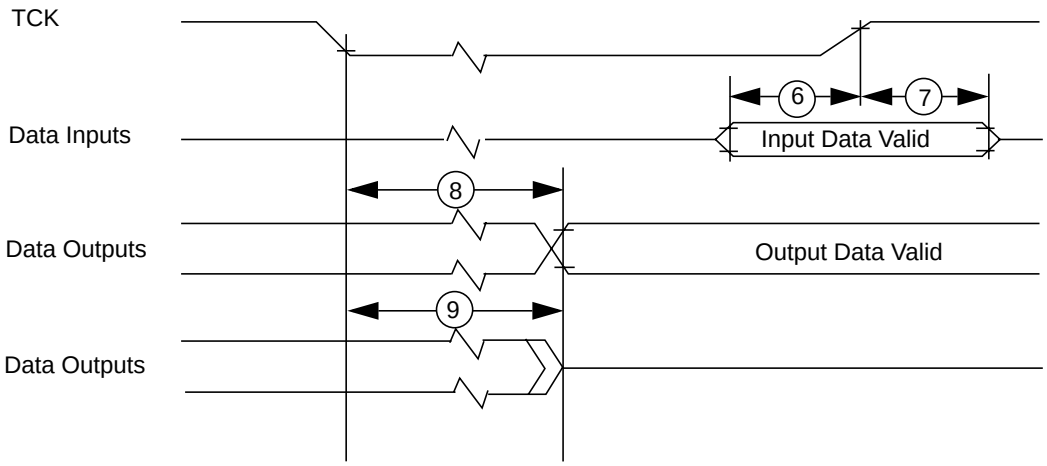


Figure 11. . Boundary-Scan Timing Diagram

Figure 12 provides the test access port timing diagram.

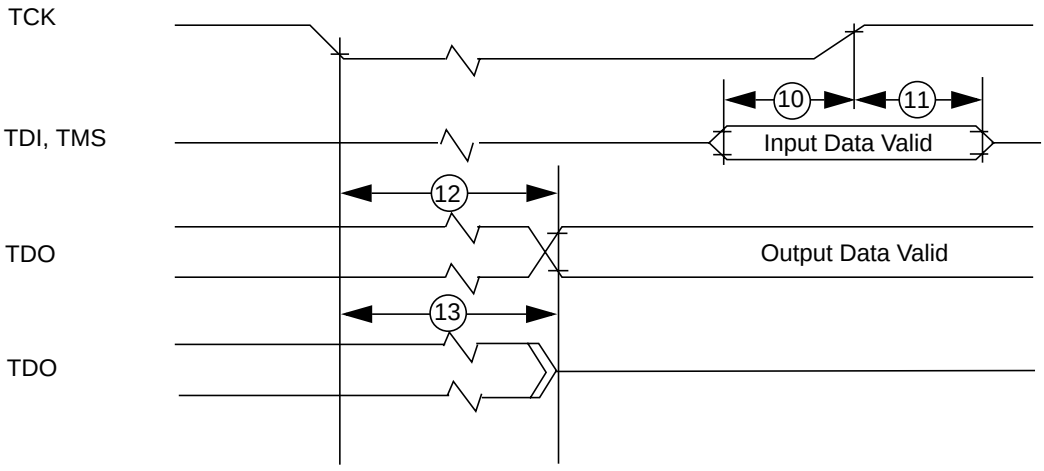


Figure 12. Test Access Port Timing Diagram

4.0 PPC740 and PPC750 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the PPC740 and PPC750. IBM offers two ceramic ball grid array (BGA) packages: a 255 CBGA (the PPC740) and a 360 CBGA (the PPC750).

Figure 13 (in part A) shows the pinout of the 255 CBGA package as viewed from the top surface. Part B shows the side profile of the 255 CBGA package to indicate the direction of the top surface view.

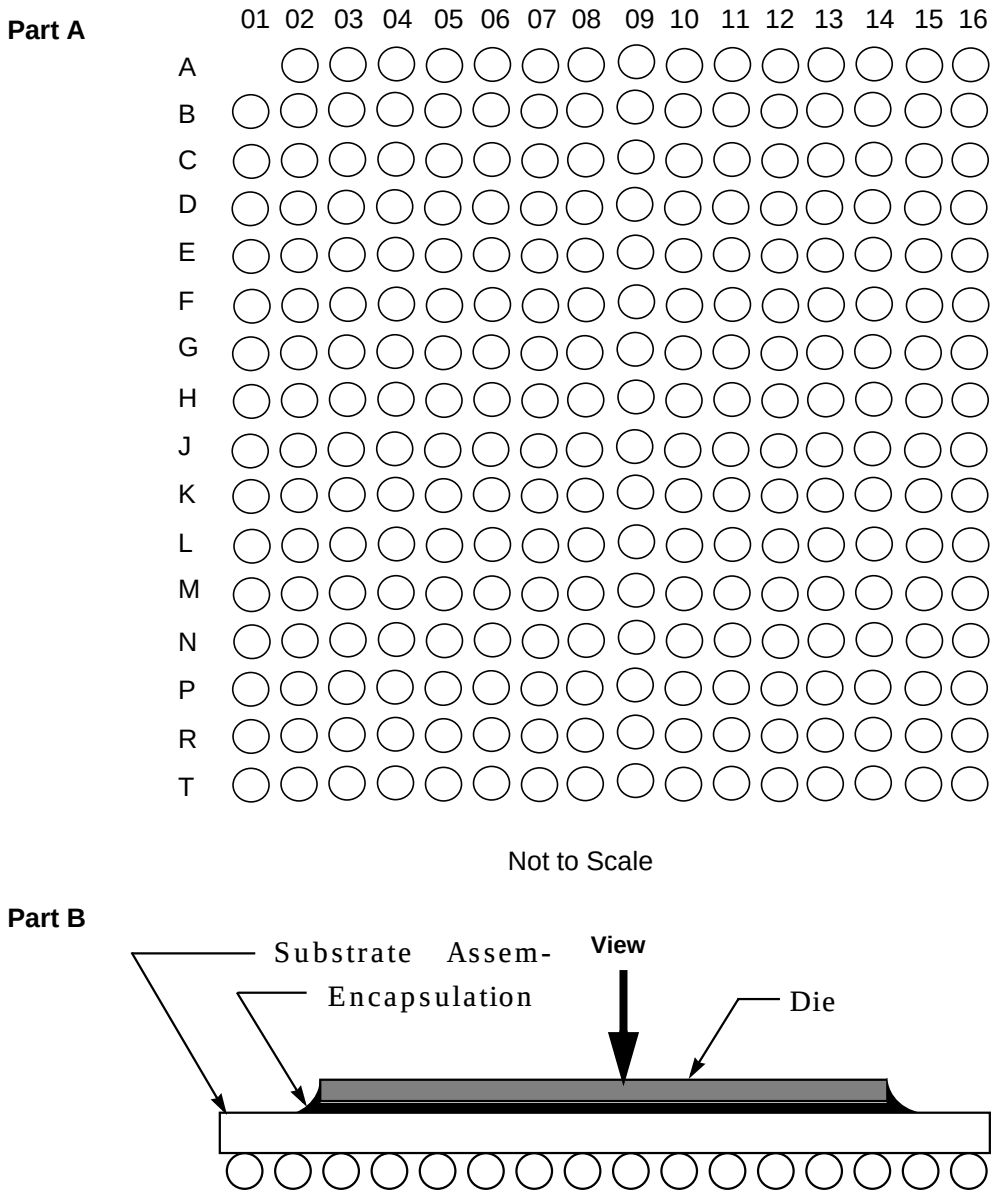


Figure 13. Pinout of the PPC740 BGA Package as Viewed from the Top Surface

Figure 14 (in part A) shows the pinout of the 360 CBGA package as viewed from the top surface. Part B shows the side profile of the 360 CBGA package to indicate the direction of the top surface view.

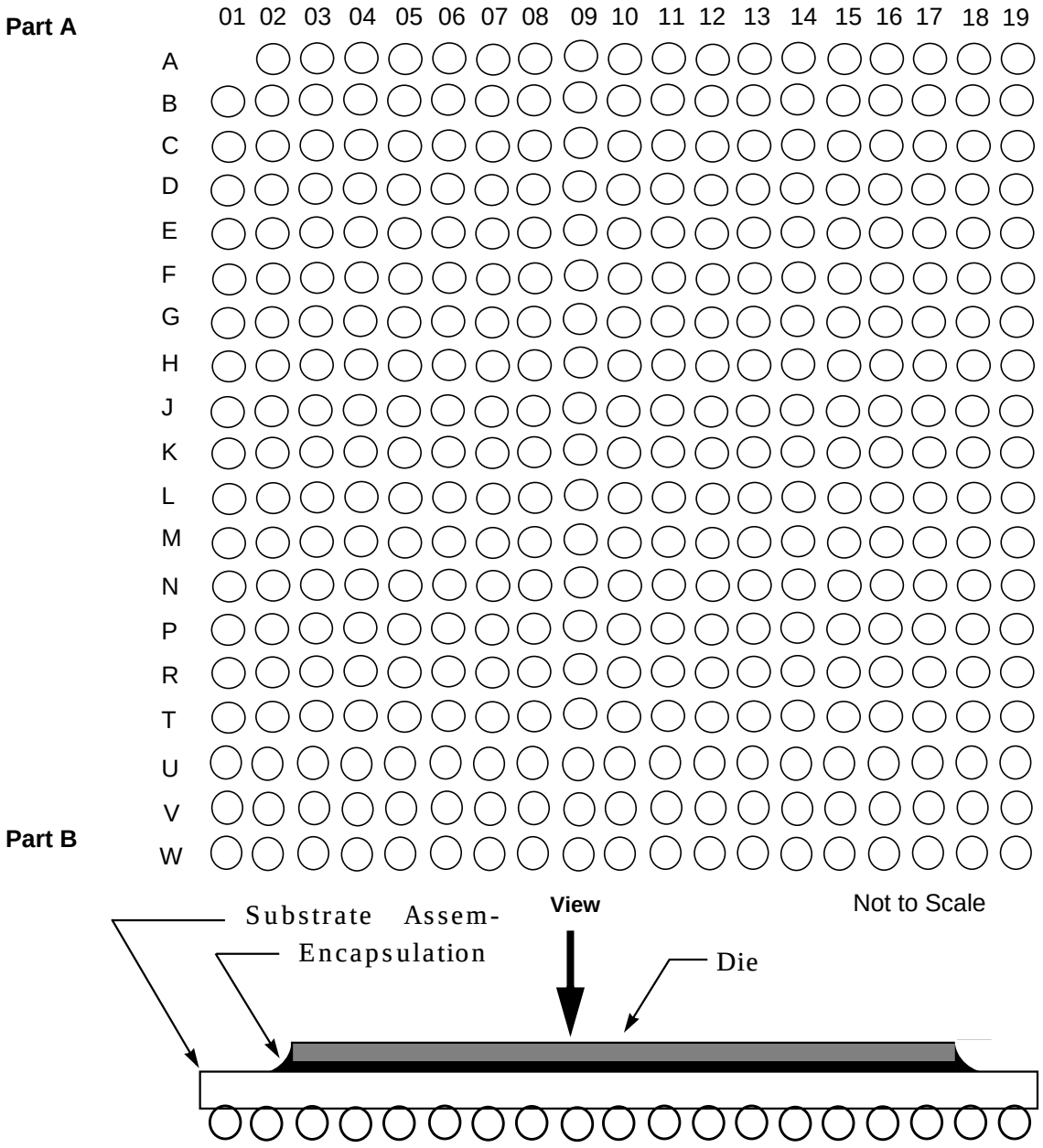


Figure 14. Pinout of the PPC750 CBGA Package as Viewed from the Top Surface

5.0 PPC740 and PPC750 Microprocessor Pinout Listings

Table 14 provides the pinout listing for the 255 CBGA package (the PPC740).

Table 14. Pinout Listing for the 255 CBGA Package

Signal Name	Pin Number	Active	I/O
A0-A31	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
AACK	L02	Low	Input
ABB	K04	Low	I/O
AP0-AP3	C01, B04, B03, B02	High	I/O
ARTRY	J04	Low	I/O
AVDD	A10	—	—
BG	L01	Low	Input
BR	B06	Low	Output
CI	E01	Low	Output
CKSTP_IN	D08	Low	Input
CKSTP_OUT	A06	Low	Output
CLK_OUT	D07	—	Output
DBB	J14	Low	I/O
DBG	N01	Low	Input
DBDIS	H15	Low	Input
DBWO	G04	Low	Input
DH0-DH31	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL0-DL31	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP0-DP7	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
DRTRY	G16	Low	Input
GBL	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
HRESET	A07	Low	Input
INT	B15	Low	Input

Table 14. Pinout Listing for the 255 CBGA Package (Continued)

Signal Name	Pin Number	Active	I/O
L1_TSTCLK [1]	D11	High	Input
L2_TSTCLK [1]	D12	High	Input
LSSD_MODE [1]	B10	Low	Input
MCP	C13	Low	Input
NC (No-Connect)	B07, B08, C03, C06, C08, D05, D06, H04, J16, A04, A05, A02, A03, B01, B05	—	—
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0-3]	A08, B09, A09, D09	High	Input
QACK	D03	Low	Intput
QREQ	J03	Low	Output
RSRV	D01	Low	Output
SMI	A16	Low	Input
SRESET	B14	Low	Input
SYSCLK	C09	—	Input
TA	H14	Low	Input
TBEN	C02	High	Input
TBST	A14	Low	I/O
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
TEA	H13	Low	Input
TLBISYNC	C04	Low	Input
TMS	B11	High	Input
TRST	C10	Low	Input
TS	J13	Low	I/O
TSIZ0-TSIZ2	A13, D10, B12,	High	Output
TT0-TT4	B13, A15, B16, C14, C15	High	I/O
WT	D02	Low	Output
VDD [2]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
VOLTDET[3]	F03	Low	Output

Note:

1. These are test signals for factory use only and must be pulled up to OVdd for normal operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
3. Internally tied to GND in the 255 CBGA package to indicate to the power supply that a low-voltage processor is present. This is NOT a supply pin.

Table 15 provides the pinout listing for the 360 CBGA package (the PPC750).

Table 15. Pinout Listing for the 360 CBGA package

Signal Name	Pin Number	Active	I/O
A0-A31	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O
AACK	N3	Low	Input
ABB	L7	Low	I/O
AP0-AP3	C4, C5, C6, C7	High	I/O
ARTRY	L6	Low	I/O
AVDD	A8	—	—
BG	H1	Low	Input
BR	E7	Low	Output
CKSTP_OUT	D7	Low	Output
CI	C2	Low	Output
CKSTP_IN	B8	Low	Input
CLKOUT	E3	--	Output
DBB	K5	Low	I/O
DBDIS	G1	Low	Input
DBG	K1	Low	Input
DBWO	D1	Low	Input
DH0-DH31	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O
DL0-DL31	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O
DP0-DP7	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O
DRTRY	H6	Low	Input
GBL	B1	Low	I/O

Table 15. Pinout Listing for the 360 CBGA package (Continued)

Signal Name	Pin Number	Active	I/O
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—
HRESET	B6	Low	Input
INT	C11	Low	Input
L1_TSTCLK [1]	F8	High	Input
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output
L2AVDD	L13	—	—
L2CE	P17	Low	Output
L2CLKOUTA	N15	—	Output
L2CLKOUTB	L16	—	Output
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—
L2SYNC_IN	L14	—	Input
L2SYNC_OUT	M14	—	Output
L2_TSTCLK[1]	F7	High	Input
L2WE	N16	Low	Output
L2ZZ	G17	High	Output
$\overline{\text{LSSD\_MODE}}$[1]	F9	Low	Input
MCP	B11	Low	Input
NC (No-Connect)	B3, B4, B5, A19, W19, W1, K9, K11[4], K19[4]	—	—
OVDD [2]	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input
QACK	B2	Low	Input

Table 15. Pinout Listing for the 360 CBGA package (Continued)

Signal Name	Pin Number	Active	I/O
QREQ	J3	Low	Output
RSRV	D3	Low	Output
SMI	A12	Low	Input
SRESET	E10	Low	Input
SYSCLK	H9	—	Input
TA	F1	Low	Input
TBEN	A2	High	Input
TBST	A11	Low	I/O
TCK	B10	High	Input
TDI	B7	High	Input
TDO	D9	High	Output
TEA	J1	Low	Input
TLBISYNC	A3	Low	Input
TMS	C8	High	Input
TRST	A10	Low	Input
TS	K7	Low	I/O
TSIZ0-TSIZ2	A9, B9, C9	High	Output
TT0-TT4	C10, D11, B12, C12, F11	High	I/O
WT	C3	Low	Output
VDD [2]	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—
VOLTDET[3]	K13	High	Output

Notes:

1. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.
3. Internally tied to L2OVDD in the PID-8t PPC750 360 CBGA package to indicate to the power supply that a 2.5v core voltage processor is present. Future lower core voltage processors may tie this pin internally to GND. **CAUTION:** this is different from the 255 CBGA package. This is NOT a supply pin.
4. These pins are reserved for potential future use as additional L2 address pins.

6.0 PPC740 and PPC750 Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the PPC740 and PPC750.

6.1 Parameters for the 255 CBGA Package (PPC740)

The package parameters are as provided in the following list. The package type is 21 x 21 mm, 255-lead ceramic ball grid array (CBGA).

Package outline	21 x 21 mm
Interconnects	255 (16 x 16 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.45 mm
Maximum module height	3.00 mm
Ball diameter	0.89 mm (35 mil)

Note: The PPC740 (255 CBGA) package offering is **subject to availability** - see your IBM marketing representative.

6.1.1 Mechanical Dimensions of the 255 CBGA Package

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the BGA package.

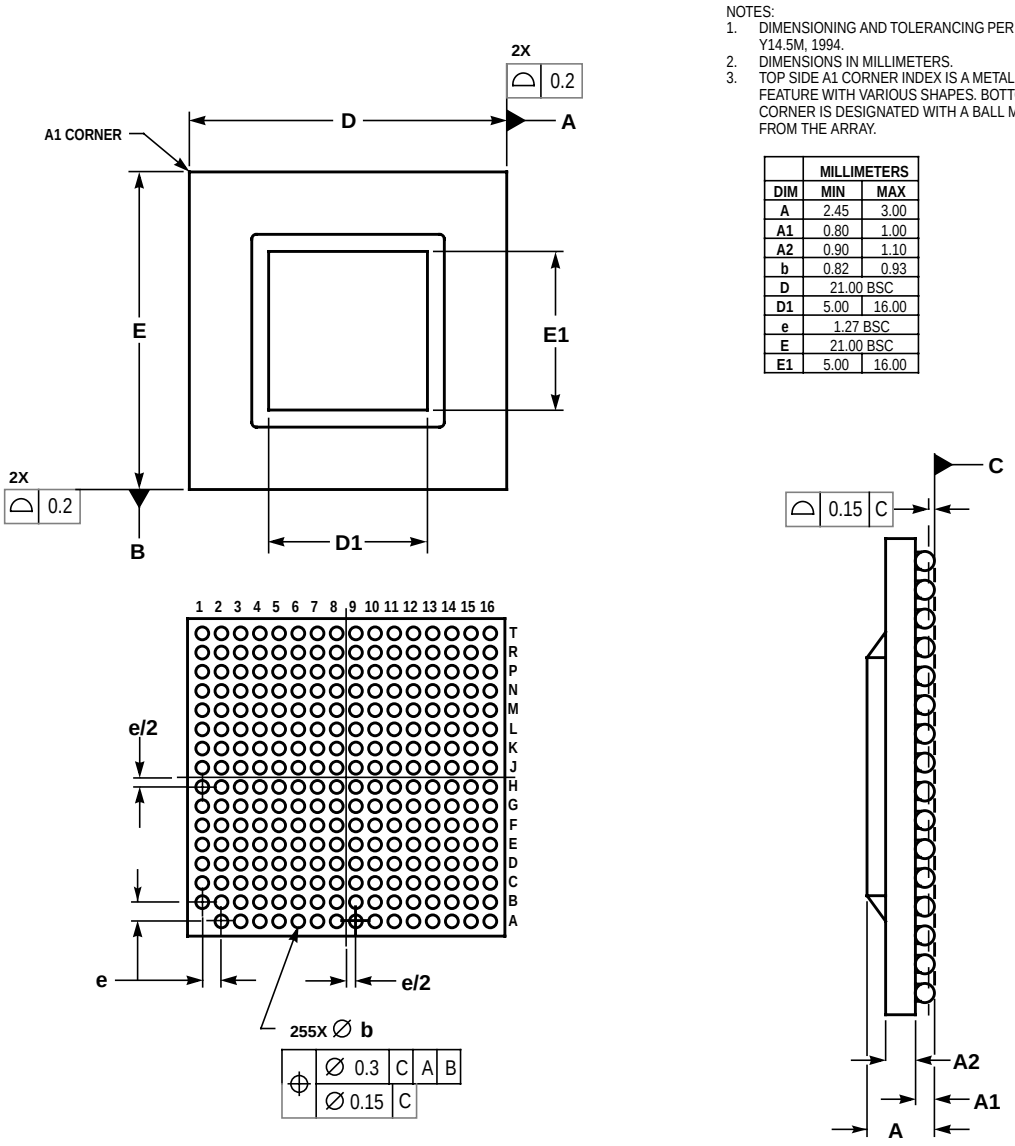


Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature of the 255 CBGA Package

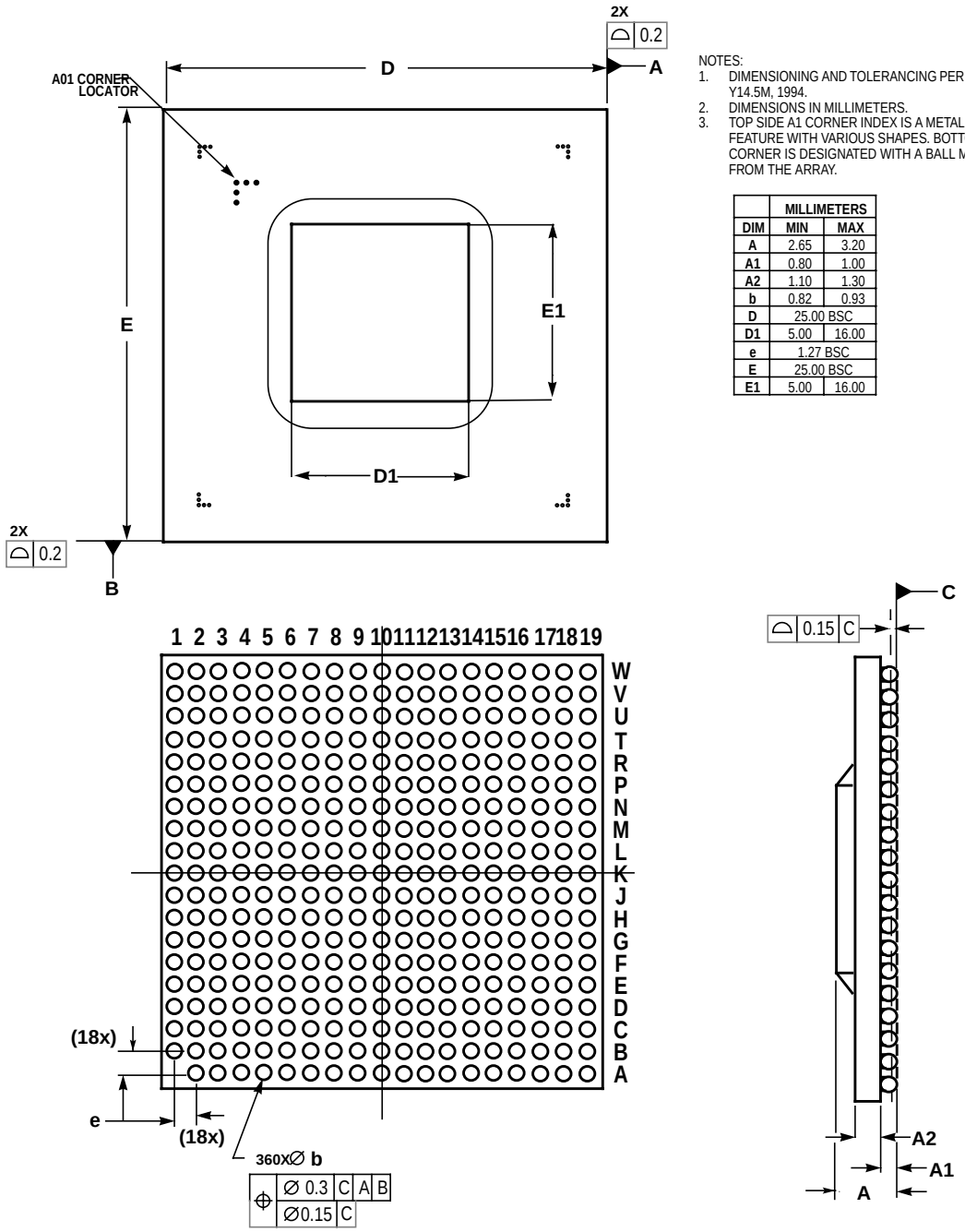
6.2 Parameters for the 360 CBGA Package (PPC750)

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 x 25 mm
Interconnects	360 (19 x 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)

6.2.1 Mechanical Dimensions of the 360 CBGA Package

Figure 16 provides the mechanical dimensions and bottom surface nomenclature of the 360 CBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.65	3.20
A1	0.80	1.00
A2	1.10	1.30
b	0.82	0.93
D	25.00 BSC	
D1	5.00	16.00
e	1.27 BSC	
E	25.00 BSC	
E1	5.00	16.00

Not To Scale

Figure 16. Mechanical Dimensions and Bottom Surface Nomenclature of the 360 CBGA Package

7.0 System Design Information

This section provides electrical and thermal design recommendations for successful application of the PPC740 and PPC 750.

7.1 PLL Configuration

The PLL for the PPC740 and PPC750 is configured by the PLL_CFG[0-3-] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PPC740 and PPC750 is shown in Table 16 for nominal frequencies.

Table 16. PPC740 and PPC750 Microprocessor PLL Configuration

PLL_CFG (0:3)		Processor to Bus Frequency Ratio (r)	VCO Divider (d)	Frequency Range Supported by VCO having an example range of VCO_{min}=300 to VCO_{max}=533 (MHz)			
				SYSCLK		Core	
bin	dec			Min= VCO_{min}/(r*d)	Max= VCO_{max}/(r*d)	Min= VCO_{min}/d	Max= VCO_{max}/d
0000	0	Rsv[1]	n/a	n/a	n/a	n/a	n/a
0001	1	7.5x	2	25[2]	35	150	266
0010	2	7x	2	25[2]	38		
0011	3	PLL Bypass[3]	n/a	n/a	n/a	n/a	n/a
0100	4	Rsv[1]	n/a	n/a	n/a	150	266
0101	5	6.5x	2	25[2]	41		
0110	6	Rsv[1]	n/a	n/a	n/a	n/a	n/a
0111	7	4.5x	2	33	59	150	266
1000	8	3x	2	50	83[5]		
1001	9	5.5x	2	27	48		
1010	10	4x	2	37	67		
1011	11	5x	2	30	53		
1100	12	8x	2	25[2]	33		
1101	13	6x	2	25	44		
1110	14	3.5x	2	43	83[5]		
1111	15	Off[4]	n/a	n/a	n/a	Off	Off

Notes:

1. Reserved settings.
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see Section 3.1.2.1,

"Clock AC Specifications" for valid SYSCLK and VCO frequencies.

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock - off mode, no clocking occurs inside the PPC740 or PPC750 regardless of the SYSCLK input.
5. This limit is 83.3 MHz as specified in Section 3.1.2.1, "Clock AC Specifications".

Table 17 provides sample core-to-L2 frequencies.

Table 17. Sample Core-to-L2 Frequencies[1]

Core Frequency in MHz	÷1	÷1.5	÷2	÷2.5	÷3
200	—	133.3	100	80	—
225	—	—	112.5	90	—
233	—	—	116.5	93.2	—
250	—	—	125	100	83.3
266	—	—	133	106.4	88.6

Note:

1. Although the PPC750 is designed for L2 bus ratios of 1:1, 1.5:1, 2:1, 2.5:1 and 3:1, this specification supports the L2 frequency range specified in Section 3.1.2.4, "L2 Clock AC Specifications". For higher L2 frequencies not supported in this document, please contact your IBM marketing representative.

7.2 PLL Power Supply Filtering

The AVdd and L2AVdd power signals are provided on the PPC740 and PPC750 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 17 . The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible. An identical but separate circuit should be placed as close as possible to the L2AVdd pin.

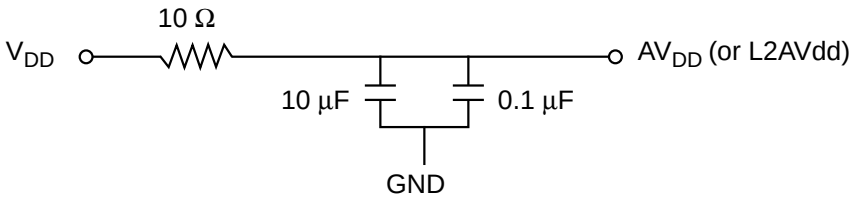


Figure 17. PLL Power Supply Filter Circuit

7.3 Decoupling Recommendations

Due to the PPC740's and PPC750's dynamic power management feature, large address and data buses, and high operating frequencies, the PPC740 and PPC750 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other com-

ponents in the PPC740 and PPC750 systems, and the processor itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin (and L2OVdd for the 360 CBGA) of the PPC740 and PPC750. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should range in value from 220 pF to 10 µF to provide both high- and low- frequency filtering, and should be placed as close as possible to their associated Vdd or OVdd pins. Suggested values for the Vdd pins -- 220 pF (ceramic), 0.01 µF (ceramic), and 0.1 µf (ceramic). Suggested values for the OVdd pins -- 0.01 µF (ceramic), 0.1 µf (ceramic), and 10 µF (tantalum). Only SMT (surface-mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors -- 100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, and GND, pins of the PPC740 and PPC750.

External clock routing should ensure that the rising-edge of the L2 clock is coincident at the CLK input of all SRAMs and at the L2SYNC_IN input of the PPC740 and PPC750. The L2CLKOUTA network could be used only, or the L2CLKOUTB network could also be used, depending on the loading, frequency, and number of SRAMs.

7.5 Output Buffer DC Impedance

The PPC750 60x and L2 I/O drivers were characterized over process, voltage and temperature. To measure Z_0, an external resistor is connected to the chip pad, either to OVdd or GND. Then, the value of such resistor is varied until the pad voltage is OVdd/2; see Section Figure 18., "Driver Impedance Measurement".

The output impedance is actually the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = OVdd/2. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = OVdd/2. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

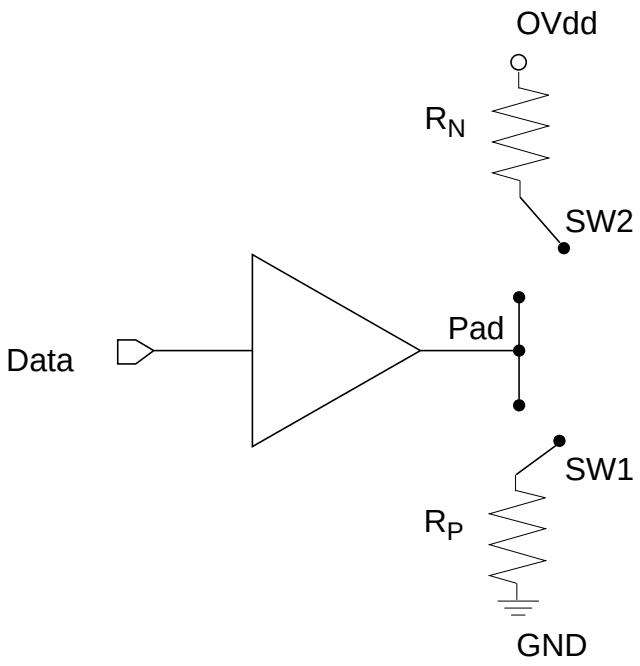


Figure 18. Driver Impedance Measurement

Table 18 summarizes the impedance a board designer would design to for a typical process. These values were derived by simulation at 65C. As the process improves, the output impedance will be lower by several ohms than this typical value.

Table 18. Impedance Characteristics

Operating conditions are specified in Section Table 2., "Recommended Operating Conditions"

Process	60x	L2	Symbol	Unit
Typical	43	38	Z_0	W

7.6 Pull-up Resistor Requirements

The PPC740 and PPC750 require high -resistive (weak: 10 KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PPC740 and PPC750 or other bus masters. These signals are -- $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the PPC750 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 KΩ - 1- KΩ) if it is used by the system. This signal is -- $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the PPC740 and PPC750 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the processor or by other receivers in the system. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors or restored in some manner by the system, The snooped address and transfer attribute inputs are -- A[0-31], AP[0-3], TT[0-4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods. The data bus signals are -- DH[0-31], DL[0-31], and DP[0-7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, than all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

No pull-up resistors are normally required for the L2 interface.

7.7 Thermal Management Information

This section provides thermal management information for the CBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, air flow and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods -- adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 19 . This spring force should not exceed 5.5 pounds.

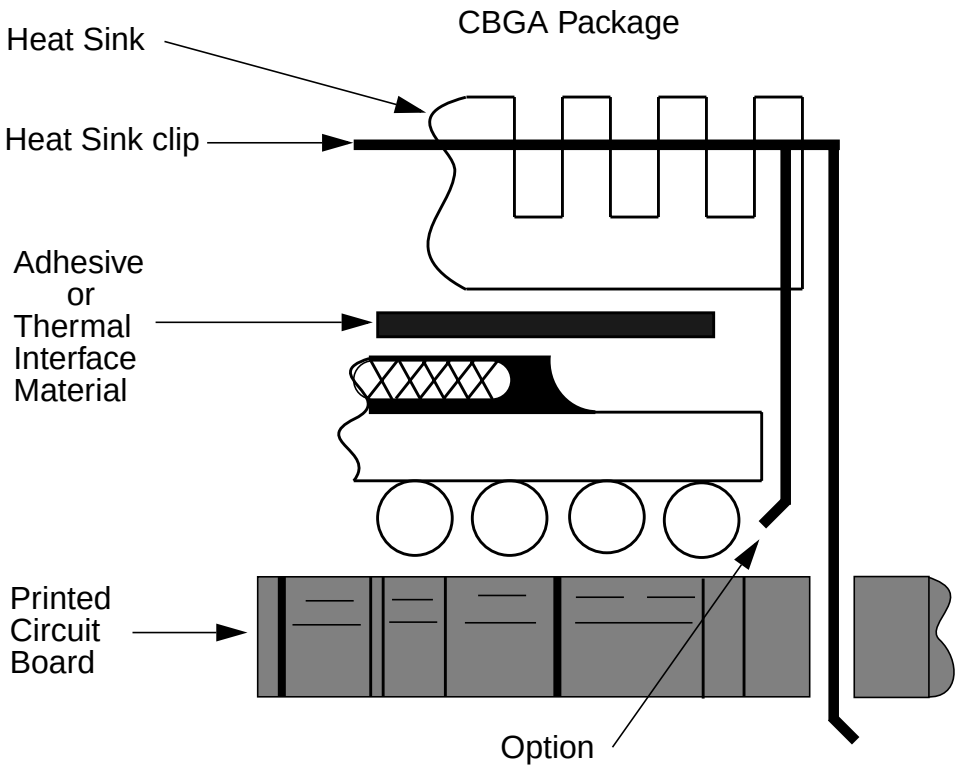


Figure 19. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the PPC740 and PPC750. There are several commercially-available heat sinks provided by the following vendors:

Chip Coolers, Inc. 800-227-0254 (USA/Canada)
333 Strawberry Field Rd. 401-739-7600
Warwick, RI 02887-6979

Thermalloy
2021 W. Valley View Lane 214-243-4321
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation (IERC)
135 W. Magnolia Blvd.
Burbank, CA 91502 818-842-7277

Aavid Engineering 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

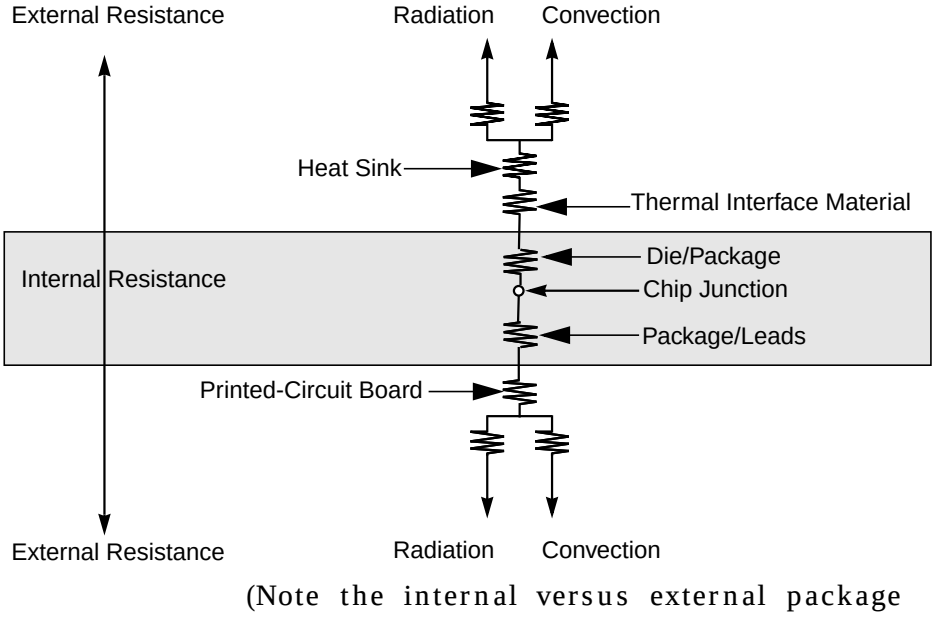
Ultimately, the final selection of an appropriate heat sink for the PPC740 and PPC750 depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

7.7.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 3 , the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

Figure 20 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package

Figure 20. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection. Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

7.7.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by a spring clip mechanism, Figure 21 shows the thermal performance of three thin-sheet thermal-interface materials (silicon, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times

greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 19). This spring force should not exceed 5.5 pounds. Therefore the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors -- thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

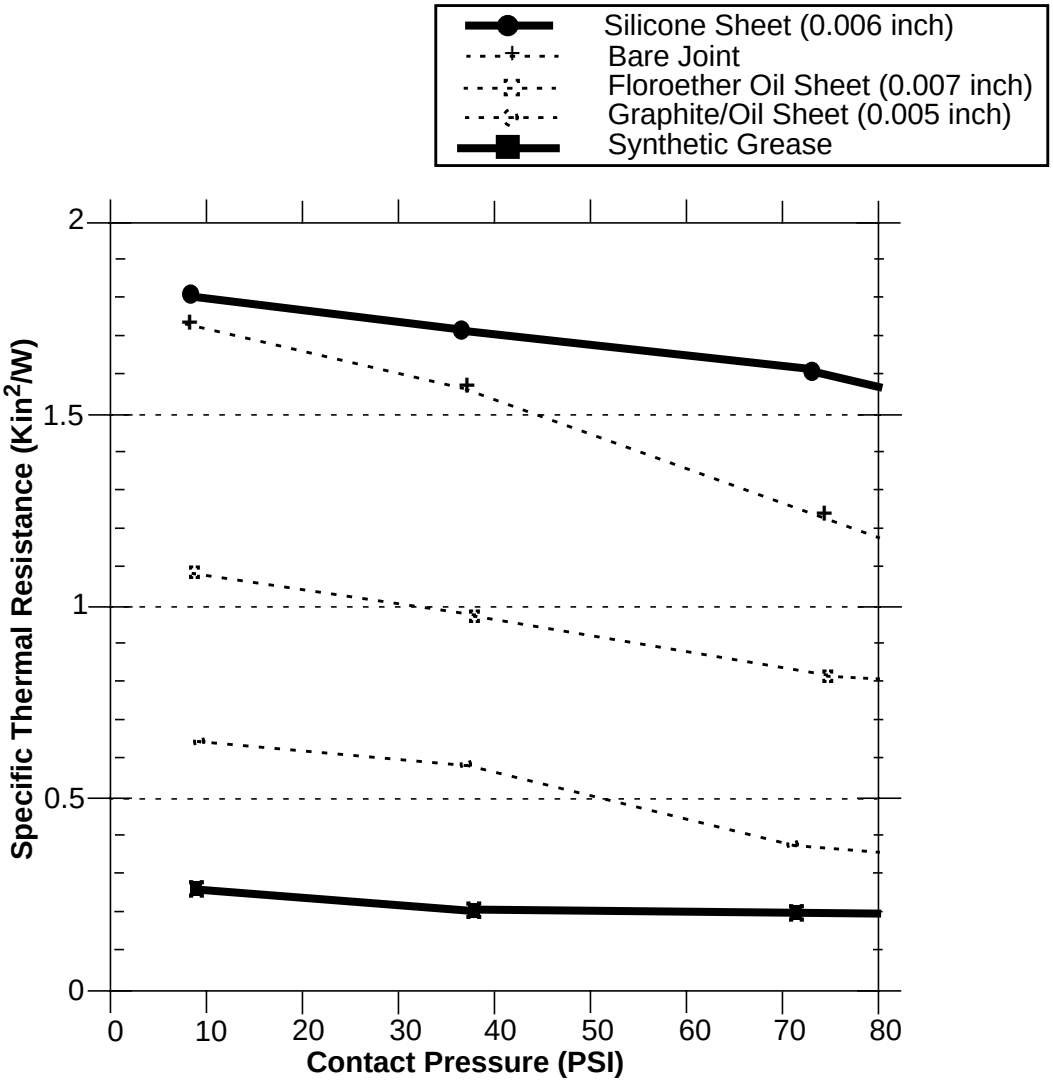


Figure 21. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interfaces. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation 517-496-4000

Dow-Corning Electronic Materials

P.O. Box 0997

Midland, MI 48686-0997

Chomerics, Inc. 617-935-4850

77 Dragon Court

Woburn, MA 01888-4850

Thermagon, Inc. 216-741-7659

3256 West 25th Street

Cleveland, OH 44109-1668

Loctite Corporation 860-571-5100

1001 Trout Brook Crossing

Rocky Hill, CT 06067

AI Technology (e.g. EG7655) 609-882-2332

1425 Lower Ferry Road

Trent, NJ 08618

The following section provides a heat sink selection example using one of the commercially available heat sinks.

7.8 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the system cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the thermal resistance of the thermal interface material

θ_{sa} is the heat sink-to-ambient thermal resistance

P_d is the power dissipated by the device

Typical die-junction temperatures (T_j) should be maintained less than the value specified in Table 3 . The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The

thermal resistance of the interface material (θ_{int}) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, a CBGA package θ_{jc} = 0.03, and a power dissipation (P_d) of 5.0 watts, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + \theta_{sa}) * 5\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus air flow velocity is shown in Figure 22 .

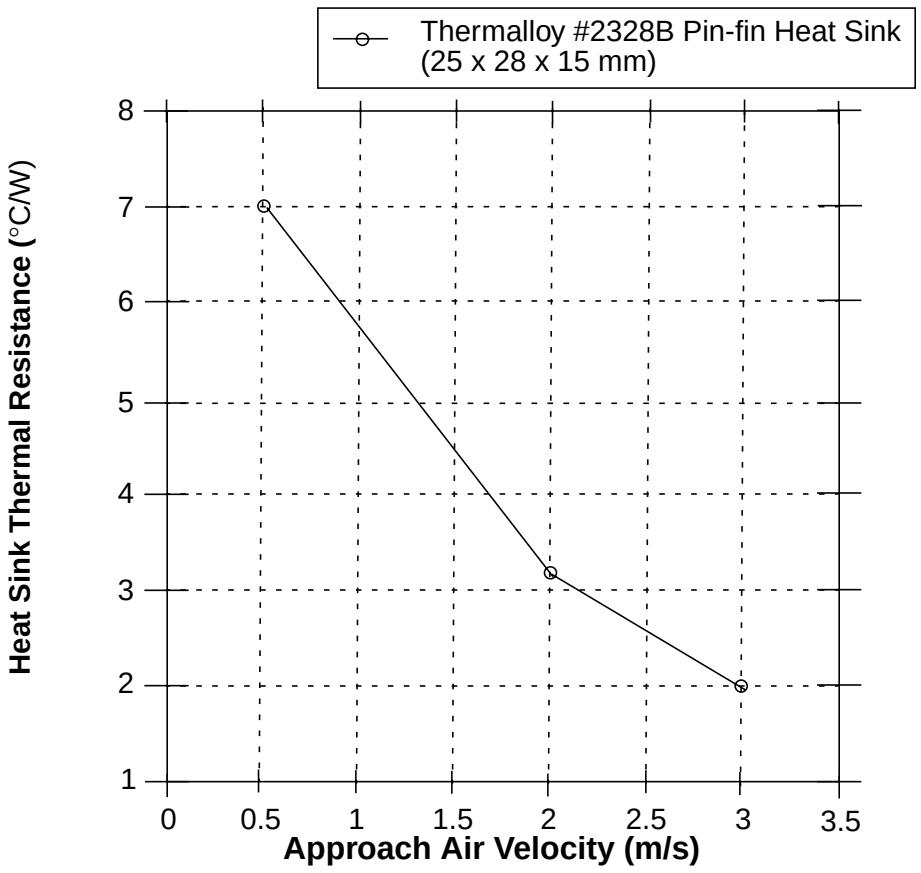


Figure 22. . Thermalloy #2328B Pin-Fin Heat Sink-to-Ambient Thermal Resistance Versus Air flow Velocity

Assuming an air velocity of 0.5 m/s, we have an effective θ_{sa} of 7 °C/W, thus

$$T_j = 30°C + 5°C + (2.2\ °C/W + 1.0°C/W + 7\ °C/W) * 4.5\ W,$$

resulting in a junction temperature of approximately 81 °C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Aavid, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can ade-

quately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include air flow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, etc.

8.0 Ordering Information

This section provides the part numbering nomenclature for the PPC740 and PPC750. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier allows for the availability of future enhanced parts (that is, lower voltage, lower power, higher performance, etc.).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

Figure 23 provides the IBM part numbering nomenclature for the PPC740 and PPC750.

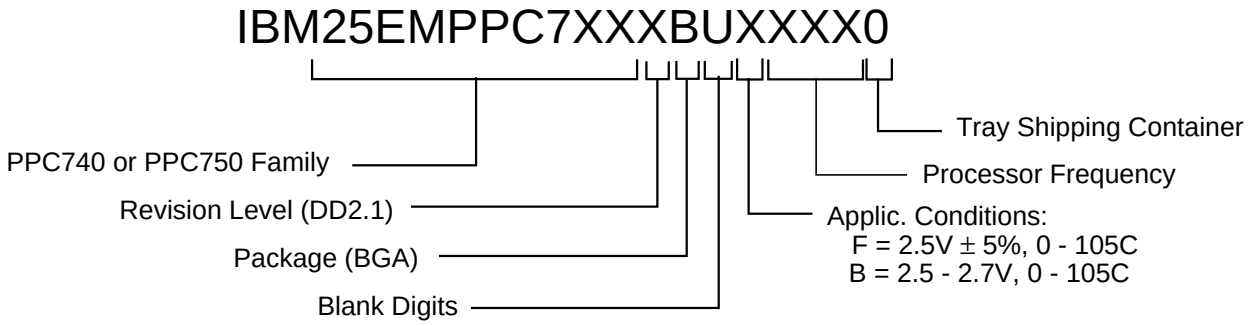


Figure 23. IBM Part Number Key

Table 19 provides a list of part descriptions.

Table 19. PPC740 and PPC750 Part Descriptions

Product Name	OEMLS Part Number	CPU Frequency	Package	PVR	DD Level
Arthur (740)	IBM25EMPPC740E BUF2000	200	21MM (255) CBGA	0X00080100	2.2
Arthur (740)	IBM25EMPPC740E BUB2330	233	21MM (255) CBGA	0X00080100	2.2

Table 19. PPC740 and PPC750 Part Descriptions (Continued)

Product Name	OEMLS Part Number	CPU Frequency	Package	PVR	DD Level
Arthur (740)	IBM25EMPPC740E BUB2660	266	21MM (255) CBGA	0X00080100	2.2
Arthur (740)	IBM25EMPPC740E BUL2660	266	21MM (255) CBGA	0X00080100	2.2
Arthur (740)	IBM25EMPPC740G BUF2000	200	21MM (255) CBGA	0X00080100	3.0
Arthur (740)	IBM25EMPPC740G BUB2330	233	21MM (255) CBGA	0X00080100	3.0
Arthur (740)	IBM25EMPPC740G BUB2660	266	21MM (255) CBGA	0X00080100	3.0
Arthur (740)	IBM25EMPPC740E BUA2660	266	21MM (255) CBGA	0X00080100	3.0
Arthur (750)	IBM25EMPPC750E BUF2000	200	51MM (360) CBGA	0X00080200	3.0
Arthur (750)	IBM25EMPPC750E BUB2330	233	51MM (360) CBGA	0X00080200	3.0
Arthur (750)	IBM25EMPPC750E BUB2660	266	51MM (360) CBGA	0X00080200	3.0
Arthur (750)	IBM25EMPPC750E BUA2660	266	51MM (360) CBGA	0X00080200	3.0

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