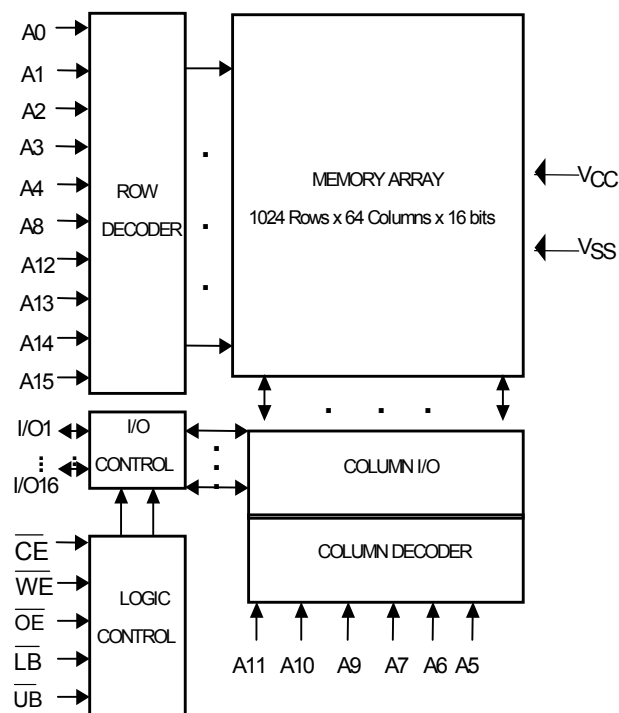


**FEATURES**

- Fast access time :
55ns(max) for Vcc=3.0V~3.6V
70/100ns(max) for Vcc=2.7V~3.6V
- CMOS Low operating power
Operating current: 45/35/25mA (Icc max)
Standby current: 20 uA(TYP.) L-version
3 uA(TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operating temperature:
Commercial : 0°C~70°C
Extended : -20°C~80°C
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage: 1.5V (min)
- Data byte control : $\overline{\text{LB}}$ (I/O1~I/O8)
 $\overline{\text{UB}}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP II
48-pin 6mm × 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM**GENERAL DESCRIPTION**

The UT62L6416 is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits.

The UT62L6416 operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L6416 is design for upper and low byte access by data byte control($\overline{\text{UB}}$ $\overline{\text{LB}}$).

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$	Lower-Byte Control
$\overline{\text{UB}}$	High-Byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection



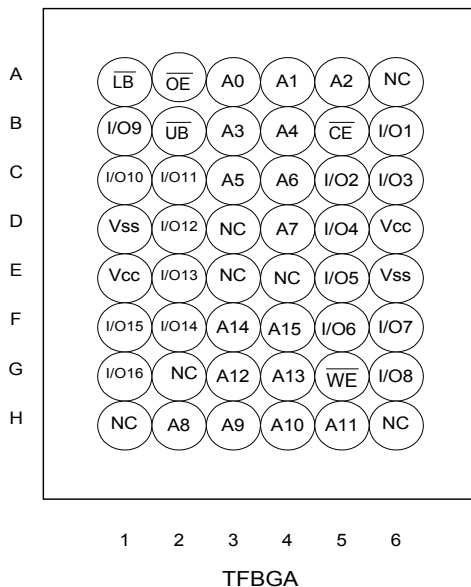
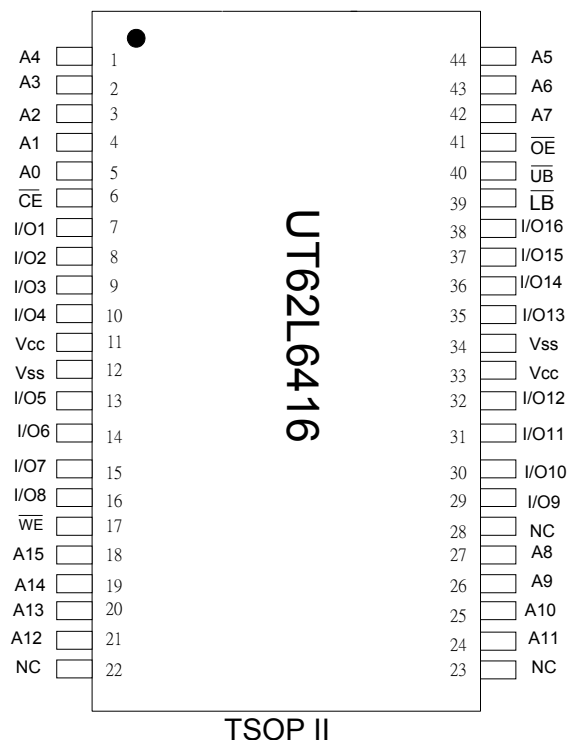
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UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High - Z	High - Z	I_{SB}, I_{SB1}
	X	X	X	H	H	High - Z	High - Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	L	X	High - Z	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	H	H	X	L	High - Z	High - Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	L	H	L	H	D_{OUT}	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	L	H	H	L	High - Z	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
	L	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	X	L	L	H	D_{IN}	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	X	L	H	L	High - Z	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}
	L	X	L	L	L	D_{IN}	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70
	Extended	T_A	-20 to 80
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = 0^\circ C$ to $70^\circ C$ / $-20^\circ C$ to $80^\circ C$ (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}		2.7	3.0	3.6	V
Input High Voltage	V_{IH}		2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}		-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_{I/O} \leq V_{CC}$; Output Disabled	-1	-	1	μA
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	-	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 2mA$	-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty, $I/O=0mA$, $\overline{CE}=V_{IL}$;	55	-	30	45
			70	-	25	35
			100	-	20	25
Average Operation Current	I_{CC1}	Cycle time= $1\mu s$, 100%duty, $I/O=0mA$, $\overline{CE} \leq 0.2V$, other pins at 0.2V or $V_{CC}-0.2V$,	-	4	5	mA
	I_{CC2}	Cycle time=500ns, 100%duty, $I/O=0mA$, $\overline{CE} \leq 0.2V$, other pins at 0.2V or $V_{CC}-0.2V$,	-	8	10	mA
Standby Current (TTL)	I_{SB}	1. $\overline{CE}=V_{IH}$, other pins = V_{IL} or V_{IH} , 2. $\overline{UB}=\overline{LB}=V_{IH}$, other pins = V_{IL} or V_{IH} ,	-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	1. $\overline{CE}=V_{CC}-0.2V$, other pins at 0.2V or $V_{CC}-0.2V$,	-L	-	20	80
		2. $\overline{UB}=\overline{LB}=V_{CC}-0.2V$, other pins at 0.2V or $V_{CC}-0.2V$,	-LL	-	3	25



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UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

CAPACITANCE (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -1mA / 2mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, TA = 0°C to 70°C / -20°C to 80°C(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L6416-55		UT62L6416-70		UT62L6416-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	100	-	ns
Address Access Time	t _{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t _{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t _{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t _{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t _{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t _{OH}	5	-	5	-	5	-	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	t _{BA}	-	55	-	70	-	100	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	t _{BHZ}	-	25	-	30	-	40	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ to Low-Z Output	t _{BLZ}	0	-	0	-	0	-	ns

(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L6416-55		UT62L6416-70		UT62L6416-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t _{WHZ*}	-	30	-	30	-	40	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Valid to End of Write	t _{BW}	45	-	60	-	80	-	ns

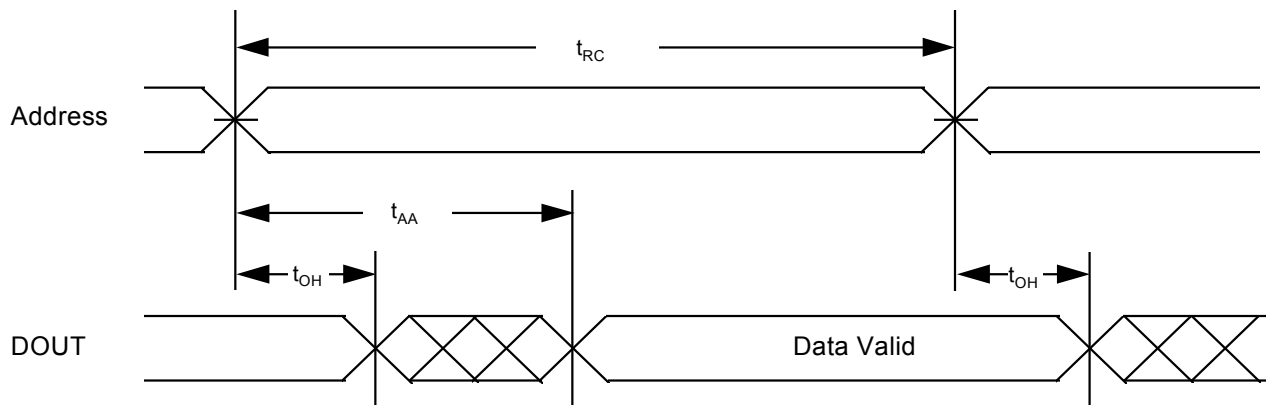
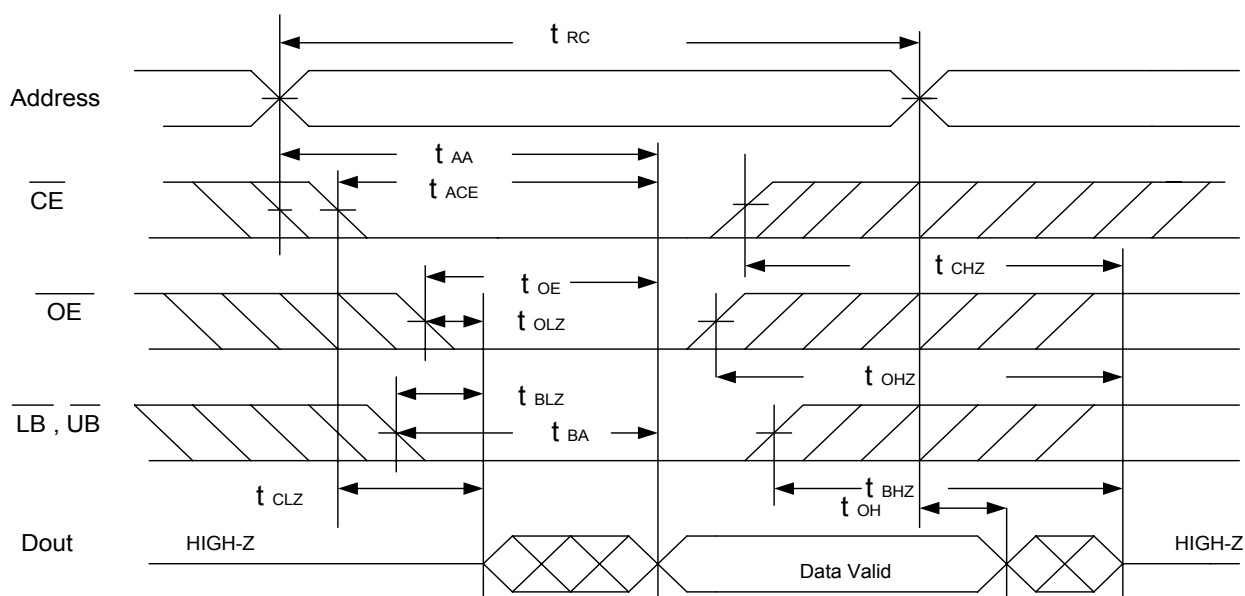
*These parameters are guaranteed by device characterization, but not production tested.

*55ns for V_{CC}=3.0V~3.6V



TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)

Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OZH} , t_{BHZ} and t_{BLZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OZH} is less than t_{OLZ} , t_{BHZ} is less than t_{BLZ} .



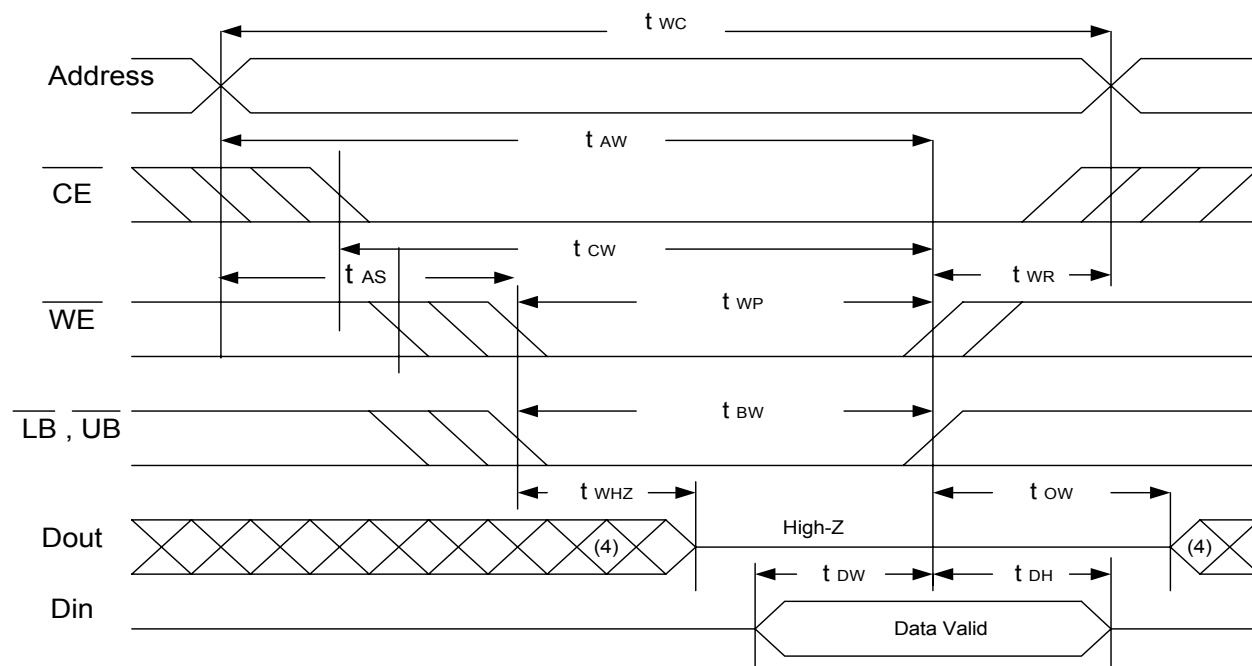
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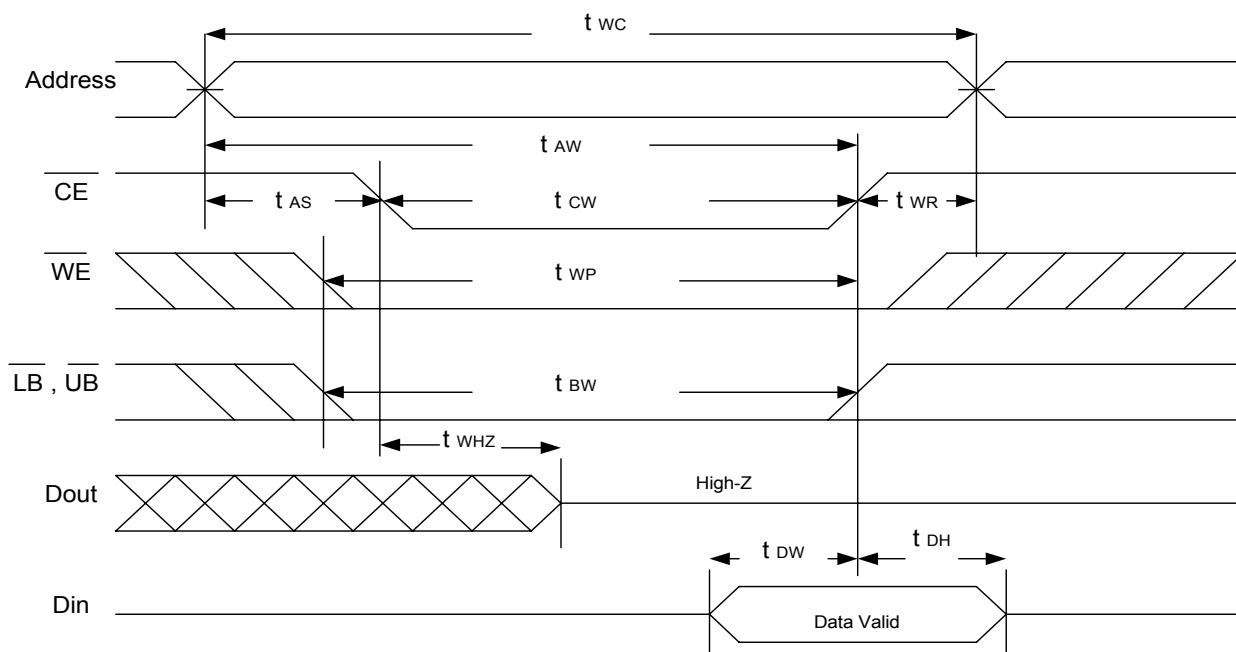
UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)

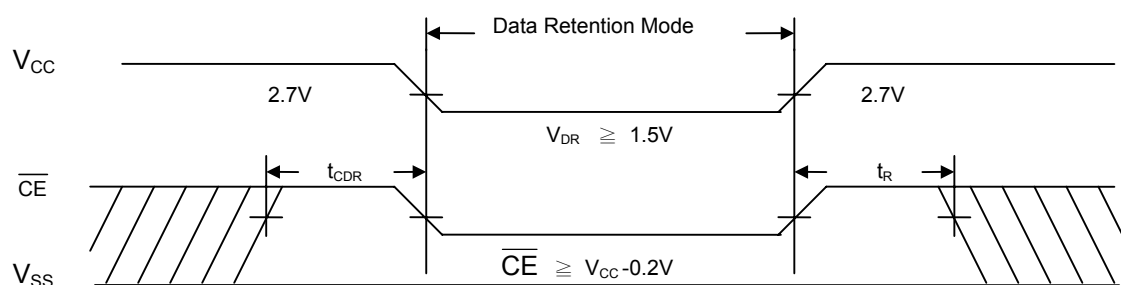


Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of $\overline{CE} = \text{low}$, $\overline{WE} = \text{low}$, $\overline{LB}$ and/or $\overline{UB} = \text{low}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

**DATA RETENTION CHARACTERISTICS** ($T_A = 0^\circ\text{C}$ to 70°C / -20°C to 80°C (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	$\overline{\text{CE}} \geq V_{\text{CC}}-0.2\text{V}$	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =1.5V	- L	-	1	μA
		$\overline{\text{CE}} \geq V_{\text{CC}}-0.2\text{V}$	- LL	-	0.5	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t _R		5	-	-	ms

DATA RETENTION WAVEFORM



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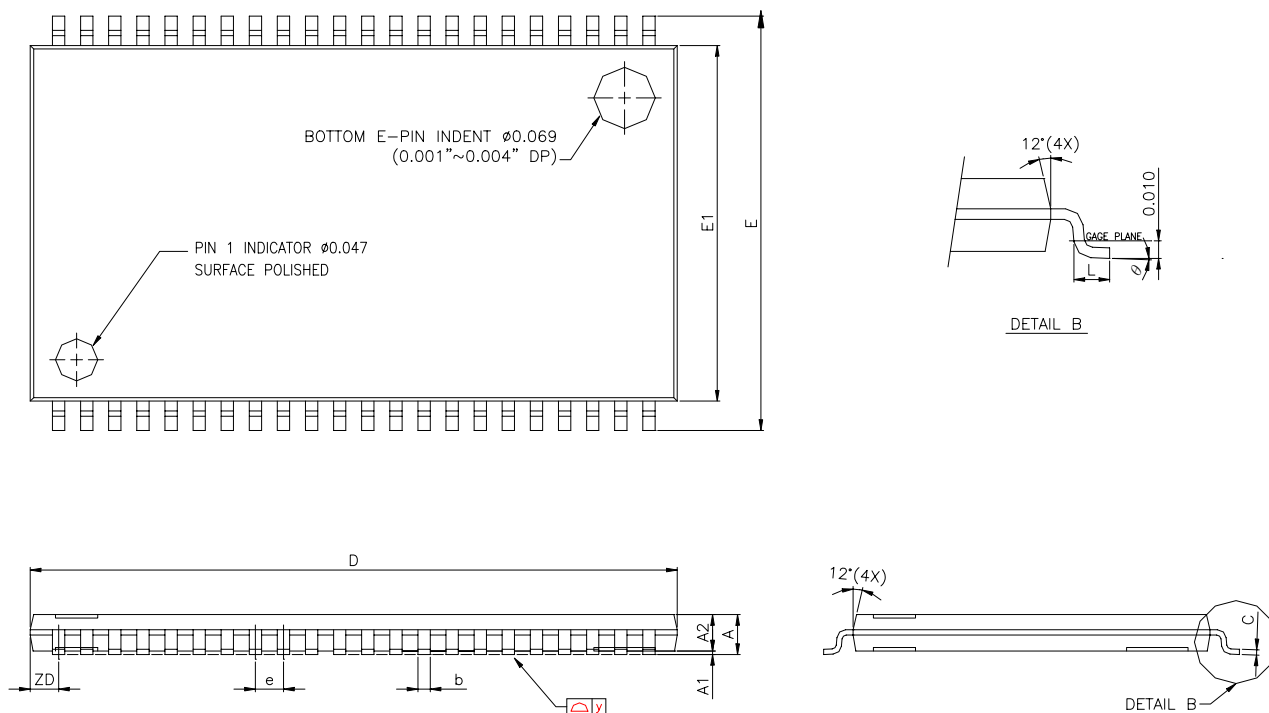
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UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

PACKAGE OUTLINE DIMENSION

44 pin 400mil TSOP-II PACKAGE OUTLINE DIMENSION



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
θ	0°	-	5°	0°	-	5°



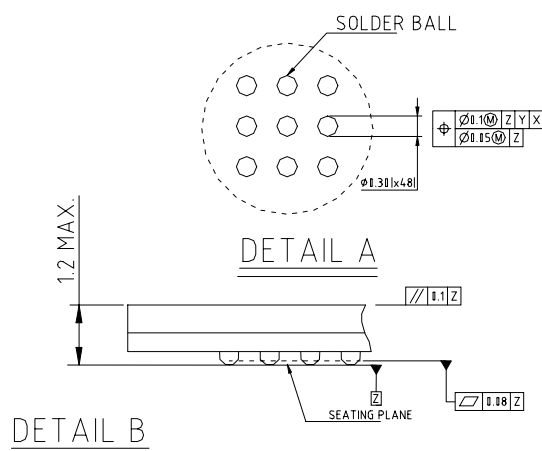
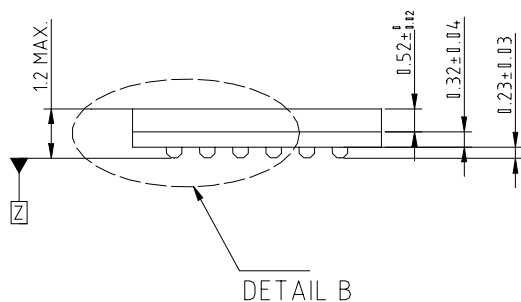
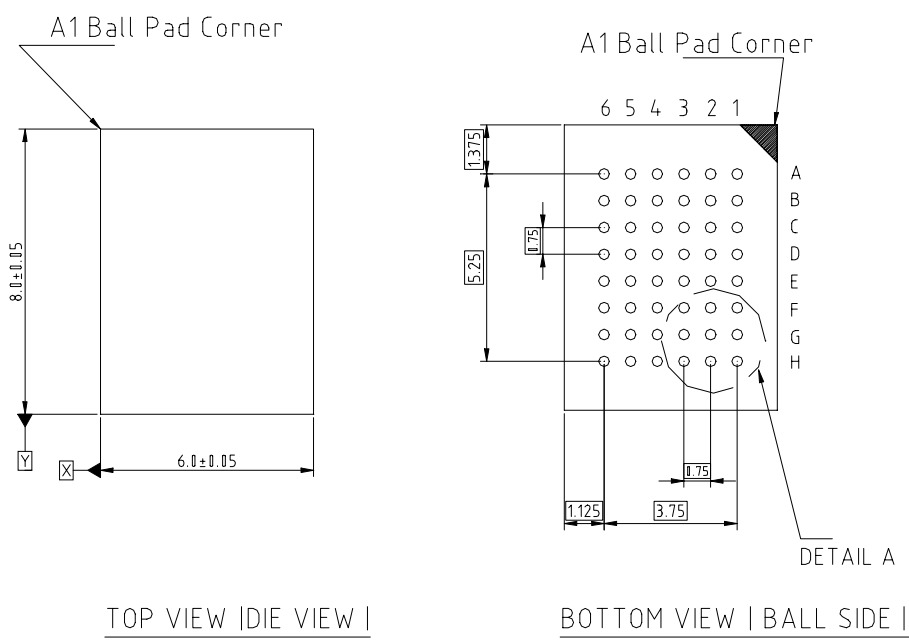
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UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

48 pin 6mm×8mm TFBGA PACKAGE OUTLINE DIMENSION



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UT62L6416**64K X 16 BIT LOW POWER CMOS SRAM****ORDERING INFORMATION****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L6416MC-55L	55	20	44 PIN TSOP- II
UT62L6416MC-55LL	55	3	44 PIN TSOP- II
UT62L6416MC-70L	70	20	44 PIN TSOP- II
UT62L6416MC-70LL	70	3	44 PIN TSOP- II
UT62L6416BS-55L	55	20	48 PIN TFBGA
UT62L6416BS-55LL	55	3	48 PIN TFBGA
UT62L6416BS-70L	70	20	48 PIN TFBGA
UT62L6416BS-70LL	70	3	48 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L6416MC-55LE	55	20	44 PIN TSOP- II
UT62L6416MC-55LLE	55	3	44 PIN TSOP- II
UT62L6416MC-70LE	70	20	44 PIN TSOP- II
UT62L6416MC-70LLE	70	3	44 PIN TSOP- II
UT62L6416BS-55LE	55	20	48 PIN TFBGA
UT62L6416BS-55LLE	55	3	48 PIN TFBGA
UT62L6416BS-70LE	70	20	48 PIN TFBGA
UT62L6416BS-70LLE	70	3	48 PIN TFBGA



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Preliminary Rev. 1.0

UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Sep 5, 2001



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Preliminary Rev. 1.0

UT62L6416

64K X 16 BIT LOW POWER CMOS SRAM

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