

## 16-Bit Registers

### Features

- Low power, pin-compatible replacement for LCX and LPT families
- 5V tolerant inputs and outputs
- 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 5.2 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250 ps
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical  $V_{olp}$  (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$
- ESD (HBM) > 2000V

### CY74FCT163H374

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors
- Devices with bus hold are not recommended for translating rail-to-rail CMOS signals to 3.3V logic levels

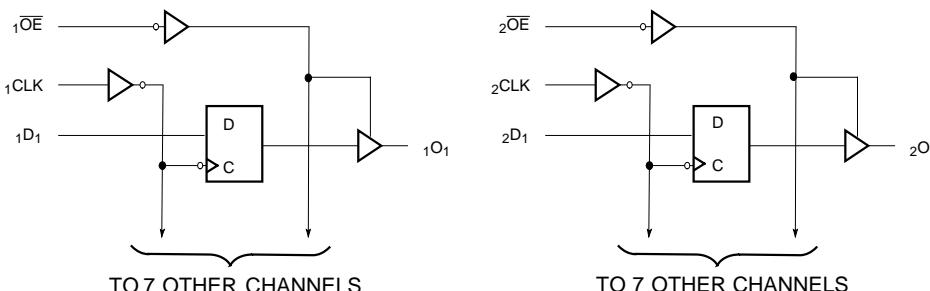
### Functional Description

These devices are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent 8-bit registers or as a single 16-bit register by connecting the output Enable ( $\overline{OE}$ ) and Clock (CLK) inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors, and provide for minimal undershoot and reduced ground bounce. Flow-through pinout and small shrink packaging aid in simplifying board layout.

The CY74FCT163H374 has "bus hold" on the data inputs, which retains the input's last state whenever the source driving the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

The CY74FCT163374 is designed with inputs and outputs capable of being driven by 5.0V buses, allowing its use in mixed voltage systems as a translator. The outputs are also designed with a power off disable feature enabling its use in applications requiring live insertion.

### Logic Block Diagrams CY74FCT163374, CY74FCT163H374



### Pin Configuration

**SSOP/TSSOP  
Top View**

	1	48	48	1
$1\overline{OE}$	1	47	1D <sub>1</sub>	
$1O_1$	2	46	1D <sub>2</sub>	
$1O_2$	3	45	GND	
GND	4	44	1D <sub>3</sub>	
$1O_3$	5	43	1D <sub>4</sub>	
$1O_4$	6	42	$V_{CC}$	
$V_{CC}$	7	41	1D <sub>5</sub>	
$1O_5$	8	40	1D <sub>6</sub>	
$1O_6$	9	39	GND	
GND	10	38	1D <sub>7</sub>	
$1O_7$	11	37	1D <sub>8</sub>	
$1O_8$	12	36	2D <sub>1</sub>	
$2O_1$	13	35	2D <sub>2</sub>	
$2O_2$	14	34	GND	
GND	15	33	2D <sub>3</sub>	
$2O_3$	16	32	2D <sub>4</sub>	
$2O_4$	17	31	$V_{CC}$	
$V_{CC}$	18	30	2D <sub>5</sub>	
$2O_5$	19	29	2D <sub>6</sub>	
$2O_6$	20	28	GND	
GND	21	27	2D <sub>7</sub>	
$2O_7$	22	26	2D <sub>8</sub>	
$2O_8$	23	25	2CLK	
$2\overline{OE}$	24			

**Function Table<sup>[1]</sup>**

Inputs			Outputs	Function
D	CLK	OE	O	
X	L	H	Z	High-Z Load Register
X	H	H	Z	
L	—	L	L	
H	—	L	H	
L	—	H	Z	
H	—	H	Z	

**Pin Description**

Name	Description
D	Data Inputs <sup>[2]</sup>
CLK	Clock Inputs
OE	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)	
Storage Temperature	—55°C to +125°C
Ambient Temperature with Power Applied	—55°C to +125°C
Supply Voltage Range	0.5V to +4.6V
DC Input Voltage	—0.5V to +7.0V
DC Output Voltage	—0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	—60 to +120 mA
Power Dissipation	1.0W

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	—40°C to +85°C	2.7V to 3.6V

**Electrical Characteristics for Non Bus Hold Devices** Over the Operating Range V<sub>CC</sub>=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit	
V <sub>IH</sub>	Input HIGH Voltage	All Inputs	2.0		5.5	V	
V <sub>IL</sub>	Input LOW Voltage				0.8	V	
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV	
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =—18 mA		—0.7	—1.2	V	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =5.5			±1	µA	
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	µA	
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =5.5V			±1	µA	
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND			±1	µA	
I <sub>OS</sub>	Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	—60	—135	—240	mA	
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V			±100	µA	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> —0.2V	V <sub>CC</sub> =Max.		0.1	10	µA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>IN</sub> =V <sub>CC</sub> —0.6V <sup>[8]</sup>	V <sub>CC</sub> =Max.		2.0	30	µA

**Notes:**

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. — = LOW-to-HIGH Transition.
2. On the CY74FCT163H374, these pins have "bus hold."
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
5. Typical values are at V<sub>CC</sub>=3.3V, T<sub>A</sub> = +25°C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
8. Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.

**Electrical Characteristics For Bus Hold Devices** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$ 

Parameter	Description	Test Conditions		Min.	Typ. <sup>[5]</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	All Inputs		2.0		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage					0.8	V
$V_H$	Input Hysteresis <sup>[6]</sup>				100		mV
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$		-0.7	-1.2	V	
$I_{IH}$	Input HIGH Current	$V_{CC}=\text{Max.}, V_I=V_{CC}$			$\pm 100$	$\mu A$	
$I_{IL}$	Input LOW Current					$\pm 100$	$\mu A$
$I_{BBH}$ $I_{BBL}$	Bus Hold Sustain Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Min.}$	$V_I=2.0V$	-50			$\mu A$
			$V_I=0.8V$	+50			$\mu A$
$I_{BHHO}$ $I_{BHLO}$	Bus Hold Overdrive Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Max.}, V_I=1.5V$				$\pm 500$	$\mu A$
$I_{OZH}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=V_{CC}$				$\pm 1$	$\mu A$
$I_{OZL}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$				$\pm 1$	$\mu A$
$I_{OS}$	Short Circuit Current <sup>[7]</sup>	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$		-60	-135	-240	mA
$I_{OFF}$	Power-Off Disable	$V_{CC}=0V, V_{OUT}\leq 4.5V$				$\pm 100$	$\mu A$
$I_{CC}$	Quiescent Power Supply Current	$V_{IN}\leq 0.2V$	$V_{CC}=\text{Max.}$			+40	$\mu A$
$\Delta I_{CC}$	Quiescent Power supply Current (TTL inputs HIGH)	$V_{IN}=V_{CC}-0.6V$ <sup>[8]</sup>	$V_{CC}=\text{Max.}$			+350	$\mu A$

**Electrical Characteristics For Balanced Drive Devices** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$ 

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$I_{ODL}$	Output LOW Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	45		110	mA
$I_{ODH}$	Output HIGH Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-45		-110	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=\text{Min.}, I_{OH}=-8\text{ mA}$	2.4 <sup>[10]</sup>	3.0		V
		$V_{CC}=3.0V, I_{OH}=-24\text{ mA}$	2.0	3.0		V
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=0.1mA$			0.2	V
		$V_{CC}=\text{Min.}, I_{OL}=24\text{ mA}$		0.3	0.55	

**Notes:**

9. Pins with bus hold are described in Pin Description.  
 10.  $V_{OH}=V_{CC}-0.6V$  at rated current.

**Capacitance<sup>[6]</sup>** ( $T_A = +25^\circ C$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

## Power Supply Characteristics

Parameter	Description	Test Conditions		Typ [5]	Max.	Unit
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC}$ =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\bar{OE}$ =GND	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	50	75	$\mu A/MHz$
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC}$ =Max., $f_1=10$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\bar{OE}$ =GND	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	0.5	0.8	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=GND$	0.5	0.8	mA
		$V_{CC}$ =Max., $f_1=2.5$ MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\bar{OE}$ =GND	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	2.0	3.0 <sup>[13]</sup>	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=GND$	2.0	3.3 <sup>[13]</sup>	mA

## Switching Characteristics Over the Operating Range $V_{CC}=3.0V$ to $3.6V$ <sup>[14,15]</sup>

Parameter	Description	CY74FCT163374A CY74FCT163H374A		CY74FCT163374C CY74FCT163H374C		Unit	Fig. No. <sup>[16]</sup>
		Min.	Max.	Min.	Max.		
$t_{PLH}$	Propagation Delay Clock to Output	1.5	6.5	1.5	5.2	ns	1, 3
$t_{PHL}$							
$t_{PZH}$	Output Enable Time	1.5	6.5	1.5	5.5	ns	1, 7, 8
$t_{PZL}$							
$t_{PHZ}$	Output Disable Time	1.5	5.5	1.5	5.0	ns	1, 7, 8
$t_{PLZ}$							
$t_{SU}$	Input Setup time	2.0		2.0		ns	1, 4
$t_H$	Input Hold time	1.5	-	1.5	-	ns	1. 4
$t_{SK(O)}$	Output Skew <sup>[17]</sup>		0.5		0.5	ns	—

### Notes:

11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in millamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.
14. Minimum limits are specified but not tested on Propagation Delays.
15. For  $V_{CC}=2.7$ , propagation delay, output enable and output disable times should be degraded by 20%.
16. See "Parameter Measurement Information" in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Switching Characteristics** Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V^{[14,15]}$ 

Parameter	Description	CY74FCT163LD374 <sup>[18]</sup> CY74FCT163LDH374		CY74FCT163LD374A <sup>[18]</sup> CY74FCT163LDH374A		Unit	Fig. No. <sup>[16]</sup>
		Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Q Output	1.5	10	1.5	6.5	ns	1, 3
$t_{PZH}$ $t_{PZL}$	Output Enable Time	1.5	12.5	1.5	6.5	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	1.5	8.0	1.5	5.5	ns	1, 7, 8
$t_{SU}$	Input Setup time	2.0		2.0		ns	1, 4
$t_H$	Input Hold time	1.5		1.5		ns	1, 4
$t_{SK(O)}$	Output Skew <sup>[17]</sup>		0.5		0.5	ns	—

**Note:**

18. For Lite Drive devices the load capacitance is 30 pF. For all others it is 50 pF.

**Ordering Information CY74FCT163374**

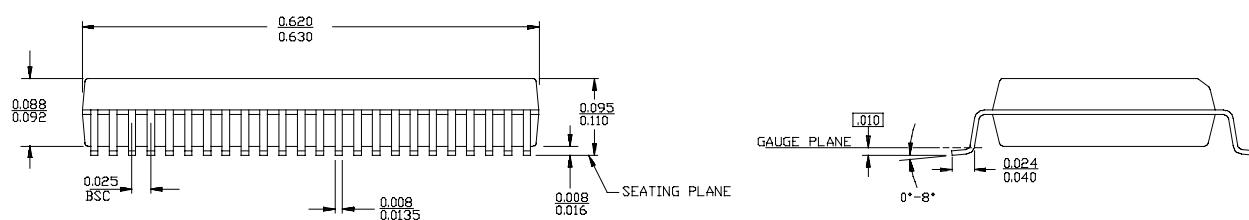
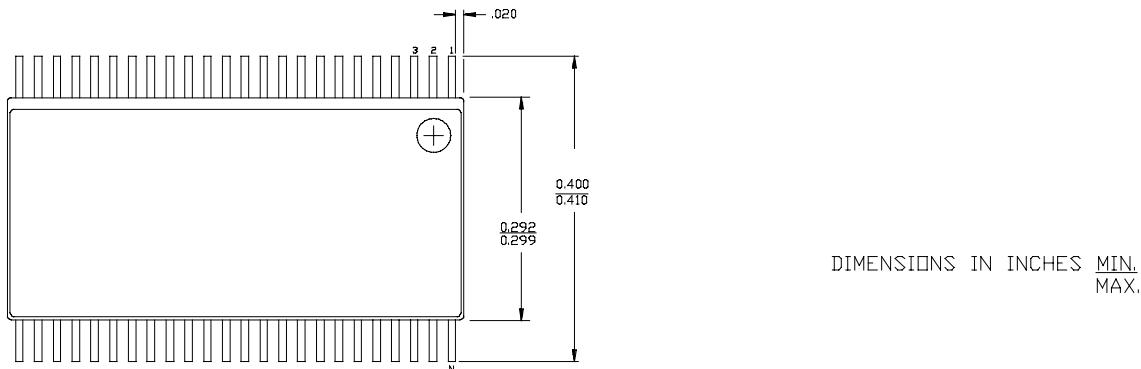
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT163374CPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163374CPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163374APACT	Z48	48-Lead (240-Mil) TSSOP	Industrial

**Ordering Information CY74FCT163H374**

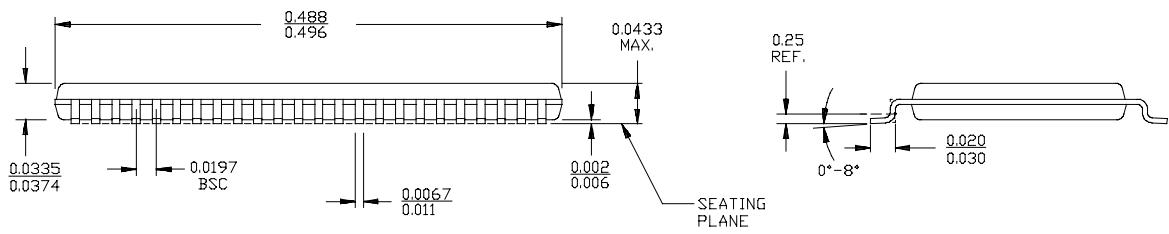
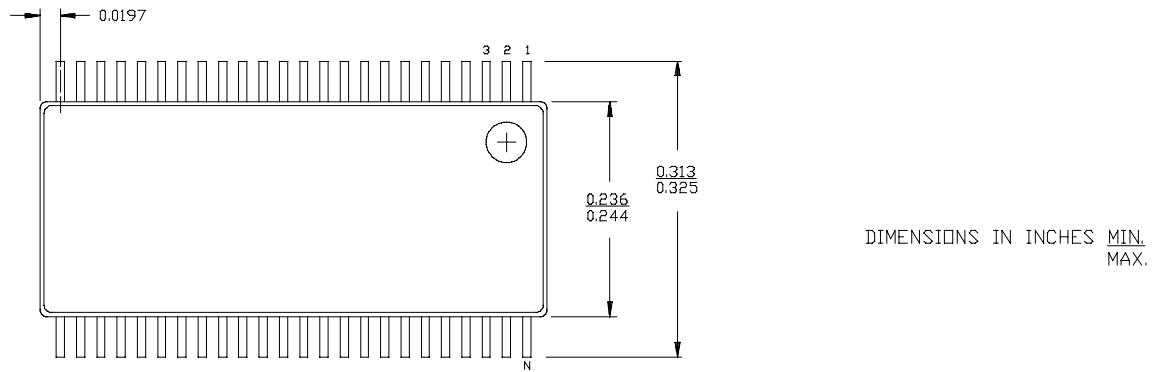
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	74FCT163H374CPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H374CPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT163H374CPVCT	O48	48-Lead (300-Mil) SSOP	

## Package Diagrams

## 48-Lead Shrunk Small Outline Package O48



## 48-Lead Thin Shrunk Small Outline Package Z48



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