FemtoClock® Crystal-to-3.3V, 2.5V LVPECL Clock Generator

843071

DATA SHEET

General Description

The 843071 is a Serial ATA (SATA)/Serial Attached SCSI (SAS) Clock Generator. The 843071 uses an 18pF parallel resonant crystal over the range of 20.833MHz - 28.3MHz. For SATA/SAS applications, a 25MHz crystal is used and either 75MHz or 150MHz may be selected with the FREQ_SEL pin. For 10Gb Fibre Channel applications, a 26.5625MHz crystal is used for 159.375MHz output. The 843071 has excellent <1ps phase jitter performance, over the 12kHz - 20MHz integration range. The 843071 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

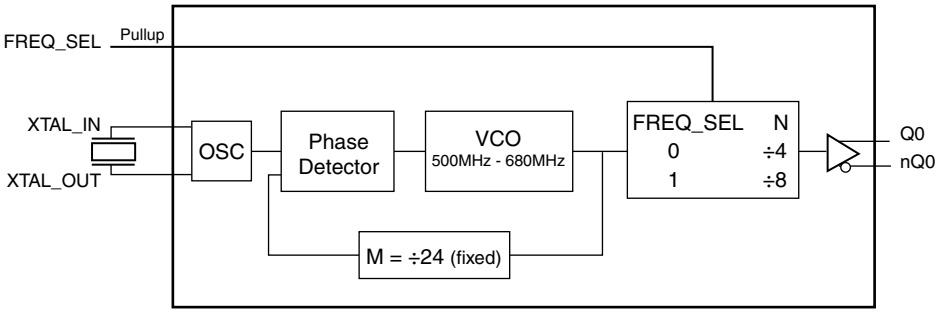
Features

- One differential 3.3V or 2.5V LVPECL output
- Crystal oscillator interface,18pF parallel resonant crystal (20.833MHz – 28.3MHz)
- Output frequency range: 62.5MHz – 170MHz
- VCO range: 500MHz – 680MHz
- RMS phase jitter at 150MHz, using a 25MHz crystal (12kHz – 20MHz): 0.64ps (typical) @ 3.3V output
- RMS phase jitter at 159.375MHz, using a 26.5625MHz crystal (1.875MHz – 20MHz): 0.40ps (typical) @ 3.3V output
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

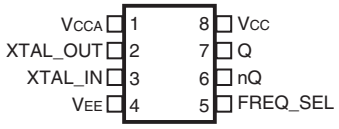
Common Configuration Table - Serial ATA/Serial Attached SCSI

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	0	24	4	6	150
25	1	24	8	3	75
26.5625	0	24	4	6	159.375

Block Diagram



Pin Assignment



843071
8 Lead TSSOP
4.40mm x 3.0mm package body

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2, 3	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V_{EE}	Power		Negative supply pin.
5	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 10\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.0	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		3.0	3.3	3.63	V
I_{CC}	Power Supply Current				96	mA
I_{CCA}	Analog Supply Current				12	mA
I_{EE}	Power Supply Current				72	mA

Table 3B. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current				72	mA
I_{CCA}	Analog Supply Current				12	mA
I_{EE}	Power Supply Current				72	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 10\%$, $2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	3.3V	2		V_{CC} + 0.3	V
		2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	3.3V	-0.3		0.8	V
		2.5V	-0.3		0.7	V
I_{IH}	Input High Current	$V_{CC} = V_{IN} = 3.63V$ or 2.625V			5	µA
I_{IL}	Input Low Current	$V_{CC} = 3.63V$ or 2.625V, $V_{IN} = 0V$	-150			µA

Table 3D. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 10\%, 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		20.833		28.3	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		170	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 12kHz – 20MHz		0.64		ps
		75MHz, Integration Range: 12kHz – 20MHz		0.64		ps
		159.375MHz, Integration Range: 1.875MHz – 20MHz		0.40		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle		48		52	%

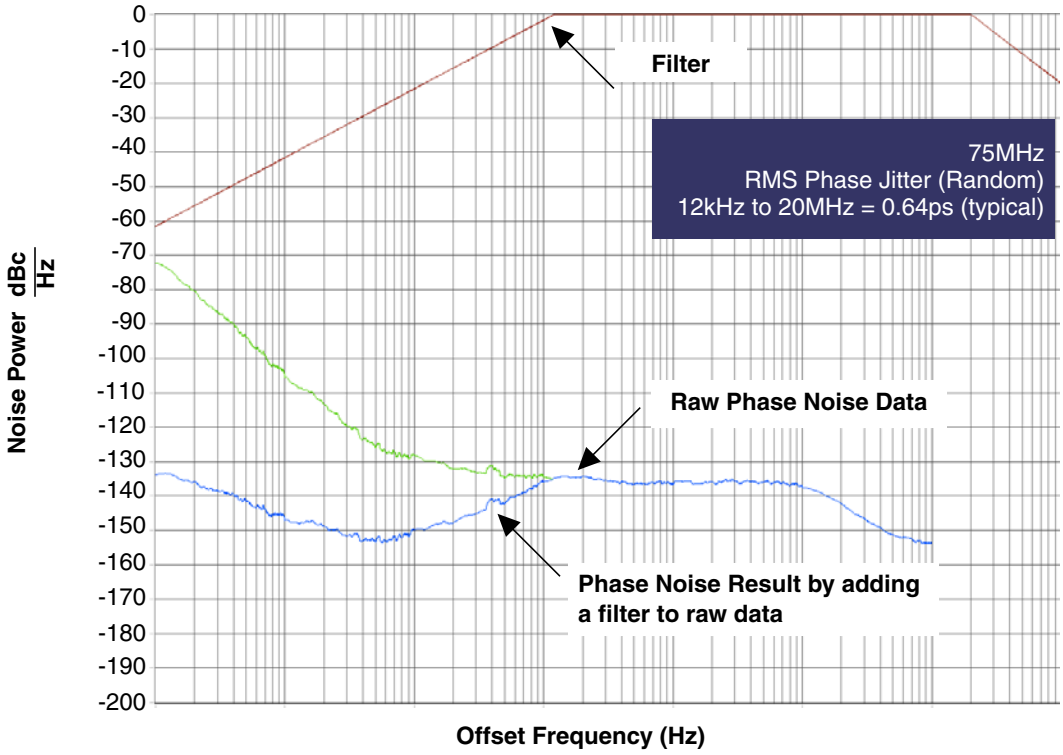
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

Table 5B. AC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

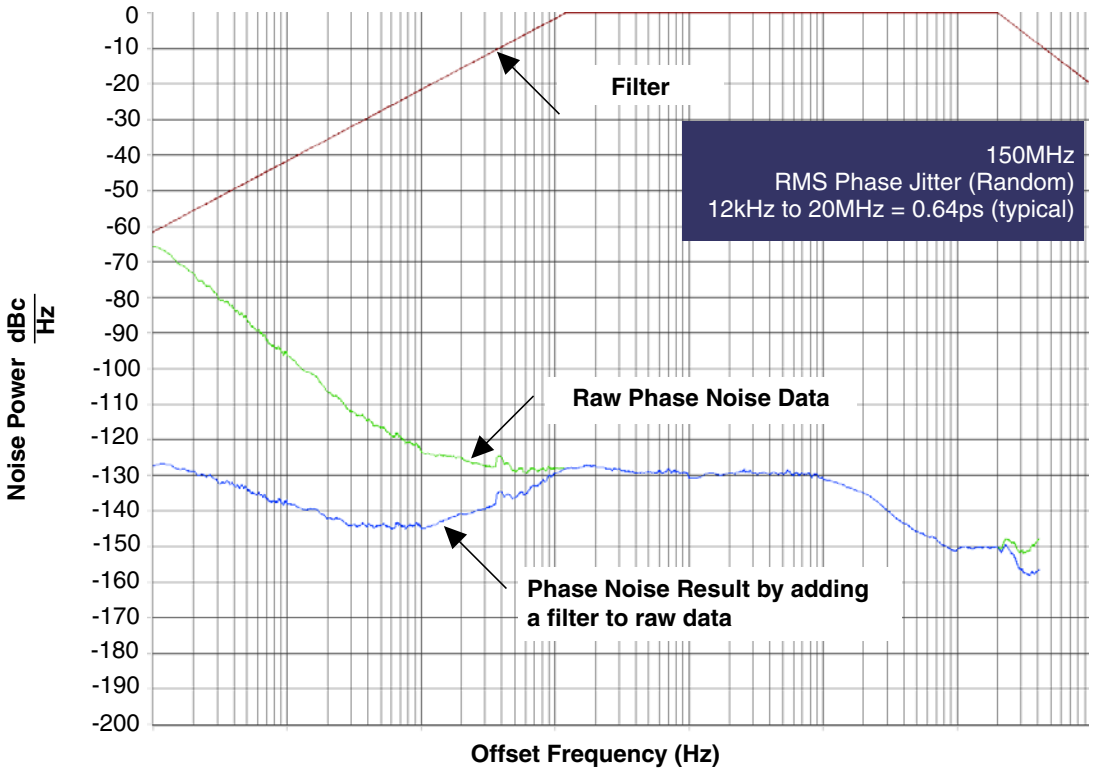
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		62.5		170	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	150MHz, Integration Range: 12kHz – 20MHz		0.94		ps
		75MHz, Integration Range: 12kHz – 20MHz		0.80		ps
		159.375MHz, Integration Range: 1.875MHz – 20MHz		0.42		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

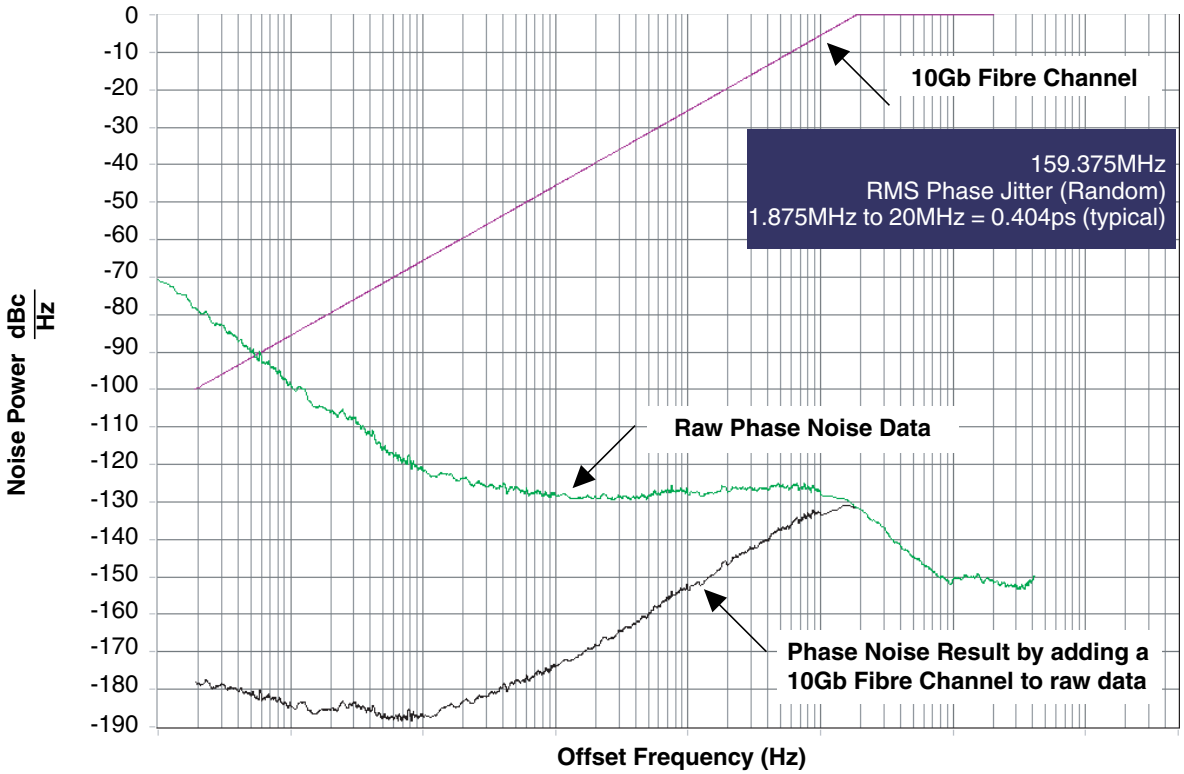
Typical Phase Noise at 75MHz (3.3V)



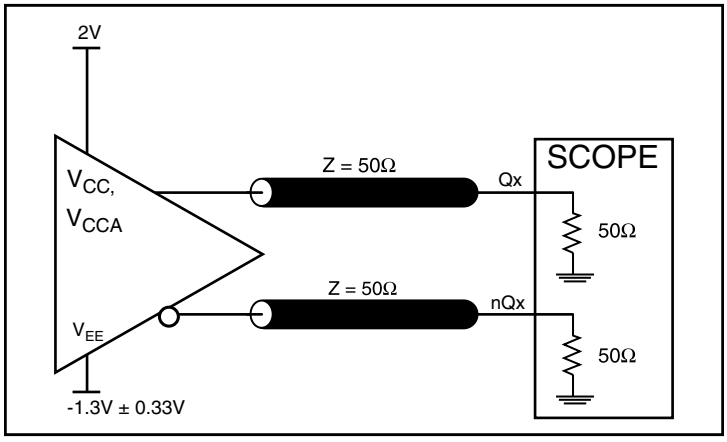
Typical Phase Noise at 150MHz (3.3V)



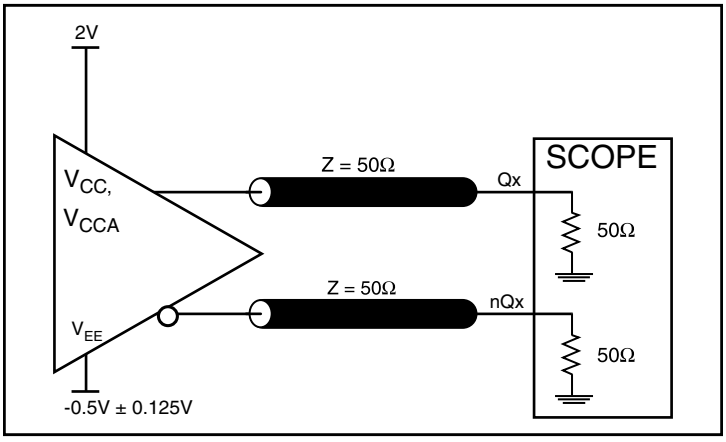
Typical Phase Noise at 159.375MHz (3.3V)



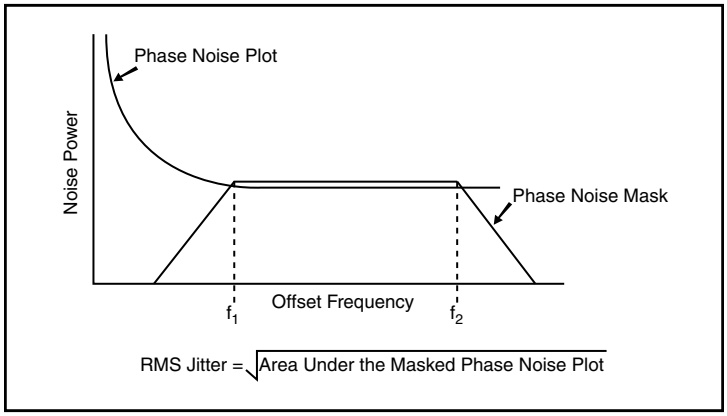
Parameter Measurement Information



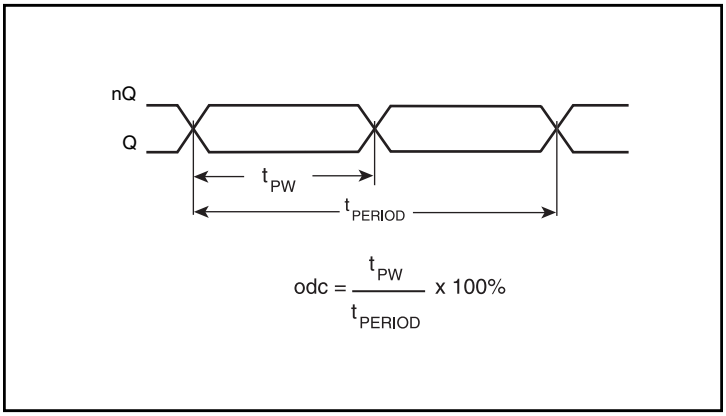
3.3V LVPECL Output Load AC Test Circuit



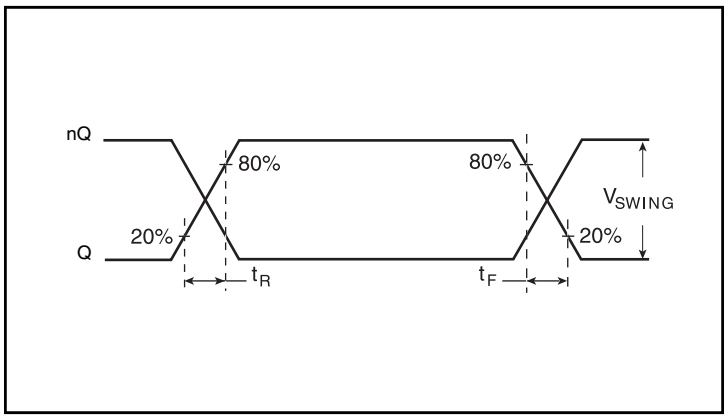
2.5V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843071 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

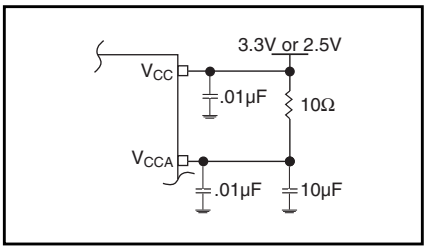


Figure 1. Power Supply Filtering

Crystal Input Interface

The 843071 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

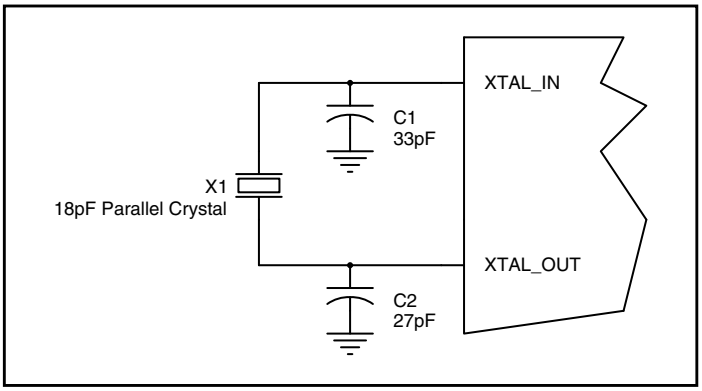


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

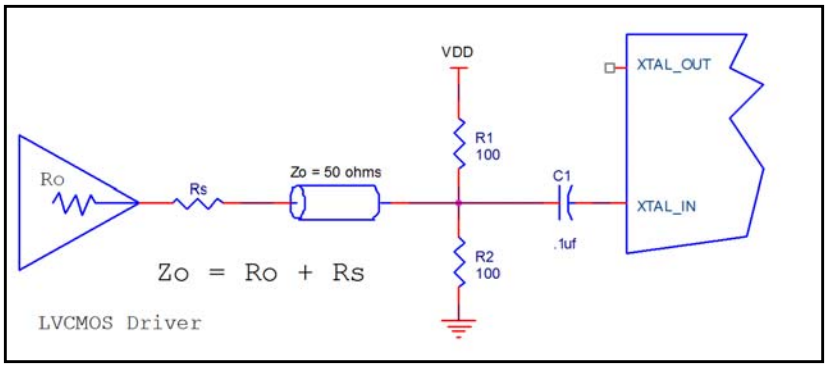


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

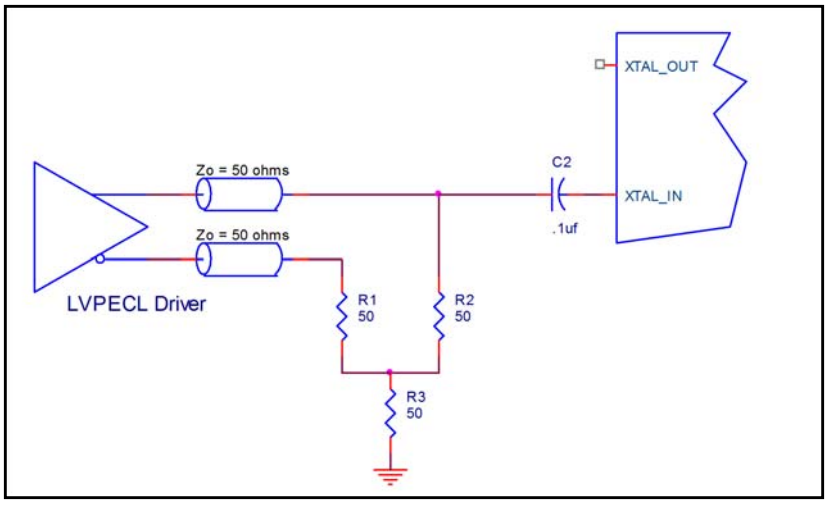


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

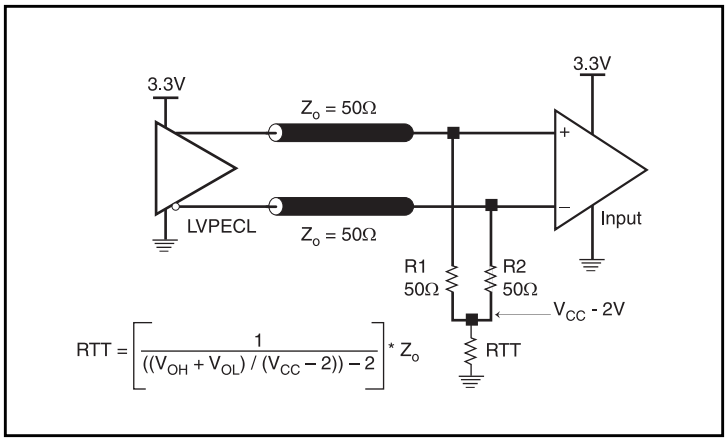


Figure 4A. 3.3V LVPECL Output Termination

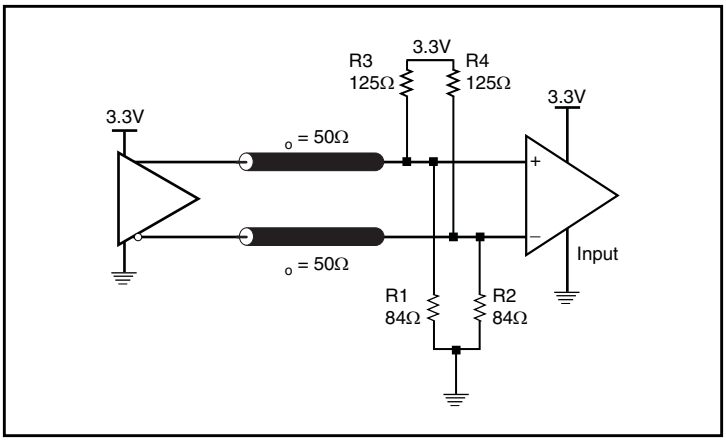


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

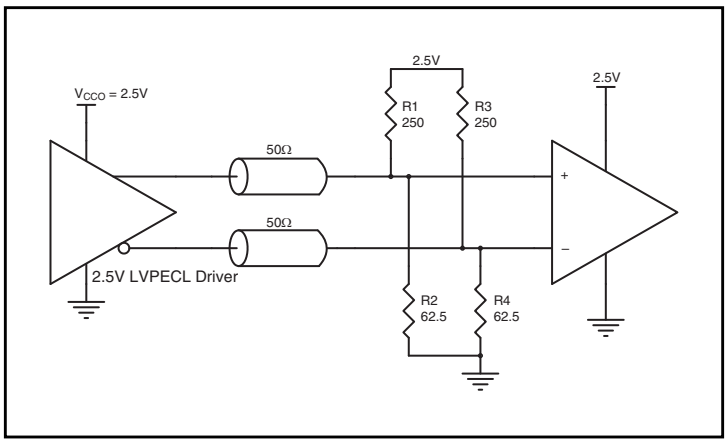


Figure 5A. 2.5V LVPECL Driver Termination Example

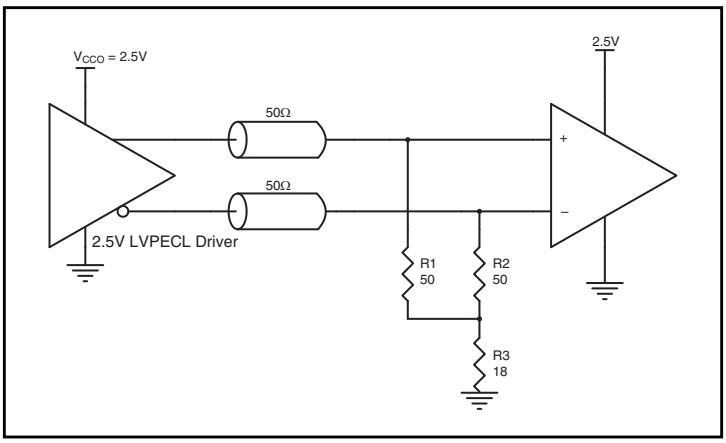


Figure 5B. 2.5V LVPECL Driver Termination Example

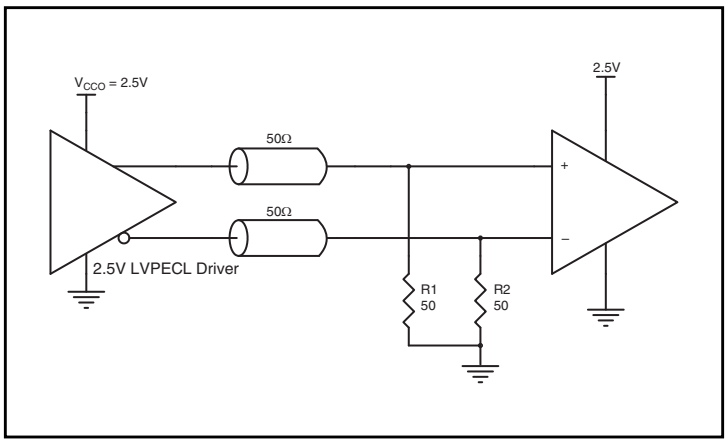


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Layout

Figure 6 shows an example of 843071 application schematic. In this example, the device is operated $V_{CC} = V_{CCA} = 3.3V$. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 33pF and C2 = 27pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843071 provides separate power supplies to isolate noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required,

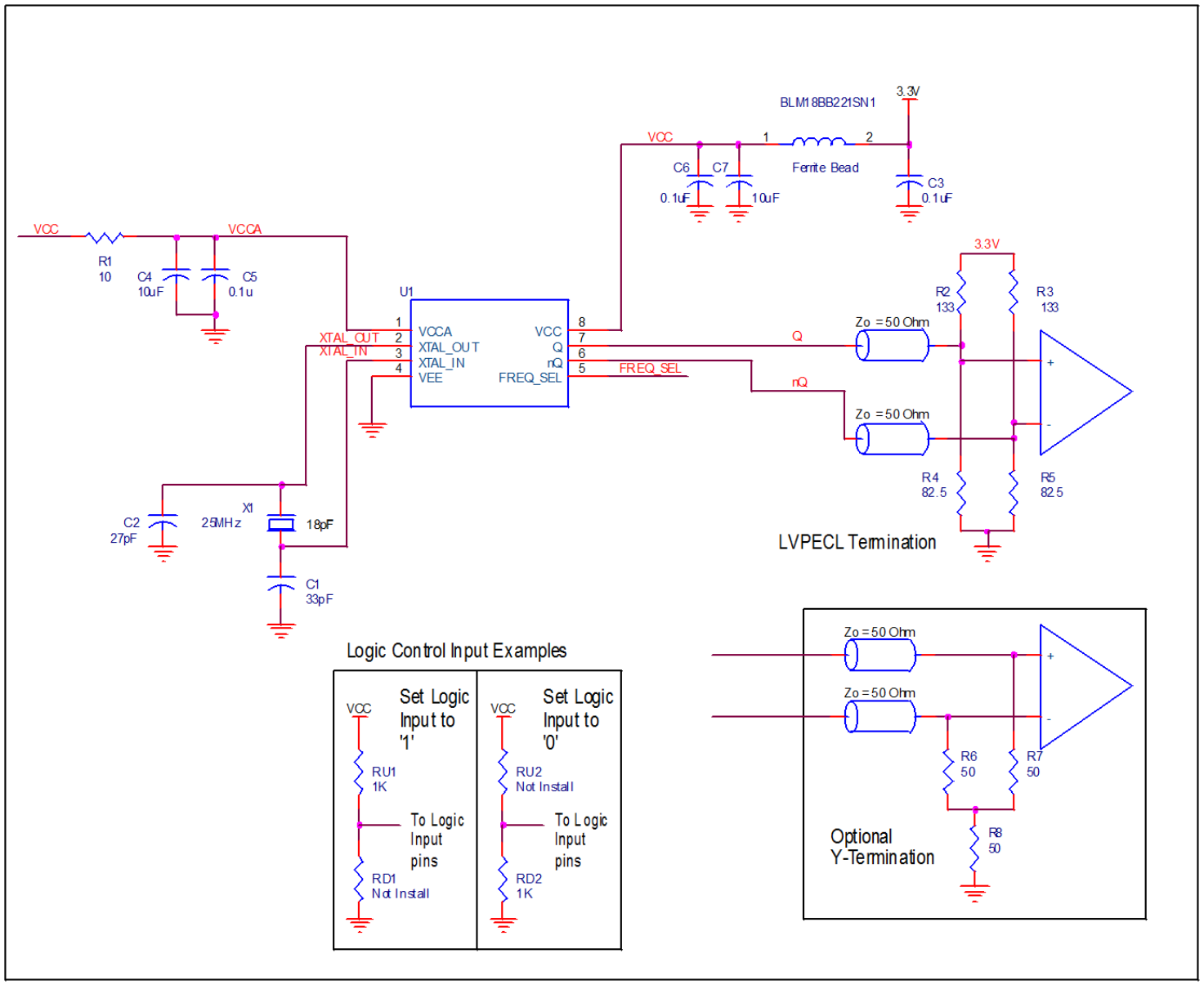


Figure 6. 843071 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 843071.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843071 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 96mA = **348.5mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.63V, with all outputs switching) = 348.55mW + 30mW = **378.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.379W * 90.5°C/W = 119.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

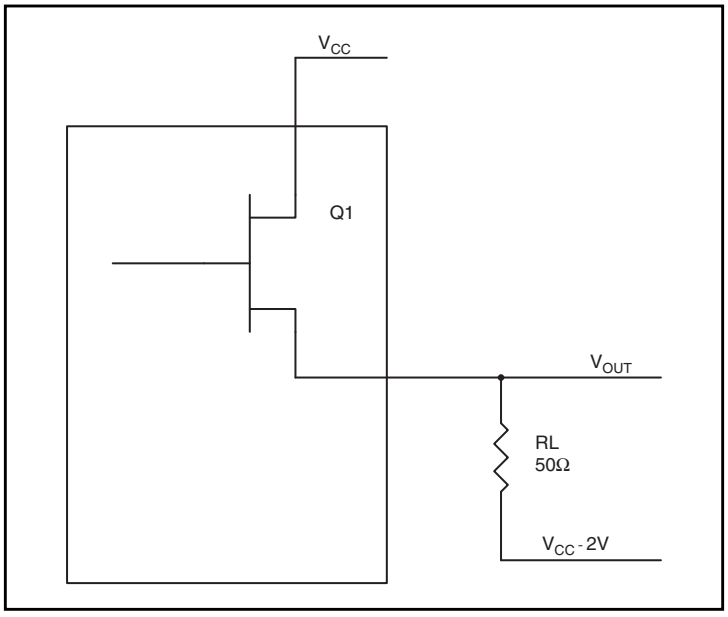


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Transistor Count

The transistor count for 843071 is: 1732

Package Outline and Package Dimension

Package Outline - G Suffix for 8 Lead TSSOP

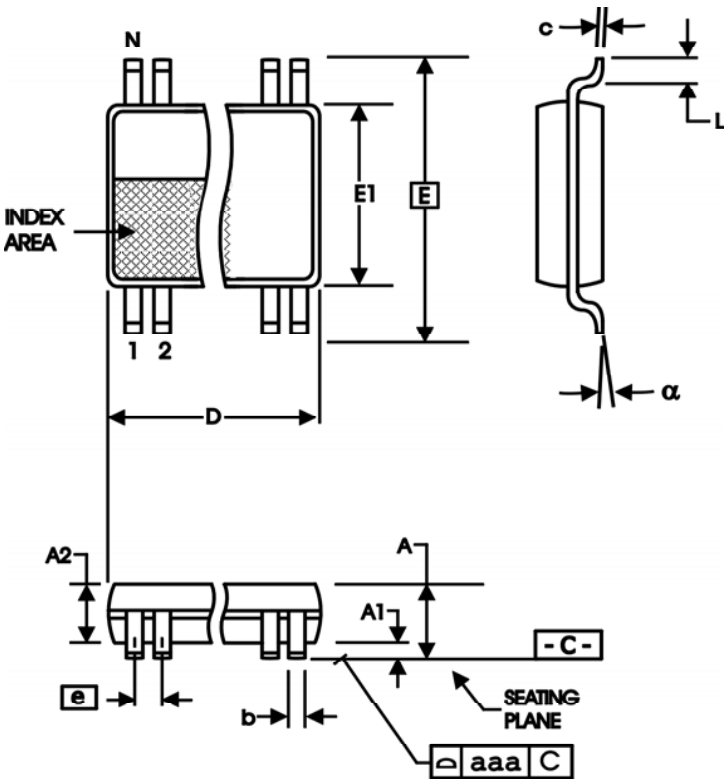


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843071AGILF	71AIL	8 Lead TSSOP, Lead-Free	Tube	-40°C to 85°C
843071AGILFT	71AIL	8 Lead TSSOP, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	15	Ordering Information Table - added lead-free marking.	4/10/06
B	T3C	3	2.5V Power Supply Table - Changed 2.5V±10% to 2.5V±5%. V_{CC} & V_{CCA} - changed 2.25V min./2.75V max. to 2.375V min./2.625V max. Corrected 2.5V throughout the datasheet.	6/11/07
		8	Crystal Input Interface - changed C1/C2 capacitor values from 22p/22p to 27p/33p.	
		9	Added *LVCMOS to XTAL Interface* section.	
	T9	14	Ordering Information Table - corrected standard marking from 3071A to 071AI.	
B	T3D	4	LVPECL DC Characteristics Table - corrected V_{OH}/V_{OL} parameters from “Current” to “Voltage” and units from "µA" to "V".	10/13/10
	T5A, T5B	4	AC Characteristics Table - added thermal note.	
		8	Updated text in Power Supply Filtering Techniques section.	
		9	Updated “Overdriving the Crystal Interface” section. Updated header/footer.	
B		12	Added schematic	11/9/12
C			Updated header/footer throughout the datasheet. Deleted *IDT* prefix and “I” suffix from part number.	10/19/15
		1	Features Section - deleted leaded information in the last bullet.	
		1	Added outline box around Block Diagram.	
		9	Updated *Overdriving the XTAL Interface* application note.	
	T9	16	Ordering Information table - deleted leaded parts rows and note.	

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