Nuvoton
PCI TO ISA BRIDGE

W83628AG
W83629AG

Revision: 1.2
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W83628AG & W83629AG Datasheet Revision History

	PAGES	DATES	VERSION	MAIN CONTENTS
1	N.A.	07/30/2007	0.5	1. First published version.
2	34, 38	08/02/2007	0.51	1. Update the information of Chapter 10 Absolute Maximum Ratings. 2. Modify the description of Chapter 12 AC Characteristics.
3	N.A.	11/01/2007	1.0	1. All versions before 1.0 are preliminary versions.
4	1	11/28/2007	1.1	1. Add the ordering information
5	11	31/1/2008	1.2	1. Modify DC characteristics

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

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1. GENERAL DESCRIPTION

The W83628AG is a PCI-to-ISA bus conversion IC. The W83629AG is a condensed centralizer IC for IRQ and DMA control. W83628AG and W83629AG together form a complete set for the PCI-to-ISA bridge.

For the new generation Intel chipsets featuring LPC bus but not supporting ISA bus and slots, the W83628AG plus the W83629AG are the best companion solution for the non-ISA chipset. Also the packages of the W83628AG (128-QFP) and the W83629AG (48-LQFP) are the most cost-effective solution that minimizes the M/B board layout size and cost.

For the new generation chipsets featuring LPC interface but not supporting ISA bus, the best and the most complete solution will be the combination of the W83627 (Nuvoton LPC I/O) family and the set of the W83628AG and the W83629AG.

2. FEATURES

PCI to ISA Bridge

- Full ISA Bus Support, including ISA Masters
- 5V ISA and 3.3V PCI interfaces
- PC/PCI DMA protocol for Software Transparent
- IRQ Serializer for ISA Parallel IRQ transfer to Serial IRQ
- Supports 3 fully ISA Compatible Slots without Buffering
- PCI Bus at 25MHz, 33MHz and up to 40MHz
- Supports Programmable ISA Bus Divide the PCI Bus Clock into 3 or 4
- All ISA Signals can be Isolated
- Supports Configuration registers for performance programming

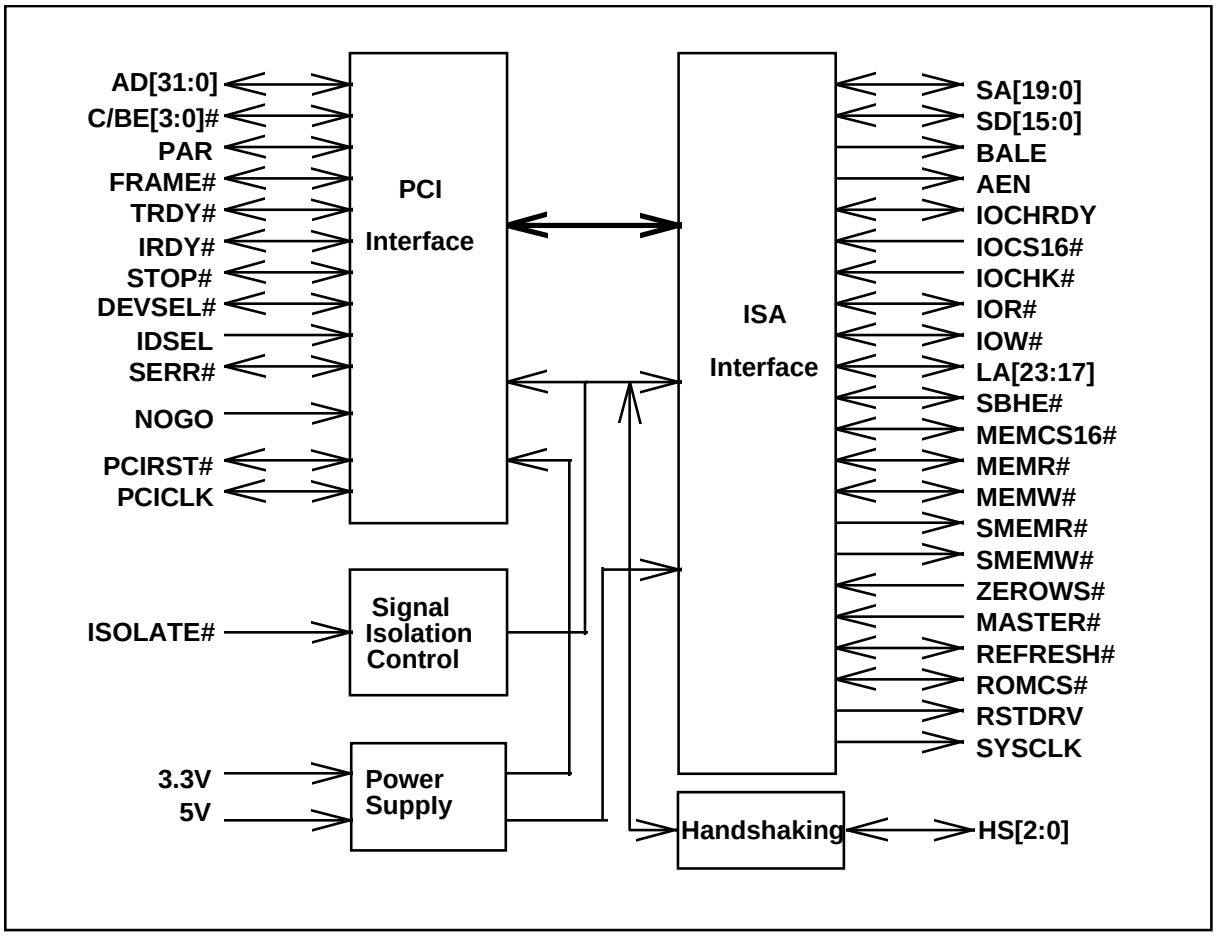
3. PACKAGE

- 128-pin QFP for the W83628AG
- 48-pin LQFP for the W83629AG

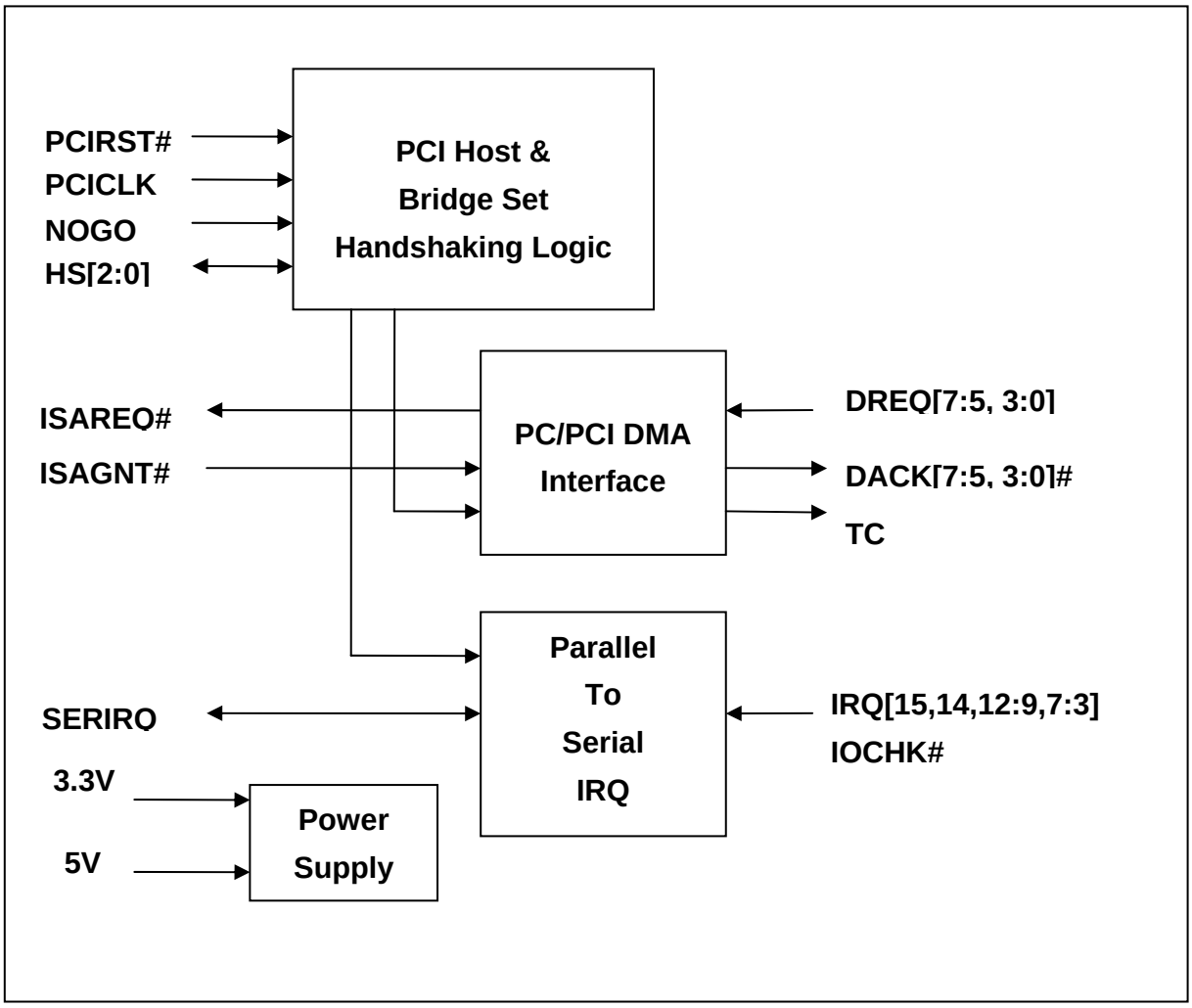
4. ORDERING INFORMATION

PART NUMBER	DESCRIPTION	PRODUCTION FLOW
W83628AG	**128-PIN QFP, Pb-free**	**Commercial, 0°C to +70°C**
W83629AG	**48-PIN LQFP, Pb-free**	**Commercial, 0°C to +70°C**
W83628AGEVB	**W83628/629AG Evaluation board**	

5. BLOCK DIAGRAM OF W83628AG



6. BLOCK DIAGRAM OF W83629AG



7. FUNCTION DESCRIPTION

The W83628AG and W83629AG support the functional sub-block interfaces described below:

7.1 PCI Interface

The W83628AG provides a PCI slave/master interface. The slave mode means the PCI cycles are initiated by the PCI Host Bridge or South Bridge chipset. Default is PCI bus cycle information from PCI Host Bridge being received in PCI slave mode. When ISA bus's MASTER# signal is asserted, the W83628A's PCI interface as slave mode will be switched to PCI master mode to drive/initiate PCI bus cycles to PCI bus. The W83628AG supports some positive decodes and implements subtractive decodes for unclaimed PCI accesses.

The PCI slave interface supports the positive decodes as below:

- PCI configuration register spaces which are positively decode with medium DEVSEL# timing speed on the Type0 PCI configuration cycle.
- Eight IO positively decode space which can be programmed to claim PCI I/O cycle with Fast/Medium/Slow/Subtractive DEVSEL# timing speed.
- Four Memory positively decode spaces which can be programmed to claim PCI Memory cycle with Fast/Medium/Slow/Substractive DEVSEL# timing speed.
- PC/PCI DMA (PPDMA) cycle space:The I/O portion of the DMA cycle generates a PCI I/O cycle to one of the four I/O addresses of 0000h/0004h/00C0h/00C4h
- ISA BIOS ROM boot up scheme: upload boot ROM on ISA bus during system boot up. Enable/disbale optionally the function through the external pull-up resistor on signal ROMCS# of the W83628AG. When PCIRST# is asserted, the signal ROMCS# will be detected and latched. After PCIRST# is released, the latched signal High(1)/Low(0) means to enable(1)/disable(0) the ISA BIOS ROM boot up function, respectively. The latched bit can also be disabled/enabled through Type0 PCI configuration cycle.

The PCI master interface will issue PCI cycle for ISA bus master cycle.

The W83628AG and the W83629AG together support PC/PCI DMA. The W83629AG uses dedicated ISAREQ# and ISAGNT# signals to permit ISA devices' transfer requests associated with specific DMA channels. Upon receiving a request and getting control of the PCI bus, South Bridge chipset performs a two-cycle transfer. For example, if data is to be moved from the peripheral to the main memory, the chipset will first read data from the peripheral and then write it to the main memory.

When in PC/PCI DMA cycle, the W83629AG DACKn# is decoded from ISAGNT#. As long as the ISAGNT# and MASTER# signals are asserted and are with an ISA command issued by ISA master, then the W83628AG PCI master interface will issues a PCI cycle for ISA master.

7.2 ISA Interface

The W83628AG provides an ISA bus interface for the subtractive decoded memory and I/O cycles on PCI. Default is driving/issuing relative legacy ISA bus cycle to ISA bus in ISA master mode. Generally if a valid PCI memory or I/O cycle is received by the W83628AG PCI slave interface, it will be passed to the internal ISA interface and the ISA interface will convert it to correspond to the ISA bus cycle. When ISA bus's MASTER# signal is asserted, the W83628AG ISA interface as master mode will be switched to ISA slave mode to receive legacy ISA bus cycles from the ISA bus. That means there is an ISA command issued by ISA master. The related ISA bus cycle will be passed to PCI master interface to drive/issue corresponding PCI bus cycle.

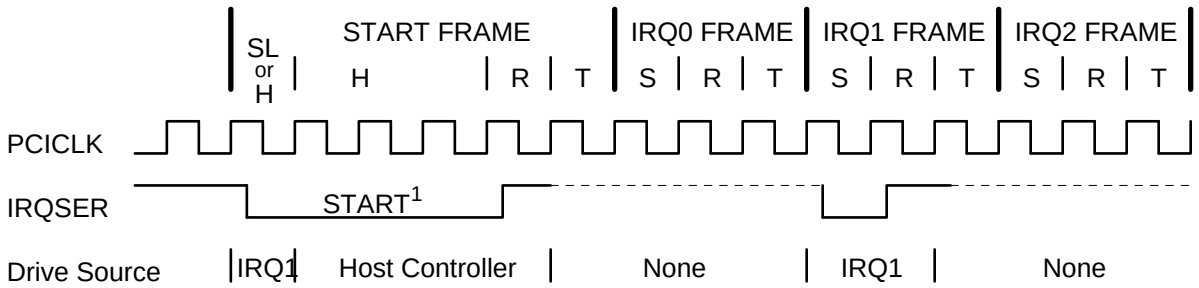
7.3 Serial IRQ Interface

The W83629AG supports a serialized IRQ slave which conforms to the specification of "Serialized IRQ Support for PCI system, rev. 6.0, September 1, 1995". Two modes, continuous and quiet, are supported.

The serial IRQ interface provides signal filtering and encoding logic for all legacy parallel ISA IRQ channels (IRQ15-14, 12-9, 7-3 and IOCHK#) to convert them to serial IRQ on the SERIRQ line. The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame.

This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

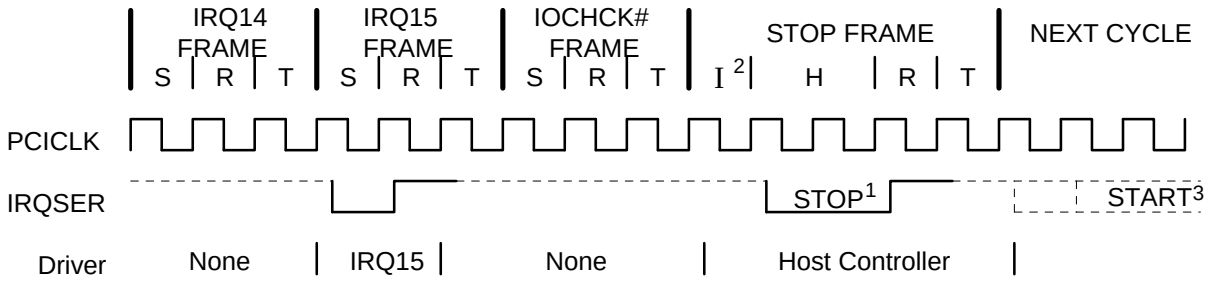
- Start Frame timing with source sampled a low pulse on IRQ1



H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Start Frame pulse can be 4-8 clocks wide

- Stop Frame Timing with Host using 17 IRQSER sampling period



H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

The main difference between the quite mode and the continuous mode for the IRQSER Frame is:

- Quiet (Active) Mode: Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle.
- Continuous (Idle) Mode: Only the Host controller can initiate a Start Frame to update IRQ/Data line information.

7.4 PC/PCI DMA Interface

The W83629AG supports PC/PCI DMA Serial Channel Passing Protocol interface as shown in Figure 6-1.

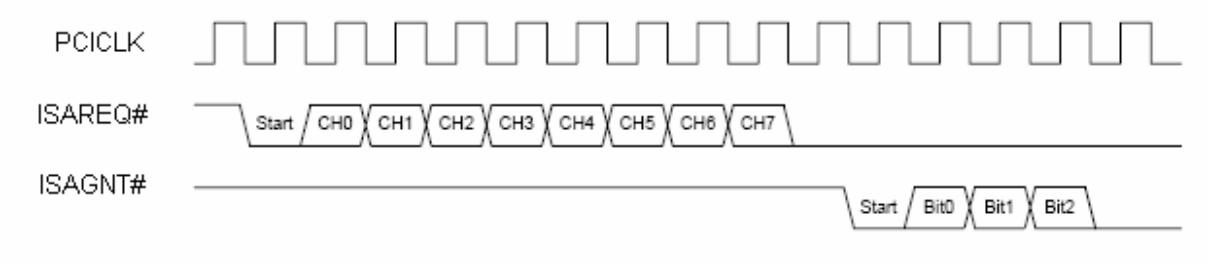


Figure 6-1: PC/PCI DMA Serial Channel Passing Protocol

When the W83629AG receives the legacy ISA DMA requesting DRQn, the DMA interface must encode the channel request information, where CH0-CH7 will be active high, depending on which is requested as the DMA channel.

The South Bridge chipset encodes the granted channel on the ISAGNT# line, where the bits have the same meaning. For example, the sequence [start, bit0, bit1, bit2] = [0, 1, 0, 0] grants DMA channel 1 to the requesting device, and the sequence [start, bit0, bit1, bit2] = [0, 0, 1, 1] grants DMA channel 6 to the requesting device.

After receiving a valid grant and detecting ISAGN# start bit, the W83629AG will decode and convert the ISAGNT# signal information to corresponding legacy ISA DMA acknowledge DACKn# signal.

Table 6-1 below shows the I/O portion of the DMA cycle generates a PCI I/O cycle to one of the four I/O addresses. The W83628AG will recognize the PCI I/O cycle with the DMA I/O address. These cycles must be qualified by an active ISAGNT# signal to the requesting device. A2 of DMA I/O address bit 2 is used to indicate DMA Terminal Count cycle.

DMA CYCLE TYPE	DMA I/O ADDRESS	TC(A2)	PCI CYCLE TYPE
Normal	00h	0	I/O Read/Write
Normal TC	04h	1	I/O Read/Write
Verify	0C0h	0	I/O Read
Verify TC	0C4h	1	I/O Read

Table 6-1: DMA Cycle Type and I/O Address

7.5 ISA Bus SYSCLK Clock Generation

The W83628AG generates the ISA SYSCLK clock using PCI clock signal. A PCICLK divisor (3, 4) is programmable through PCI configuration register to generate the ISA SYSCLK clock signal. This provides ISA SYSCLK frequencies 8.33MHz and 11MHz of a typical 33MHz PCICLK.

7.6 ISA Bus I/O Recovery Time

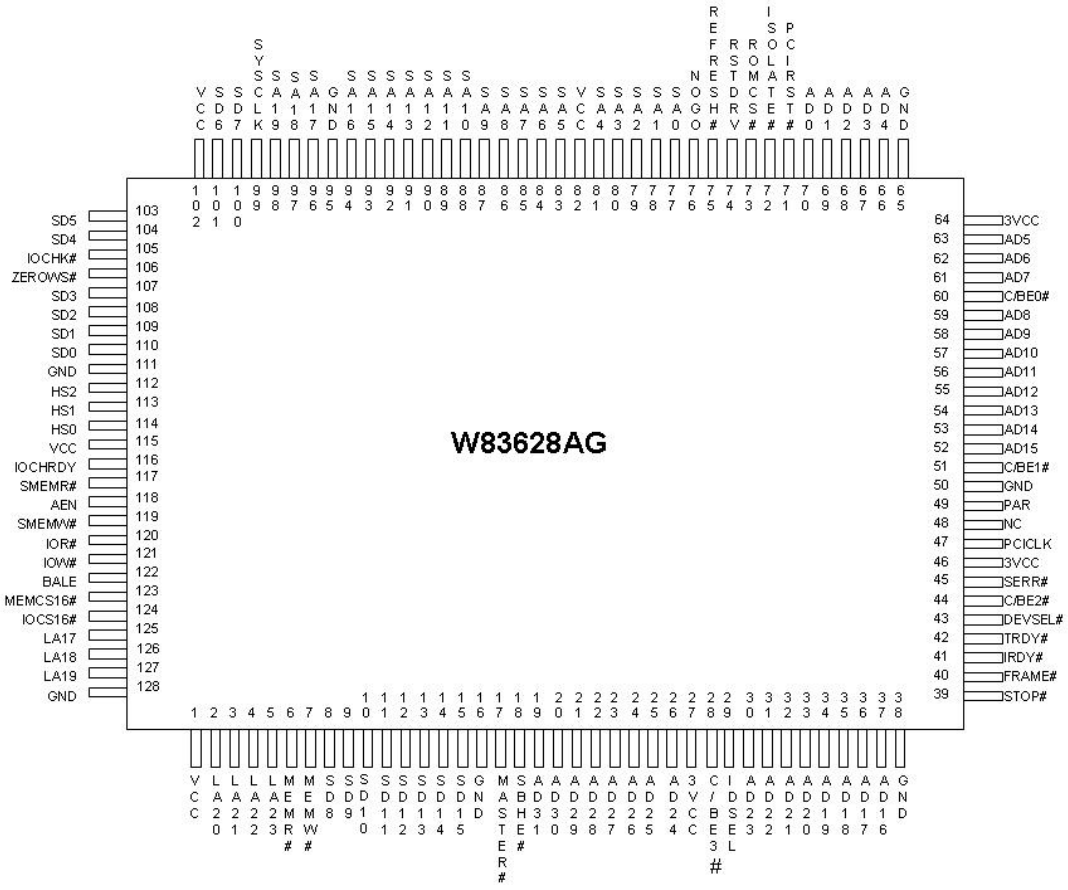
The W83628AG supports 8-bit/16-bit I/O recovery time for back-to-back ISA I/O cycles. The register can be programmed through Type0 PCI configuration cycle.

7.7 NOGO

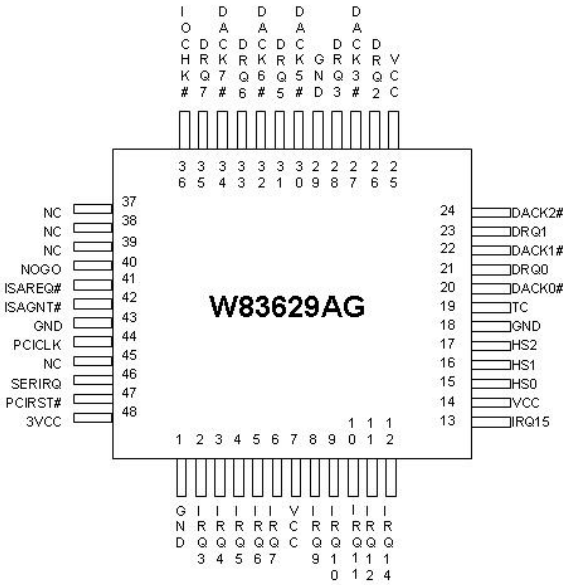
The W83628AG and W83629AG also support NOGO function. The NOGO signal generally connected to South Bridge chipset's NOGO signal is used to disable the subtractive decode function when NOGO signal is asserted high during system boot-up, since there is only one subtractive decode device presented on the PCI bus .

8. PIN CONFIGURATION

8.1 PIN CONFIGURATION FOR W83628AG



8.2 PIN CONFIGURATION FOR W83629AG



9. PIN DESCRIPTION

Note: Please refer to Section 10 DC CHARACTERISTICS for details.

I/O_{10t}	- TTL level bi-directional pin with 10 mA source-sink capability
I/O_{18t}	- TTL level bi-directional pin with 18 mA source-sink capability
I/O_{10tp3}	- 3.3V TTL level bi-directional pin with 10 mA source-sink capability
I/O_{18tp3}	- 3.3V TTL level bi-directional pin with 18 mA source-sink capability
I/OD_{10t}	- TTL level bi-directional pin open drain output with 10 mA sink capability
I/OD_{18t}	- TTL level bi-directional pin open drain output with 18 mA sink capability
OUT_{10t}	- TTL level output pin with 10 mA source-sink capability
OUT_{18t}	- TTL level output pin with 18 mA source-sink capability
OD_{10}	- Open-drain output pin with 10 mA sink capability
IN_t	- TTL level input pin
IN_{ts}	- TTL level Schmitt-trigger input pin

9.1 W83628AG PIN DESCRIPTION

9.1.1 PCI Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
AD[31:0]	19-26 30-37 52-59 61-63 66-70	I/O_{18tp3}	**PCI Bus Address and Data Signals.** The standard PCI address and data lines. The address is driven with FRAME# assertion; the data is driven or received in following clocks.	3.3V
C/BE[3:0]#	28,44 51,60	I/O_{18tp3}	**PCI Bus Command and Byte Enables.** During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as Byte Enables.	3.3V
PCICLK	47	IN_{ts}	**PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All the other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.	3.3V

8.1.1 PCI Interface, contiuned

SYMBOL	PIN	I/O	FUNCTION	LEVEL
FRAME#	40	I/O_{18tp3}	**Frame Signal**. FRAME# is driven by the current PCI bus master to indicate the beginning and duration of an access.	3.3V
IDSEL	29	IN_{ts}	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write transactions. This signal should be externally tied to one of the upper 21 address signals.	3.3V
STOP#	39	I/O_{10tp3}	**Bus Stop#.** STOP# indicates the current target is requesting the master to stop the current PCI bus transaction.	3.3V
IRDY#	41	I/O_{10tp3}	**Initiator Ready.** IRDY# indicates the initiating agent's ability to complete the current data phase of the PCI bus transaction.	3.3V
TRDY#	42	I/O_{10tp3}	**Target Ready.** TRDY# indicates the target agent's ability to complete the current data phase of the PCI bus transaction.	3.3V
DEVSEL#	43	I/O_{10tp3}	**Device Select.** The W83628AG drives DEVSEL# to indicate that it is the target of the current PCI bus transaction. The W83628AG uses subtractive decoding and the NOGO protocol to claim PCI transactions.	3.3V
SERR#	45	OD_{10}	**System Error.** SERR# can be pulsed active by any PCI agent that detects a system error condition.	3.3V
PAR	49	I/O_{10tp3}	**Parity Signal.** The W83628AG generates even parity across AD[31:0] and C/BE[3:0]#.	3.3V
PCIRST#	71	IN_{ts}	**PCI Reset.** The W83628AG receives PCIRST# as a reset from the PCI Bus.	3.3V

9.1.2 Control Logic and Handshaking Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
HS[2:0]	112-114	I/O10t	**Handshaking Signals.** HS[2:0] are connected to the W83629AG for PCI to ISA SET handshaking signals. **HS1 is handshaking Signal 1; this pin is weak pulled-down while PCIRST# is asserted. Applying a pull-up resistor (4.7Kohm) to this pin disables ISA bridge subtraction decoder.**	5V
ISOLATE#	72	INts	**Isolation Control Input. Isolate#** is an active low signal by user programming to control all of the output signals of the W83628AG to Isolation and Tri-state.	3.3V
NOGO	76	INt	**NOGO,** This signal indicates which master initiates the current transaction and whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and the W83628AG.	5V

9.1.3 ISA Interface Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
SA[19:17]	98-96	I/O18t	**System Address Bus.** These are the upper address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[19:17] are at an unknown state upon PCIRST#.	5V
SA[16:0]	94-83 81-77	I/O18t	**System Address Bus.** These are the bi-directional lower address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[16:0] are at an unknown state upon PCIRST#.	5V
SD[15:0]	110-107, 104,103, 101,100, 8-15	I/O18t	**System Data.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. The W83628AG tri-states SD[15:0] during PCIRST#.	5V
AEN	118	OUT18t	**Address Enable.** AEN is asserted during DMA cycles. This signal is also driven high when the W83628AG initiates refresh cycles. AEN is driven low upon PCIRST#.	5V
IOR#	120	I/O18t	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]).	5V

SYMBOL	PIN	I/O	FUNCTION	LEVEL
IOW#	121	I/O_{18t}	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]).	5V
IOCHRDY	116	I/O_{18t}	**I/O Channel Ready.** Resources on the ISA Bus negate IOCHRDY to indicate that additional time (wait states) is required to complete the cycle.	5V
SYSCLK	99	OUT_{18t}	**ISA System Clock.** SYSCLK is the reference clock for the ISA bus. The SYSCLK is generated by dividing PCICLK by 3 or 4.	5V
RSTDRV	74	OUT_{18t}	**Reset Drive.** The W83628AG asserts RSTDRV to reset devices that reside on the ISA Bus. The W83628AG asserts this signal while the PCIRST# is asserted.	5V
IOCS16#	124	IN_t	**16-bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.	5V
SBHE#	18	I/O_{18t}	**System Byte High Enable.** SBHE# asserted indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is at an unknown state upon PCIRST#.	5V
IOCHK#	105	IN_t	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus during the detection of an error.	5V
MEMR#	6	I/O_{18t}	**Memory Read.** MEMR# asserted indicates the current ISA bus cycle is a memory read.	5V
MEMW#	7	I/O_{18t}	**Memory Write.** MEMW# asserted indicates the current ISA bus cycle is a memory write.	5V
MASTER#	17	IN_t	**MASTER#.** This signal is used with a DREQ line by an ISA master to gain control over the ISA Bus.	5V
LA[23:17]	5-2 127-125	I/O_{18t}	**Unlatched Address.** The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when the W83628AG owns the ISA Bus.	5V

SYMBOL	PIN	I/O	FUNCTION	LEVEL
ROMCS#	73	I/O10t	**ROMCS#. This pin is weak pulled-down while PCIRST is asserted. Applying a pull-up resistor (4.7K ohm) to this pin enables positive decoder of BIOS address range (depending on Configure register 70, bit 3,2). When the BIOS access range is enabled, the pin is BIOS ROMCS# output.**	5V
REFRESH#	75	I/O18t	**Refresh.** REFRESH# asserted indicates that a refresh cycle is in progress, or that an ISA master is requesting the W83628AG to generate a refresh cycle. Upon PCIRST#, this signal is tri-stated.	5V
ZEROWS#	106	INt	**Zero Wait States.** An ISA slave asserts ZEROWS# after its address and command signals are decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles.	5V
SMEMR#	117	OUT18t	**Standard Memory Read.** SMEMR# asserted indicates the current ISA bus cycle is a memory read cycle to an address below 1 Mbyte.	5V
SMEMW#	119	OUT18t	**Standard Memory Write.** SMEMW# asserted indicates the current ISA bus cycle is a memory write cycle to an address below 1 Mbyte.	5V
BALE	122	OUT18t	**Bus Address Latch Enable.** BALE is an active high signal asserted by the W83628AG to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. BALE is driven low upon PCIRST#.	5V
MEMCS16#	123	I/OD18t	**Memory Chip Select 16.** MEMCS16# asserted indicates that the memory slave supports 16-bit accesses.	5V

9.1.4 Power Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
VCC	1, 82, 102, 115	PWR	**5V Supply.**	5V
3VCC	27, 46, 64	PWR	**3.3V Supply.**	3.3V
GND	16, 38, 50, 65, 95, 111, 128	PWR	**Ground.**	0V

9.1.5 NC Pins

SYMBOL	PIN	I/O	FUNCTION	LEVEL
NC	48		**No Connection.**	

9.2 W83629AG PIN DESCRIPTION

9.2.1 Control Logic and Handshaking Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
HS[2:0]	17-15	I/O_{10t}	**Handshaking Signals.** HS[2:0] are connected to the W83628AG for PCI to ISA SET handshaking signals.	5V
NOGO	40	IN_{ts}	**NO GO.** This signal indicates which master initiates the current transaction and whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and the W83628AG.	5V
PCICLK	44	IN_{ts}	**PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All the other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge.	3.3V
PCIRST#	47	IN_{ts}	**PCI Reset.** The W83628AG receives PCIRST# as a reset from the PCI Bus.	3.3V

9.2.2 PC/PCI Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
ISAREQ#	41	OUT_{18t}	**ISA Bus Request.** This signal is a point-to-point signal between the W83629AG and a PCI HOST arbiter. The W83629AG asserts this signal according to the PC/PCI protocol.	3.3V
ISAGNT#	42	IN_{ts}	**ISA Bus Grant.** This signal is a point-to-point signal between the W83629AG and a PCI HOST Bridge's secondary bus PCPCIGNT# signal. The W83629AG asserts this signal according to the PC/PCI protocol.	3.3V
DRQ [7:5,3:0]	35,33,31, 28,26,23, 21	IN_{t}	**DMA Request.** The DREQ signal indicates that either a slave DMA device is requesting DMA services, or an ISA bus master is requesting to use the ISA bus.	5V

SYMBOL	PIN	I/O	FUNCTION	LEVEL
DACK [7:5,3:0]#	34,32,30, 27,24,22, 20	OUT_{18t}	**DMA Acknowledge.** The DACK# signal indicates that either a DMA channel or an ISA bus master is granted to the ISA bus.	5V
TC	19	OUT_{18t}	**Terminal Count.** The W83628AG asserts TC to DMA slaves as a terminal count indicator.	5V

9.2.3 IRQ Serializer Interface

SYMBOL	PIN	I/O	FUNCTION	LEVEL
SERIRQ	46	I/OD_{10t}	**Serial Interrupt Requested Signals.** This signal is to transfer IRQ from the parallel IRQ mode to the serial IRQ mode.	3.3V
IRQ[3:7,9:12,14,15]	2-6 8-13	IN_t	**Parallel Interrupt Requested Input.**	5V
IOCHK#	36	IN_t	**I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus with the detection of an error.	5V

9.2.4 Power Signals

SYMBOL	PIN	I/O	FUNCTION	LEVEL
VCC	7, 14, 25	PWR	**5V Supply.**	5V
3VCC	48	PWR	**3.3V Supply.**	3.3V
GND	1, 18, 29, 43	PWR	**Ground.**	0V

9.2.5 NC Pins

SYMBOL	PIN	I/O	FUNCTION	LEVEL
NC	37, 38, 39, 45		**No Connection**	

10. PCI CONFIGURATION REGISTERS

10.1 VID-VENDOR IDENTIFICATION REGISTER

Address Offset: 01h_00h

Default Value: 10h_50h

Attribute: Read only

This register is read-only and contains Nuvoton vendor identification number (1050h).

10.2 DID-DEVICE IDENTIFICATION REGISTER

Address Offset: 03h_02h

Default Value: 06h_28h

Attribute: Read only

This register is read-only and contains the device identification number (0628h).

10.3 PCICMD-PCI COMMAND REGISTER

Address Offset: 05h_04h

Default Value: 00h_07h

Attribute: Read/Write

This register provides control over the ISA bridge to generate and respond to PCI cycles properly. When a 0 is written to this register, the ISA bridge is to be disconnected from the PCI bus for all accesses except configuration accesses.

Bit 15:10 **Reserved.**

Bit 9 **Fast Back to Back.** This bit always returns a zero.

Bit 8 **SERR# Enable.**

=1 Enable.

=0 Disable.

Bit 7 **Wait Cycle Control (Not supported).**

Hardwired to zero.

Bit 6 **Parity Error Response (Not supported).**

Hardwired to zero.

Bit 5 **VGA Palette Snoop Enable (Not supported).**

Hardwired to zero.

Bit 4 **Memory Write and Invalidate Enable (Not supported).**

Hardwired to zero.

Bit 3 **Parity Error Response (Not supported).**

Hardwired to zero.

Bit 2 **Bus Master Enable**

Hardwired to one. The ISA bridge Bus Masters are always supported to generate a PCI Bus master cycle.

Bit 1 **Memory Space Enable**

Hardwired to one. The ISA bridge Memory space is always enabled.

Bit 0 **I/O Space Enable**

Hardwired to one. The ISA bridge I/O space is always enabled.

10.4 PCISTS-PCI STATUS REGISTER

Address Offset: 07h_06h

Default Value: 02h_00h

Attribute: Read/Write

This register shows status information for PCI bus related events.

Bit 15 **Detected Parity Error**

Hardwired to zero. The ISA bridge does not check bus parity.

Bit 14 **Signaled System Error**

This bit is set when ISA bridge asserts SERR# on PCI bus.

Bit 13 **Received Master Abort Status**

This bit is set when the ISA bridge is target aborted as a master on the PCI bus. Software sets this bit to 0 by writing a 1 to it.

Bit 12 **Received Target Abort Status**

This bit is set when the ISA bridge target aborts a PCI transaction as a target. Software sets this bit to 0 by writing a 1 to it.

Bit 11 **Signaled Target Abort Status**

This bit is set when the ISA bridge signals a target abortion for a PCI transaction. Software sets this bit to 0 by writing a 1 to it.

Bit 10:9 **DEVSEL# Timing.** This 2 bits always return a 01b (medium decode).

Bit 8 **Data Parity Detected (Not supported)**

Hardwired to zero.

Bit 7 **Fast Back-to-Back (Not supported)**

Hardwired to zero.

Bit 6 **66 MHz/ 33 MHz (Only support 33 MHz).**

Hardwired to zero.

Bit 5 **User Defineable Features (Not supported).**

Hardwired to zero.

Bit 4:0 **Reserved.**

Reserved and will return zero when reading this register.

10.5 REVID-REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: See the lastest stepping information
Attribute: Read Only

This register shows status information for PCI bus related events.

Bit 7:0 **Revision Identification Number.**

10.6 CCODE-CALSS CODE REGISTER

Address Offset: 0Bh_0Ah_09h
Default Value: 06h_01h_00h
Attribute: Read Only

The class code register is a read-only register and used to identify the ISA bridge.

Bit 23:16 **Base Class Code.**

06h = Bus Bridge

Bit 15:8 **Sub-Class Code.**

01h = PCI to ISA Bridge

Bit 7:0 **Programming Interface.**

00h

10.7 HEADT-HEAD TYPE REGISTER

Address Offset: 0Eh

Default Value: 00h

Attribute: Read Only

The register is a read-only register and used to indicate that the ISA bridge configuration space adheres to PCI local bus specification. It also indicates that ISA bridge is not a multifunction device.

Bit 7 **Multifunction Indicator.**

0 = Not a multifunction device.

Bit 6:0 **Layout Code.**

00h = PCI layout type.

10.8 IO_RCVR-IO RECOVERY REGISTER

Address Offset: 40h

Default Value: 4Dh

Attribute: Read/Write

Bit 7 **SYSCLK Divider.**

0 = SYSCLK is equal to PCICLK divided by 4.

1 = SYSCLK is equal to PCICLK divided by 3.

Bit 6 **8-bit I/O Recovery Enable**

0 = Disable bits 5:3 setting and use 3.5 SYSCLKs for 8 bit I/O recovery time.

1 = Enable bits 5:3 setting.

Bit 5:3 **8-bit I/O RecoveryTimes.**

When bit 6=1, this 3-bit field defines the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 8 bit I/O

000 =0 SYSCLK

001 =1 SYSCLK

010 =2 SYSCLKs

011 =3 SYSCLKs

100 =4 SYSCLKs

101 =5 SYSCLKs

110 =6 SYSCLKs

111 = 7 SYSCLKs

Bit 2 **16-bit I/O Recovery Enable.**

= 0 Ignore bits 1:0 setting and uses 3.5 SYSCLKs for 16-bit I/O recovery time.

= 1 The 16-bit I/O recovery time is decided by bits 1:0.

Bit 1:0 **16-bit I/O Recovery Times.**

When bit 2=1, this 2-bit field defines the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 16 bit I/O

= 01 1 SYSCLK

= 10 2 SYSCLKs

= 11 3 SYSCLKs

= 00 4 SYSCLKs

10.9 WISA_STS-ISA BRIDGE ERROR STATUS REGISTER

Address Offset: 42h

Default Value: 00h

Attribute: Read/Write

Bit 7:3 **Reserved.**

Bit 2 **IOCHK# Pin State.**

This bit reflects the inverse state of the IOCHK# pin on the ISA bus.

Bit 1 **Reserved.**

Bit 0 **Byte Lane Error.**

This bit is set if the ISA bridge detects an illegal byte lane combination for a PCI I/O cycles.

10.10 BRIDGE FAST MEMORY DECODER #0 CONTROL REGISTERS

Address Offset: 47h_46h_45h_44h

Default Value: 00h_00h_02h_00h

Attribute: Read/Write

Bit [31:24] High Page Base Address of Fast Memory Decoder #0:

PCI A[31:24]. W83628AG will relocate the access within Fast Memory Decoder to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.

Bit [23:14] Low Base Address of Fast Memory Decoder #0:PCI A[23:14]

Bit [13:12] Reserved.

Bit 11 Enable/Disable Fast Memory Decoder #0

1=Enable, 0=Disable

Bit 10 Enable Fast Memory Decoder #0 High Page Address A[31:24] Comparison Function.

1=Enable, 0=Disable

Bit [9:8] Fast Memory Decoder #0

00=Subtractive speed, 01= Slow speed, 10=Medium speed, 11=Fast speed

Bit[7:0] Fast Memory Decoder#0 Mask Control

Bit[7:0] is used to mask PCI address bits of A[23:14], respectively. If the corresponding bit of the register is set to 1 (one), the corresponding address bits [23:14] are ignored by the Fast Memory Address Decoder #0. The following example will show the Fast Memory Decoder #0 size setting. If bit[7:0] = 00h, the size is 16K bytes. If bit[7:0]=01h, the size is 32K bytes. If bit[7:0]=7fh, the size is 2M bytes. If bit[7:0]=ffh, the size is 4M bytes.

10.11 BRIDGE FAST MEMORY DECODER #1 CONTROL REGISTERS

Address Offset: 4Bh_4Ah_49h_48h

Default Value: 00h_00h_02h_00h

Attribute: Read/Write

Bit [31:24] High Page Base Address of Fast Memory Decoder #1: PCI A[31:24].

W83628AG will relocate the access within Fast Memory Decoder to ISA bus, but the A[31:24] will be ignored since ISA has SA[23:0] only.

Bit [23:14] Low Base Address of Fast Memory Decoder #1:PCI A[23:14]

Bit [13:12] Reserved.

Bit 11 Enable/Disable Fast Memory Decoder #1

1=Enable, 0=Disable

Bit 10 Enable Fast Memory Decoder #1 High Page Address A[31:24] Comparison Function.

1=Enable, 0=Disable

Bit [9:8] Fast Memory Decoder #1

00=Subtractive speed, 01= Slow speed, 10=Medium speed,11=Fast speed

Bit [7:0] Fast Memory Decoder#1 Mask Control

Bit[7:0] is used to mask PCI address bits of A[23:14], respectively. If the corresponding bit of the register is set to 1 (one), the corresponding address bits [23:14] are ignored by Fast Memory Address Decoder #1. The following example will show the Fast Memory Decoder #1 size setting. If bit[7:0] = 00h, the size is 16K bytes. If bit[7:0]=01h, the size is 32K bytes. If bit[7:0]=7fh, the size is 2M bytes. If bit[7:0]=ffh, the size is 4M bytes.

10.12 BRIDGE FAST MEMEORY DECODER #2 CONTROL REGISTERS

Address Offset: 4Fh_4Eh_4Dh_4Ch
Default Value: 00h_00h_02h_00h
Attribute: Read/Write

Bit [31:24] High Page Base Address of Fast Memory Decoder #2: PCI A[31:24].

W83628AG will relocate the access within Fast Memory Decoder to ISA bus, but the A[31:24] will be ignored, since ISA has SA[23:0] only.

Bit [23:14] Low Base Address of Fast Memory Decoder #2:PCI A[23:14]

Bit [13:12] Reserved.

Bit 11 Enable/Disable Fast Memory Decoder #2.

1=Enable, 0=Disable

Bit 10 Enable Fast Memory Decoder #2 High Page Address A[31:24] Comparison Function.

1=Enable, 0=Disable

Bit [9:8] Fast Memory Decoder #2.

00=Subtractive speed, 01= Slow speed, 10=Medium speed, 11=Fast speed

Bit [7:0] Fast Memory Decoder#2 Mask Control

Bit[7:0] is used to mask PCI address bits of A[23:14], respectively. If the corresponding bit of the register is set to 1 (one), the corresponding address bits [23:14] are ignored by Fast Memory Address Decoder #2. The following example will show the Fast Memory Decoder #2 size setting. If bit[7:0] = 00h, the size is 16K bytes. If bit[7:0]=01h, the size is 32K bytes. If bit[7:0]=7fh, the size is 2M bytes. If bit[7:0]=ffh, the size is 4M bytes.

10.13 WISA_FADC-ISA BRIDGE FAST IO DECODERS CONTROL REGISTERS

Address Offset: 53h_52h_51h_50h

Default Value: AAh_AAh_00h_00h

Attribute: Read/Write

Bit [31:30] IO Decoder #7.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [29:28] IO Decoder #6.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [27:26] IO Decoder #5.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [25:24] IO Decoder #4.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [23:22] IO Decoder #3.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [21:20] IO Decoder #2.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit[19:18] IO Decoder #1.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit [17:16] IO Decoder #0.

00=Subtractive speed, 01=Slow speed, 10=Medium speed, 11=Fast speed

Bit 15 Enable IO Decoder #7 Address A[15:12] comparison

1=Enable, 0=Disable

Bit 14 Enable IO Decoder #6 Address A[15:12] comparison

1=Enable, 0=Disable

Bit 13 **Enable IO Decoder #5 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit 12 **Enable IO Decoder #4 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit 11 **Enable IO Decoder #3 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit10 **Enable IO Decoder #2 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit 9 **Enable IO Decoder #1 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit 8 **Enable IO Decoder #0 Address A[15:12] comparison**

1=Enable, 0=Disable

Bit 7 **Enable/Disable Fast I/O Address Decoder # 7.**

Bit 6 **Enable/Disable Fast I/O Address Decoder # 6.**

Bit 5 **Enable/Disable Fast I/O Address Decoder # 5.**

Bit 4 **Enable/Disable Fast I/O Address Decoder # 4.**

Bit 3 **Enable/Disable Fast I/O Address Decoder # 3.**

Bit 2 **Enable/Disable Fast I/O Address Decoder # 2.**

Bit 1 **Enable/Disable Fast I/O Address Decoder # 1.**

Bit 0 **Enable/Disable Fast I/O Address Decoder # 0.**

10.14 ISA_FAD0MC-ISA BRIDGE FAST DECODERS # 0 MASK CONTROL REGISTER

Address Offset: 58h

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 0. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 0.

10.15 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 1 MASK CONTROL REGISTER

Address Offset: 59h

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 1. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 1.

10.16 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 2 MASK CONTROL REGISTER

Address Offset: 5Ah

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 2. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 2.

10.17 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 3 MASK CONTROL REGISTER

Address Offset: 5Bh

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 3. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 3.

10.18 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 4 MASK CONTROL REGISTER

Address Offset: 5Ch
Default Value: 00h
Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 4. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 4.

10.19 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 5 MASK CONTROL REGISTER

Address Offset: 5Dh
Default Value: 00h
Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 5. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 5.

10.20 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 6 MASK CONTROL REGISTER

Address Offset: 5Eh
Default Value: 00h
Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 6. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 6.

10.21 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 7 MASK CONTROL REGISTER

Address Offset: 5Fh
Default Value: 00h
Attribute: Read/Write

This register is used to mask address bits (A7~A0) for fast address decoder # 7. If the corresponding bit of this register is set to 1, the corresponding address bit (A7~A0) is ignored by the faster address decoder # 7.

10.22 WISA_FADCB0-ISA BRIDGE FAST DECODERS # 0 BASE ADDRESS REGISTER

Address Offset: 61h_60h**
Default Value: 00h_00h
Attribute: Read/Write
This register contains the base address for fast address decoder # 0.

Note: 60h is the lower byte and 61h is the upper byte.

10.23 WISA_FADCB1-ISA BRIDGE FAST DECODERS # 1 BASE ADDRESS REGISTER

Address Offset: 63h_62h
Default Value: 00h_00h
Attribute: Read/Write
This register contains the base address for fast address decoder # 1.

10.24 WISA_FADCB2-ISA BRIDGE FAST DECODERS # 2 BASE ADDRESS REGISTER

Address Offset: 65h_64h
Default Value: 00h_00h
Attribute: Read/Write
This register contains the base address for fast address decoder # 2.

10.25 WISA_FADCB3-ISA BRIDGE FAST DECODERS # 3 BASE ADDRESS REGISTER

Address Offset: 67h_66h
Default Value: 00h_00h
Attribute: Read/Write
This register contains the base address for fast address decoder # 3.

10.26 WISA_FADCB4-ISA BRIDGE FAST DECODERS # 4 BASE ADDRESS REGISTER

Address Offset: 69h_68h
Default Value: 00h_00h
Attribute: Read/Write
This register contains the base address for fast address decoder # 4.

10.27 WISA_FADCB5-ISA BRIDGE FAST DECODERS # 5 BASE ADDRESS REGISTER

Address Offset: 6Bh_6Ah

Default Value: 00h_00h

Attribute: Read/Write

This register contains the base address for fast address decoder # 5.

10.28 WISA_FADCB6-ISA BRIDGE FAST DECODERS # 6 BASE ADDRESS REGISTER

Address Offset: 6Dh_6Ch

Default Value: 00h_00h

Attribute: Read/Write

This register contains the base address for fast address decoder # 6.

10.29 WISA_FADCB7-ISA BRIDGE FAST DECODERS # 7 BASE ADDRESS REGISTER

Address Offset: 6Fh_6Eh

Default Value: 00h_00h

Attribute: Read/Write

This register contains the base address for fast address decoder # 7.

10.30 WISA_CTRLREG1-ISA BRIDGE CONTROL REGISTER 1

Address Offset: 70h

Default Value: 0000***10s***sb

Attribute: Read/Write

Power-on setting bits bit 1:0 are power-on set by ROMCS# and HS1.

Default voltage level will be internal pull-down resistance 47K ohm to logical 0 level during PCIRST# reset cycle.

Bit 7-6 Reserved.

Bit 5-4 = 00 Send AD Bus with no STEP

= 01 Send AD Bus with 2 STEP

= 10 Send AD Bus with 4 STEP

= 11 Reverse

Bit 3-2 = 00 1MB BIOS ROM positive decode.

= 01 2MB BIOS ROM positive decode.

= 10 4MB BIOS ROM positive decode.

= 11 8MB BIOS ROM positive decode.

Bit 1 =0 Disable High-Address BIOS ROM decoder.

=1 Enable High-Address BIOS ROM decoder.

This bit can be set/reset by ROMCS# power-on setting during PCIRST# assertion.

Bit 0 =0 Normal mode.

=1 Disable ISA Bridge subtraction decoder.

This bit can be set/reset by HS1 power-on setting during PCIRST# assertion.

10.31 WISA_CTRLREG2-ISA BRIDGE CONTROL REGISTER 2

Address Offset: 71h
Default Value: 00h
Attribute: Read/Write

Bit 7 **=0 Enable IRQ11.** **=1 Disable IRQ11.**

Bit 6 **=0 Enable IRQ10.** **=1 Disable IRQ10.**

Bit 5 **=0 Enable IRQ9.** **=1 Disable IRQ9.**

Bit 4 **=0 Enable IRQ7** **=1 Disable IRQ7.**

Bit 3 **=0 Enable IRQ6.** **=1 Disable IRQ6.**

Bit 2 **=0 Enable IRQ5.** **=1 Disable IRQ5.**

Bit 1 **=0 Enable IRQ4.** **=1 Disable IRQ4.**

Bit 0 **=0 Enable IRQ3.** **=1 Disable IRQ3.**

10.32 WISA_CTRLREG3-ISA BRIDGE CONTROL REGISTER 3

Address Offset: 72h
Default Value: 00h
Attribute: Read/Write

Bit 7 **Reserved. Always write 0 to this bit.**

Bit 6 **Reserved. Always write 0 to this bit.**

Bit 5 **Reserved. Always write 0 to this bit.**

Bit 4 **Reserved. Always write 0 to this bit.**

Bit 3 **1=Enable IOCHK#, 0=Disable IOCHK#**

Bit 2 **0=Enable IRQ15, 1=Disable IRQ15**

Bit 1 **0=Enable IRQ14, 1=Disable IRQ14**

Bit 0 **0=Enable IRQ12, 1=Disable IRQ12**

10.33 WISA_CTRLREG4-ISA BRIDGE CONTROL REGISTER 4

Address Offset: 73h
Default Value: 00h
Attribute: Read/Write

Bit 7 **=0 Enable DRQ 7. =1 Disable DRQ 7.**

Bit 6 **=0 Enable DRQ6. =1 Disable DRQ6.**

Bit 5 **=0 Enable DRQ5. =1 Disable DRQ5.**

Bit 4 **Reserevd. Always write 0 to this bit.**

Bit 3 **=0 Enable DRQ 3. =1 Disable DRQ 3.**

Bit 2 **=0 Enable DRQ 2. =1 Disable DRQ 2.**

Bit 1 **=0 Enable DRQ 1. =1 Disable DRQ 1.**

Bit 0 **=0 Enable DRQ 0. =1 Disable DRQ 0.**

10.34 BRIDGE FAST MEMORY DECODER #3 CONTROL REGISTERS

Address Offset: 77h_76h_75h_74h
Default Value: 00h_00h_02h_00h

Bit [31:24] **High Page Base Address of Fast Memory Decoder #3: PCI A[31:24].**

W83628AG will relocate the access within Fast Memory Decoder to ISA bus, but the A[31:24] will be ignored, since ISA has SA[23:0] only.

Bit [23:14] **Low Base Address of Fast Memory Decoder #3:PCI A[23:14]**

Bit [13:12] **Reserved.**

Bit 11 **Enable/Disable Fast Memory Decoder #3.**

1=Enable, 0=Disable

Bit 10 **Enable Fast Memory Decoder #3 High Page Address A[31:24] Comparison Function.**

1=Enable, 0=Disable

Bit [9:8] **Fast Memory Decoder #3.**

00=Subtractive speed,01= Slow speed, 10=Medium speed, 11=Fast speed

Bit [7:0] **Fast Memory Decoder#3 Mask Control**

Bit[7:0] is used to mask PCI address bits of A[23:14], respectively. If the corresponding bit of the register is set to 1 (one), the corresponding address bits [23:14] are ignored by the Fast Memory Address Decoder #3. The following example shows the Fast Memory Decoder #3 size setting. If bit[7:0] = 00h, the size is 16K bytes. If bit[7:0]=01h, the size is 32K bytes. If bit[7:0]=7fh, the size is 2M bytes. If bit[7:0]=ffh, the size is 4M bytes.

10.35 WISA_TSTREG-ISA BRIDGE TEST REGISTER

Address Offset: 82h_81h_80h

Default Value: 3Fh_00h_08h

Attribute: Read/Write

Bit 23 **Reserved. No data should be written to this register.**

Bit 22 **Reserved. No data should be written to this register.**

Bit [21:16] **Reserved. No data should be written to this register.**

Bit 15 **Reserved. No data should be written to this register.**

Bit 14 **Reserved**

Bit 13 **Reserved**

Bit 12 **Reserved**

Bit 11 **Reserved**

Bit [10:8] **Reserved. Always write 0 to the bits.**

Bit 7 **Reserved. No data should be written to this register.**

Bit 6 **Reserved. No data should be written to this register.**

Bit 5 **Reserved. No data should be written to this register.**

Bit 4 **0= 80h port decoding on subtractive cycles of LPC I/F**

1= 80h port decoding on positive cycles of LPC I/F

This bit must be set to 1 when LPC I/F is only decoding on positive cycles, but when the bridge is used in PIIX4 for test, set the bit to 0.

Bit 3 **Reserved. No data should be written to this register.**

Bit 2 **Reserved. No data should be written to this register.**

Bit 1 **Reserved. No data should be written to this register.**

Bit 0 **Reserved. No data should be written to this register.**

11. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 6.0	V
Input Voltage	-0.5 to Vcc+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to+ 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

12. DC CHARACTERISTICS

(Ta = 0° C to 70° C, Vcc = 5V ± 10%, 3Vcc=3.3V± 5% , GND = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_t – TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/O_{10t} - TTL level bi-directional pin with source-sink capability of 10 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -10 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{10tp3} – 3.3 V TTL level bi-directional pin with source-sink capability of 10 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -10 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/O_{18t} - TTL level bi-directional pin with source-sink capability of 18 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 18 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -18 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/O_{18tp3} – 3.3 V TTL level bi-directional pin with source-sink capability of 18 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 18 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -18 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD_{10t} – TTL level bi-directional pin. Open-drain output with 10 mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{18t} – TTL level bi-directional pin. Open-drain output with 18 mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 18 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
OD_{10} – Open-drain output pin with sink capability of 10 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
OUT_{10t} - TTL level output pin with source-sink capability of 10 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -10mA
OUT_{18t} - TTL level output pin with source-sink capability of 18mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 18 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -18 mA

13. AC CHARACTERISTICS

The PCI Bus Interface Signals are compliant with PCI Bus Specification, Rev 2.1

The ISA Bus Interface Signals conform with Abide Industry Standards.

(Ta = 0° C to 70° C, Vcc = 5V ± 10%, 3Vcc=3.3V± 5% , GND = 0V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	COMMENTS
PCICLK						
PCICLK Period	T_cyc	30		∞	ns	
PCICLK High Time	T_high	11			Ns	
PCICLK Low Time	T_low	11			ns	
PCICLK Slew time	--	1		4	mV/ns	

Unit: 1T = 1 PCICLK period

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	COMMENTS
SYSCLK						
SYSCLK Period	tSYSCLK		4T		ns	SYSCLK freq. = PCICLK freq. /4
			3T		ns	SYSCLK freq. = PCICLK freq. /3
SYSCLK High Time	tSYSCLK_H		2T		ns	SYSCLK freq. = PCICLK freq. /4
			1.5T		ns	SYSCLK freq. = PCICLK freq. /3
SYSCLK Low Time	tSYSCLK_L		2T		ns	SYSCLK freq. = PCICLK freq. /4
			1.5T		ns	SYSCLK freq. = PCICLK freq. /3

The following table values are measured in design simulation. The SYSCLK frequency is equal to PCICLK frequency divided by 4.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	COMMENTS
BALE						
BALE Pulse Width	t1a		2T		ns	
LA[23:17]						
LA[23:17] Valid Setup to BALE Inactive	t2a		6T		ns	
LA[23:17] Valid Hold from BALE Inactive	t2b	6T	10.5 T		ns	
LA[23:17] Valid Setup to MEMx# Active	t2c	1.5T	2T		ns	
LA[23:17] Valid Setuip to IOx# Active	t2d		2T		ns	

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	COMMENTS
LA[23:17] Invalid from MEMx# Active	t2e		11T		ns	8-bit memory cycle
			9T		ns	16-bit memory cycle
LA[23:17] Invalid from IOx# Active	t2f		30T		ns	8-bit I/O cycle
			18T		ns	16-bit I/O cycle
SA[19:0], SBHE#						
SA[19:0], SBHE# Valid Setup to BALE Inactive	t3a		2T		ns	
SA[19:0], SBHE# Valid Setup to MEMx# Active	t3b	2T	4T		ns	
SA[19:0], SBHE# Valid Setup to IOx# Active	t3c	4T	4T		ns	
SA[19:0], SBHE# Valid Hold from MEMx# Inactive	t3d		20T		ns	8-bit memory cycle
			10T		ns	16-bit memory cycle
SA[19:0], SBHE# Valid Hold from IOx# Inactive	t3e		32T		ns	8-bit I/O cycle
			20T		ns	16-bit I/O cycle
MEMR#, MEMW#, IOR#, and IOW#						
MEMx# Active Pulse Width (std)	t4a		18T		ns	8-bit memory cycle
			8T		ns	16-bit memory cycle
MEMx# Active Pulse Width (nws)	t4b		6T		ns	8-bit memory cycle
			4T		ns	16-bit memory cycle
IOx# Active Pulse (std)	t4c		18T		ns	8-bit I/O cycle
			6T		ns	16-bit I/O cycle
IOx# Active Pulse (nws)	t4d		6T		ns	8-bit I/O cycle
			6T		ns	16-bit I/O cycle
MEMx# Inactive Pulse Width	t4e	6T	6T		ns	8-bit memory cycle
		4T	4T		ns	16-bit memory cycle
IOX# Inactive Pulse Width	t4f	18T	18T		ns	8-bit I/O cycle
		18T	18T		ns	16-bit I/O cycle
SD[15:0]						
SD[15:0] Read Data Valid Setup to MEMR#	t5a	2T	2T		ns	
SD[15:0] Read Data Valid Setup to IOR#	t5b	2T	2T		ns	

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	COMMENTS
SD[15:0] Read Data Valid Hold from MEMR# Inactive	t5c	2T	2T		ns	
SD[15:0] Read Data Valid Hold from IOR# Inactive	t5d	2T	2T		ns	
SD[15:0] Write Data Valid Setup to MEMW# Active	t6a	2T	4T		ns	
SD[15:0] Write Data Valid setup to IOW# Active	t6b	4T	4T		ns	
SD[15:0] Write Data Valid Hold from MEMW# Inactive	t6c	2T	2T		ns	
SD[15:0] Write Data Valid Hold from IOW# Inactive	t6d	2T	2T		ns	

14. WAVEFORMS

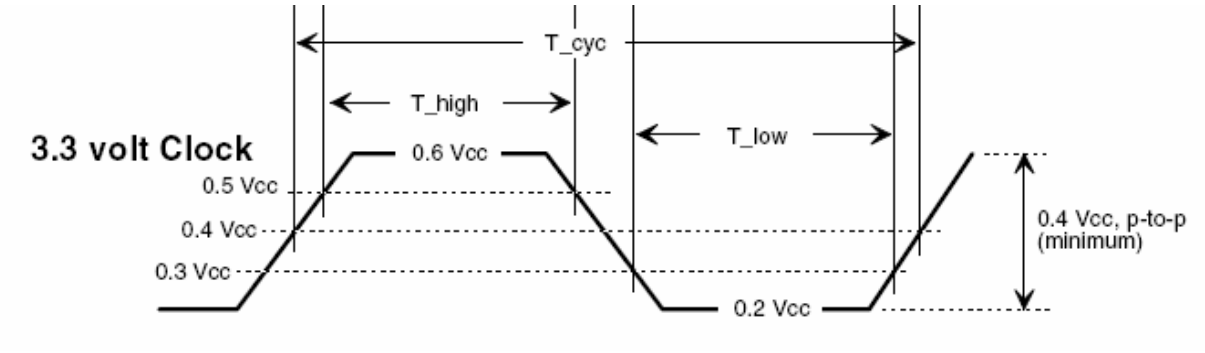


Figure 13-1: PCICLK Waveform

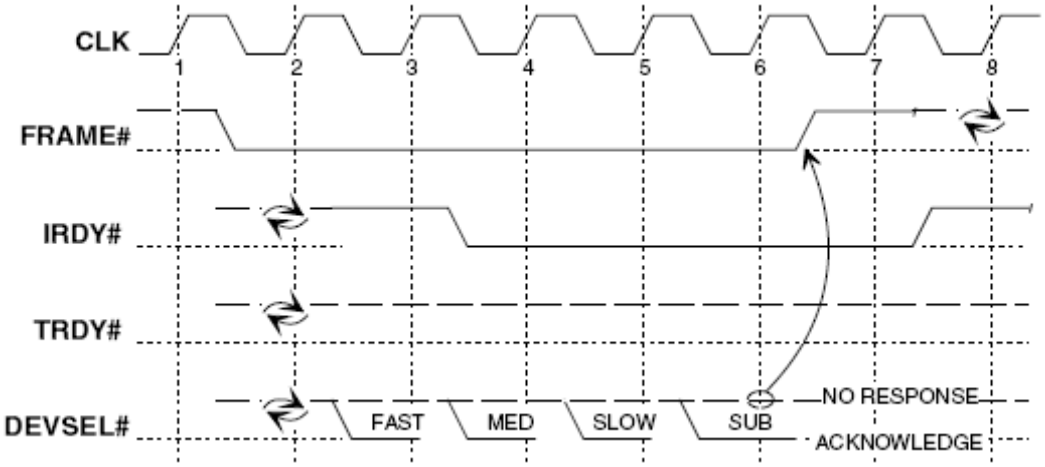


Figure 13-2: PCI DEVSEL# Timing Speed with Master Abort Termination

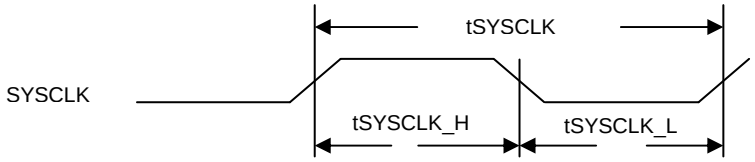


Figure 13-3: SYSCLK Waveform

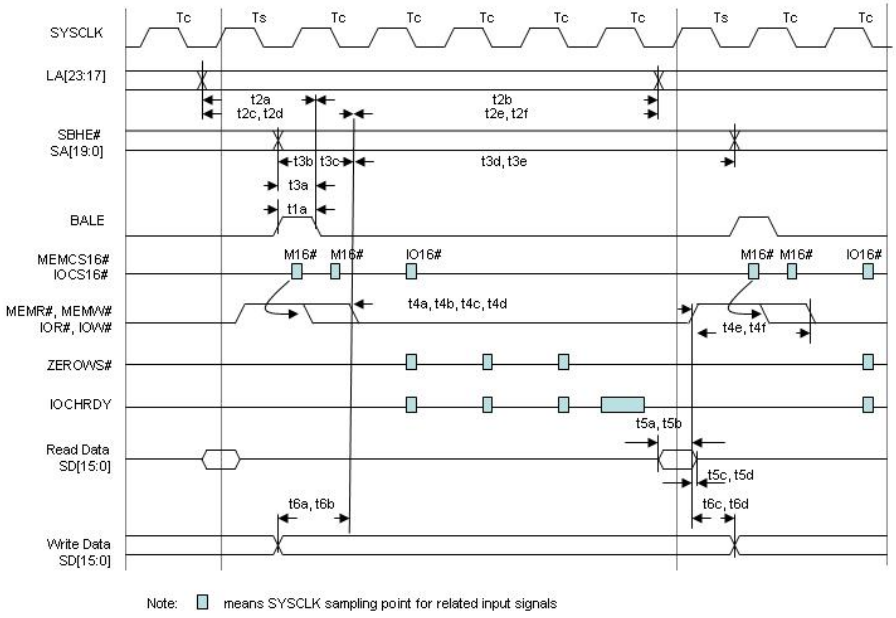


Figure 13-4: ISA Memory/I/O Read/Write Access Waveform

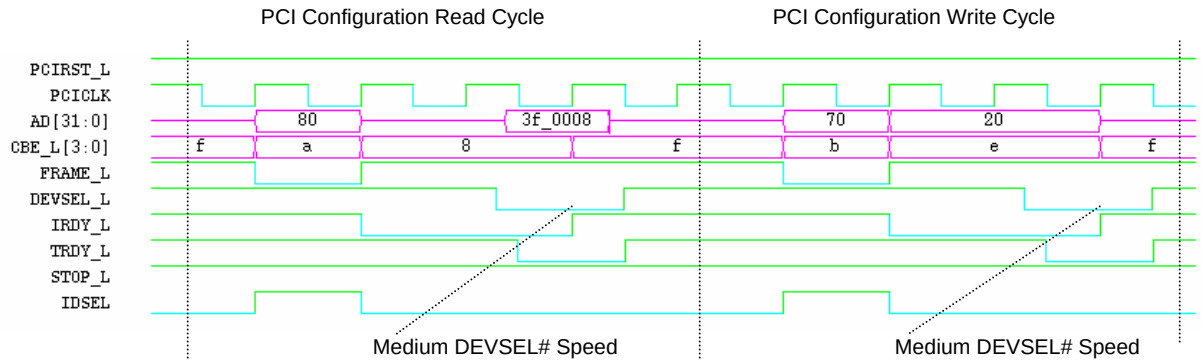


Figure 13-5: PCI Configuration Read/Write Cycle

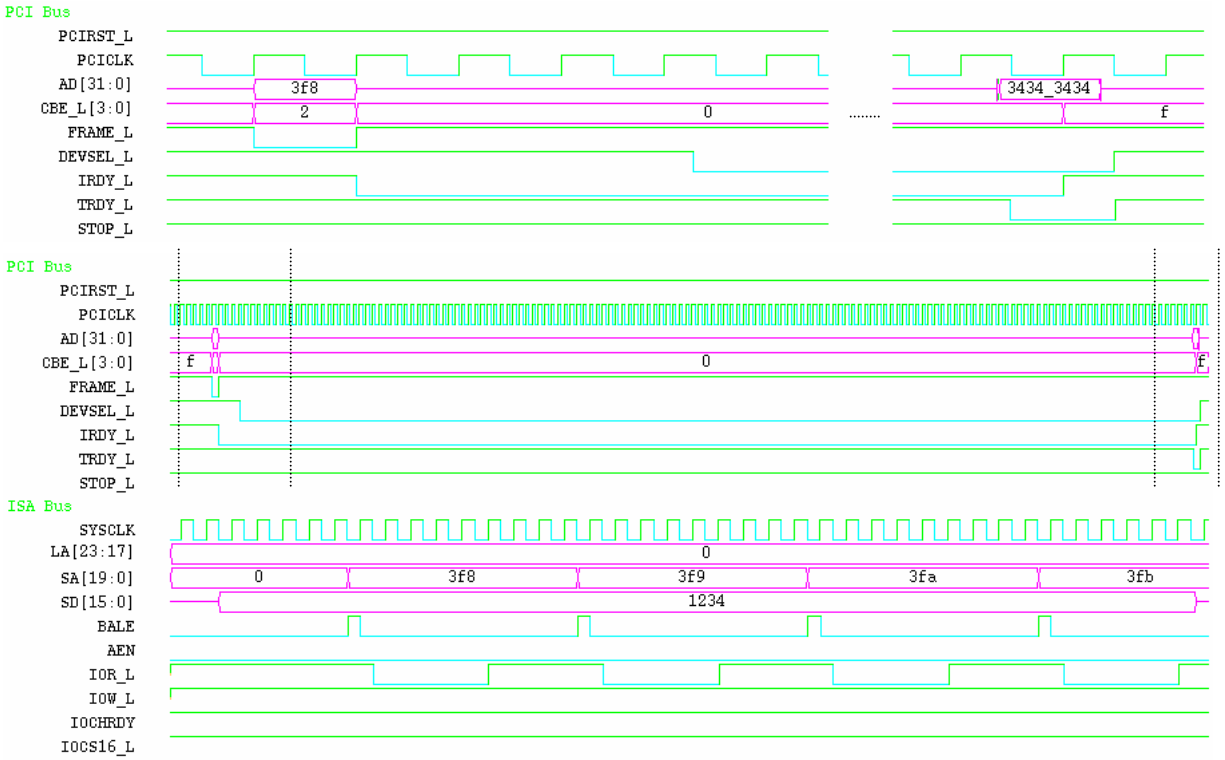


Figure 13-6: PCI I/O Read from 8-bit ISA Device
with SA=3f8h and BE#=0000b

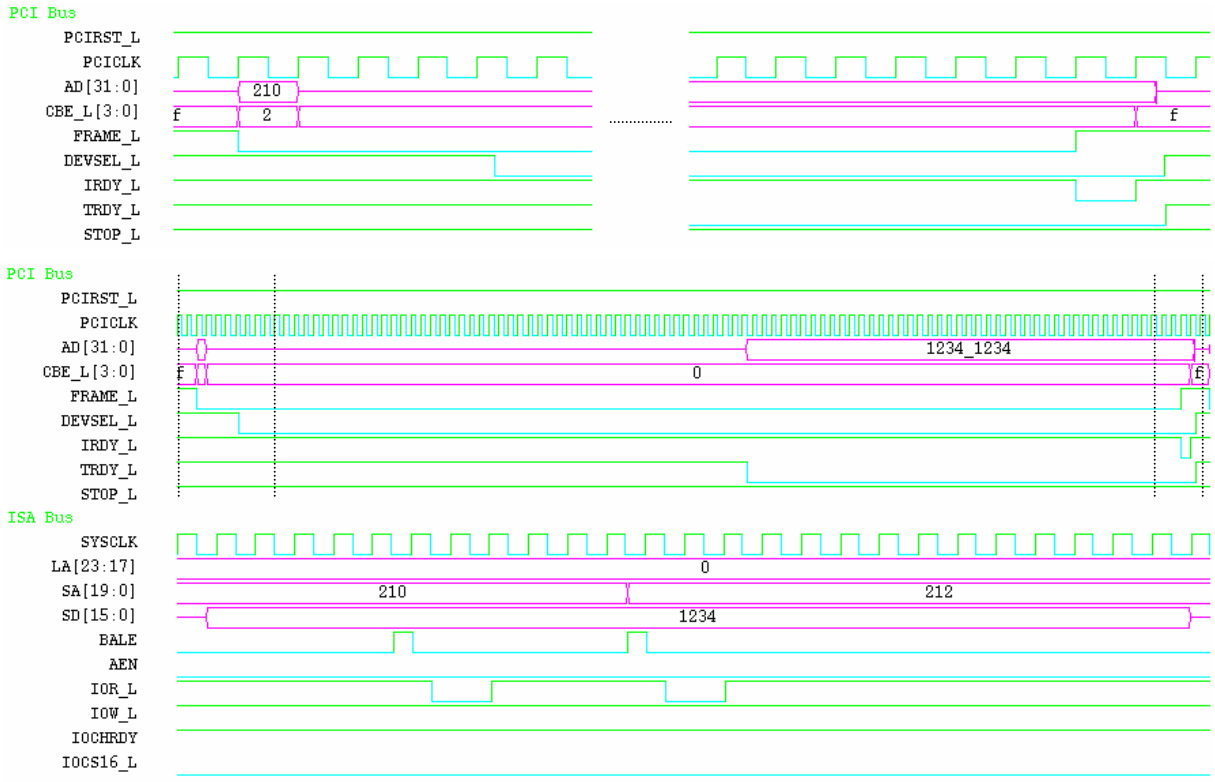


Figure 13-7: PCI I/O Read from 16-bit ISA Device
with SA=210h and BE#=0000b

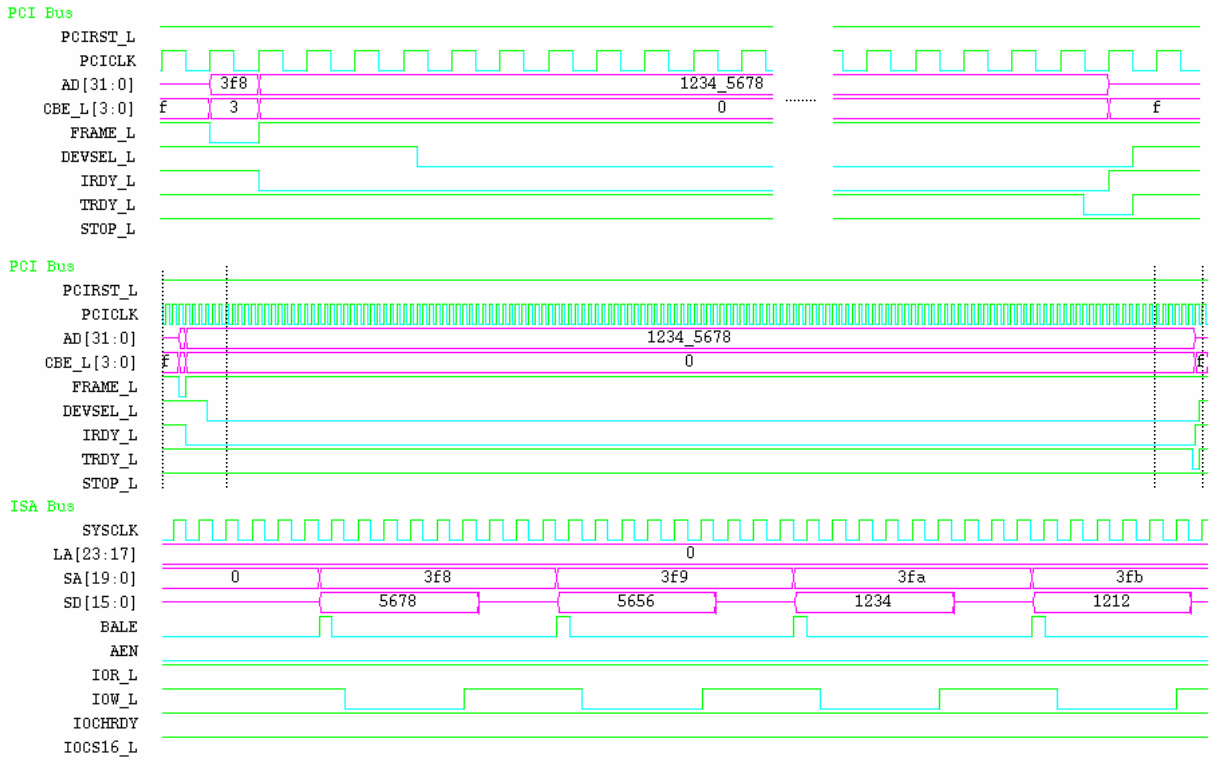


Figure 13-8: PCI I/O Write to 8-bit ISA Device
with Write Data = 1234_5678h, SA=3f8h, and BE#=0000b

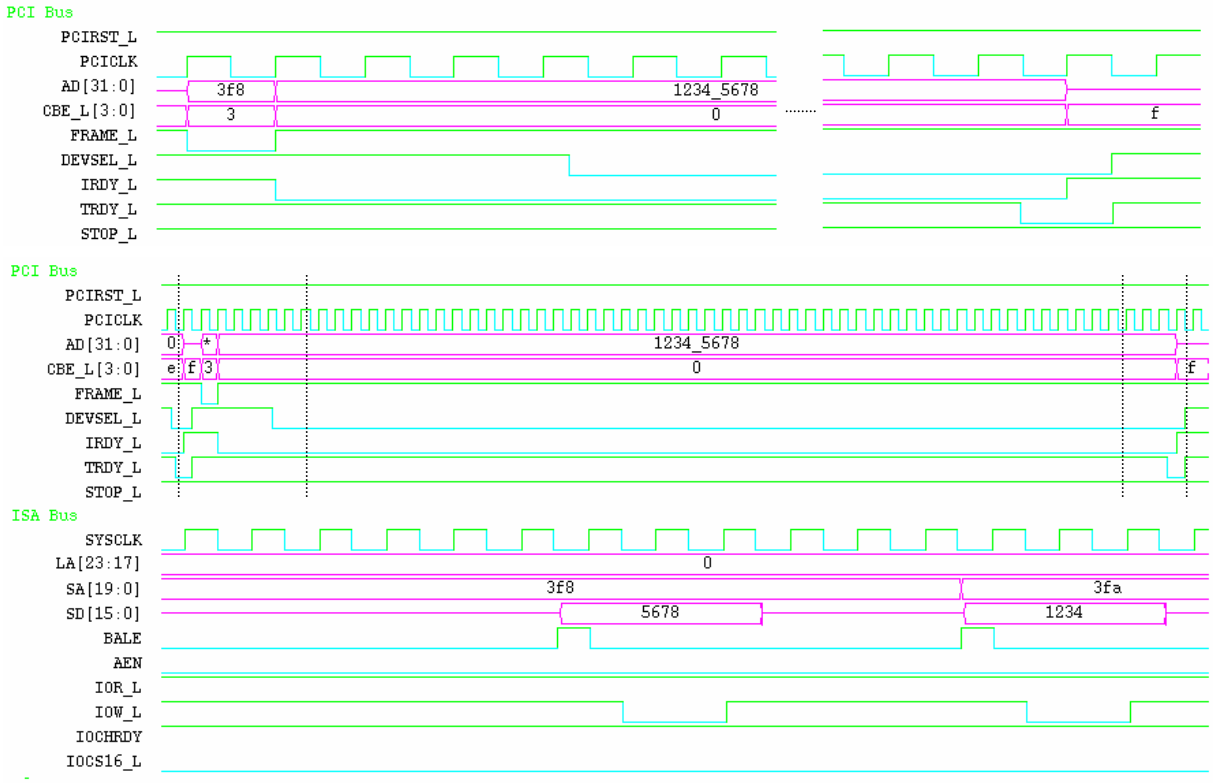


Figure 13-9: PCI I/O Write to 16-bit ISA Device
with Write Data = 1234_5678h, SA = 3f8h, and BE#=0000b

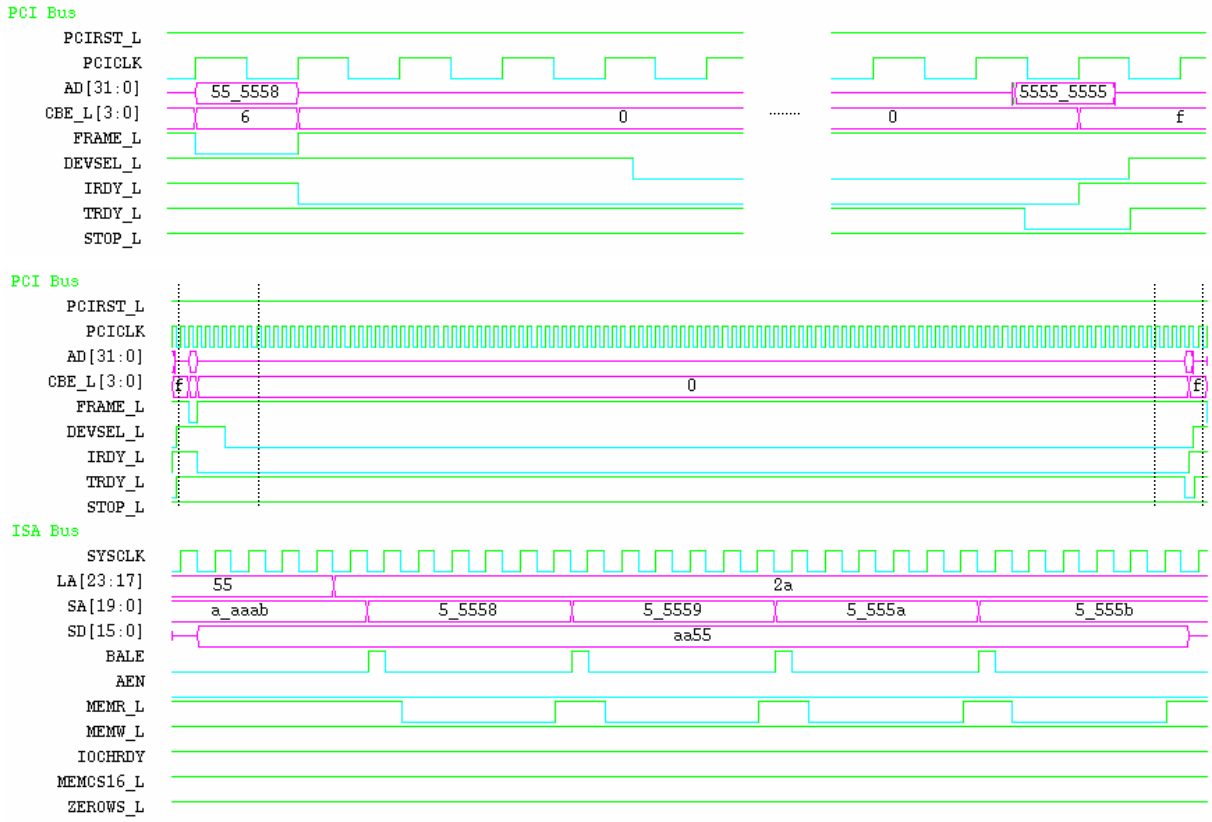


Figure 13-10: PCI Memory Read from 8-bit ISA Device
with SA=55_5558h and BE#=0000b

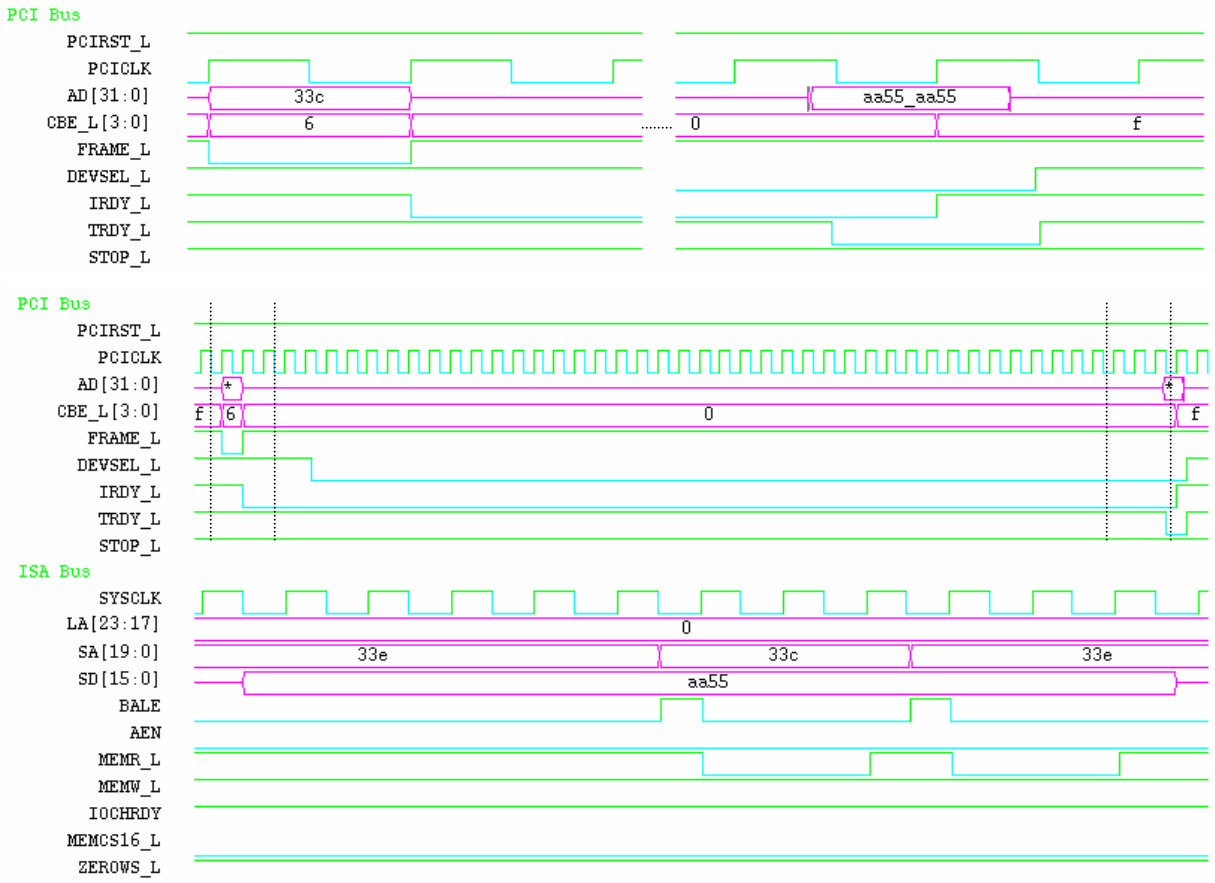


Figure 13-11: PCI Memory Read from 16-bit ISA Device
with SA=33ch and BE#=0000b

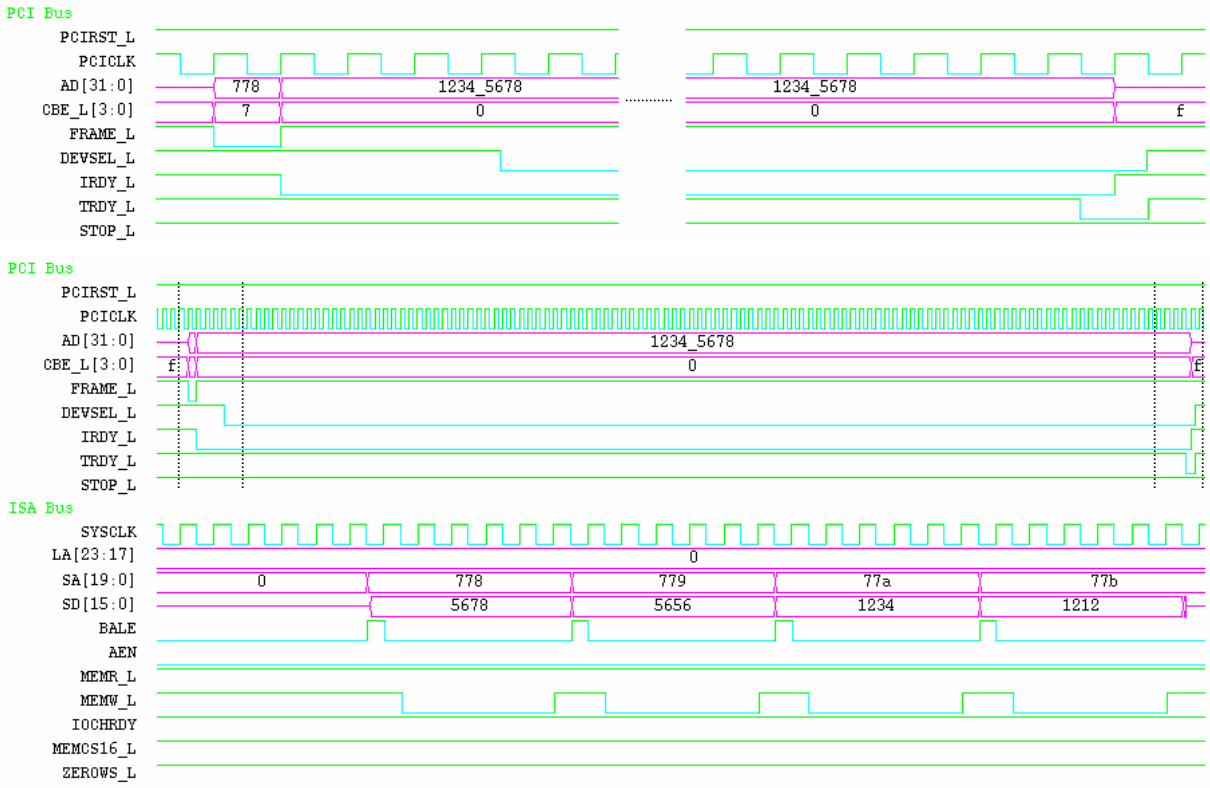


Figure 13-12: PCI Memory Write to 8-bit ISA Device
with Write Data=1234_5678h, SA=778h and BE#=0000b

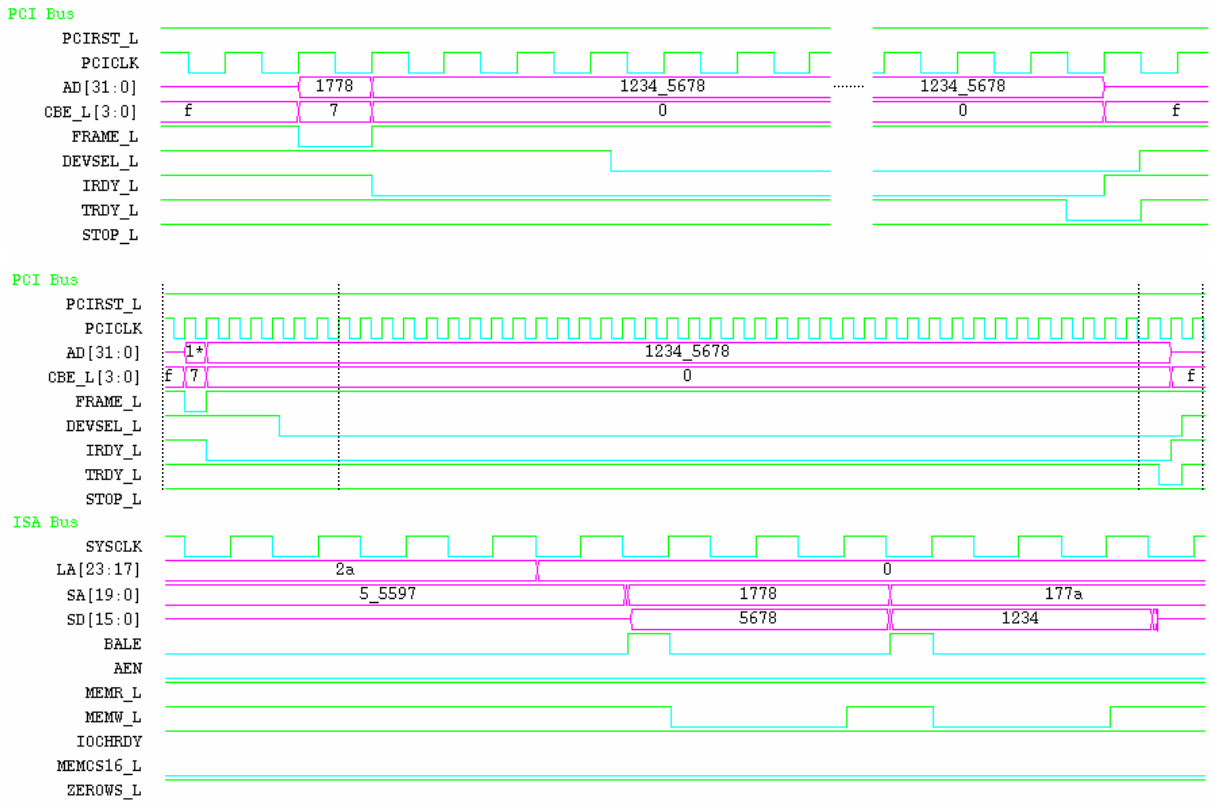


Figure 13-13: PCI Memory Write to 16-bit ISA Device
with Write Data = 1234_5678h, SA=1778h, and BE#=0000b

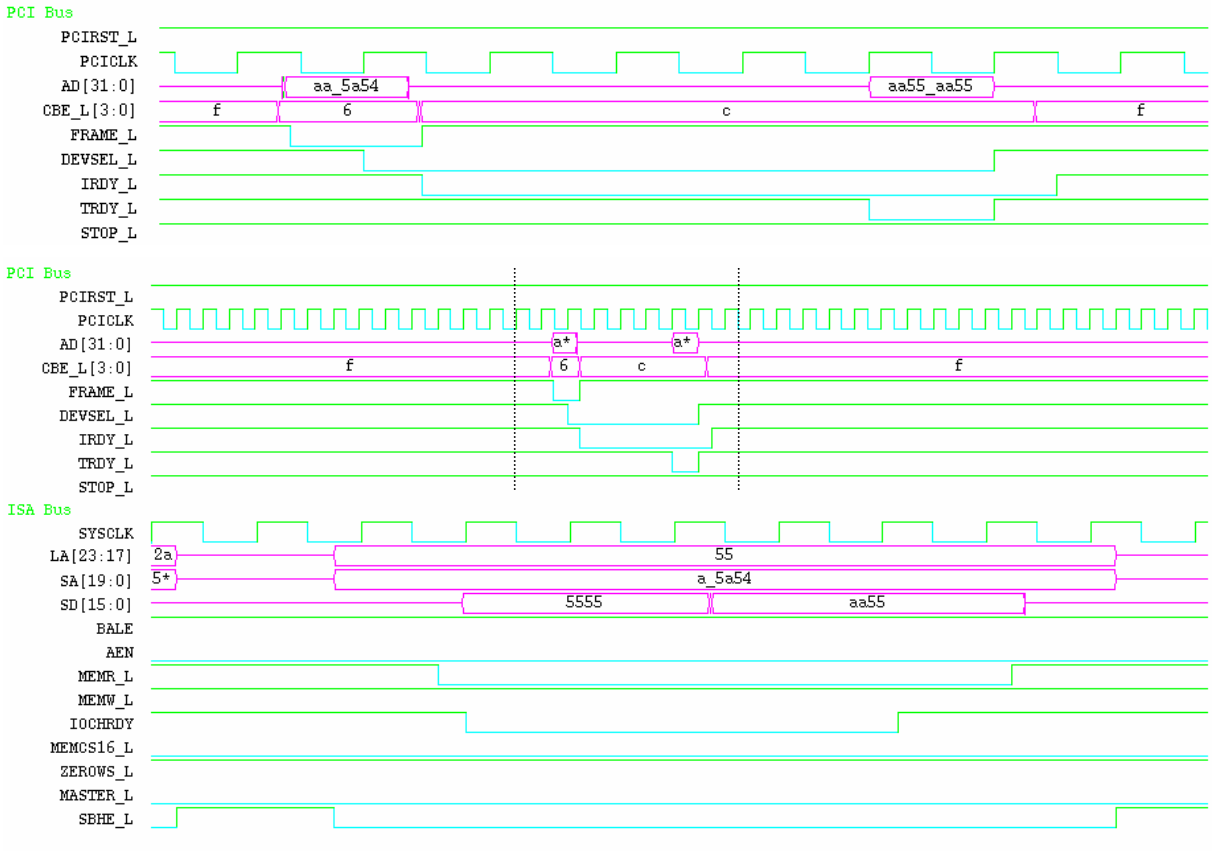


Figure 13-14: ISA Master Memory Read from PCI
with Even Address SA and SBHE#=0b

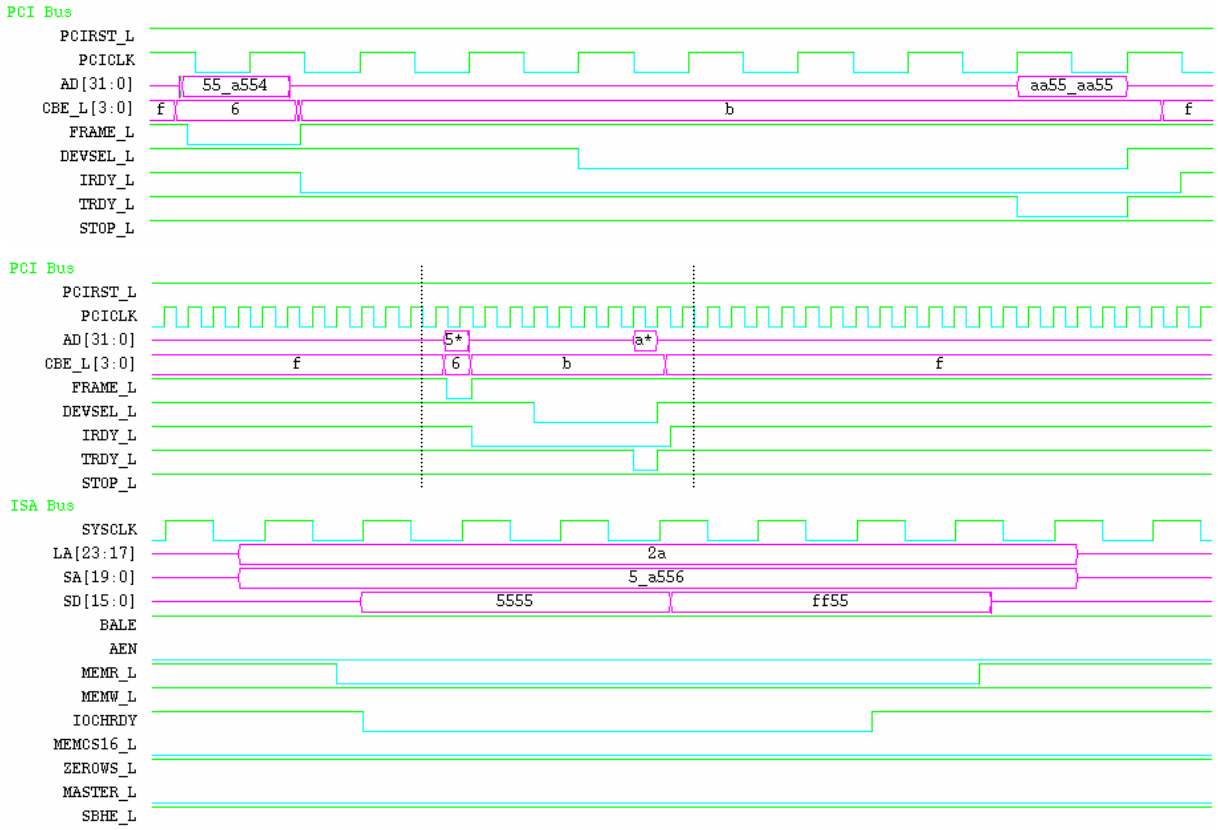


Figure 13-15: ISA Master Memory Read from PCI
with Even Address SA and SBHE#=1b

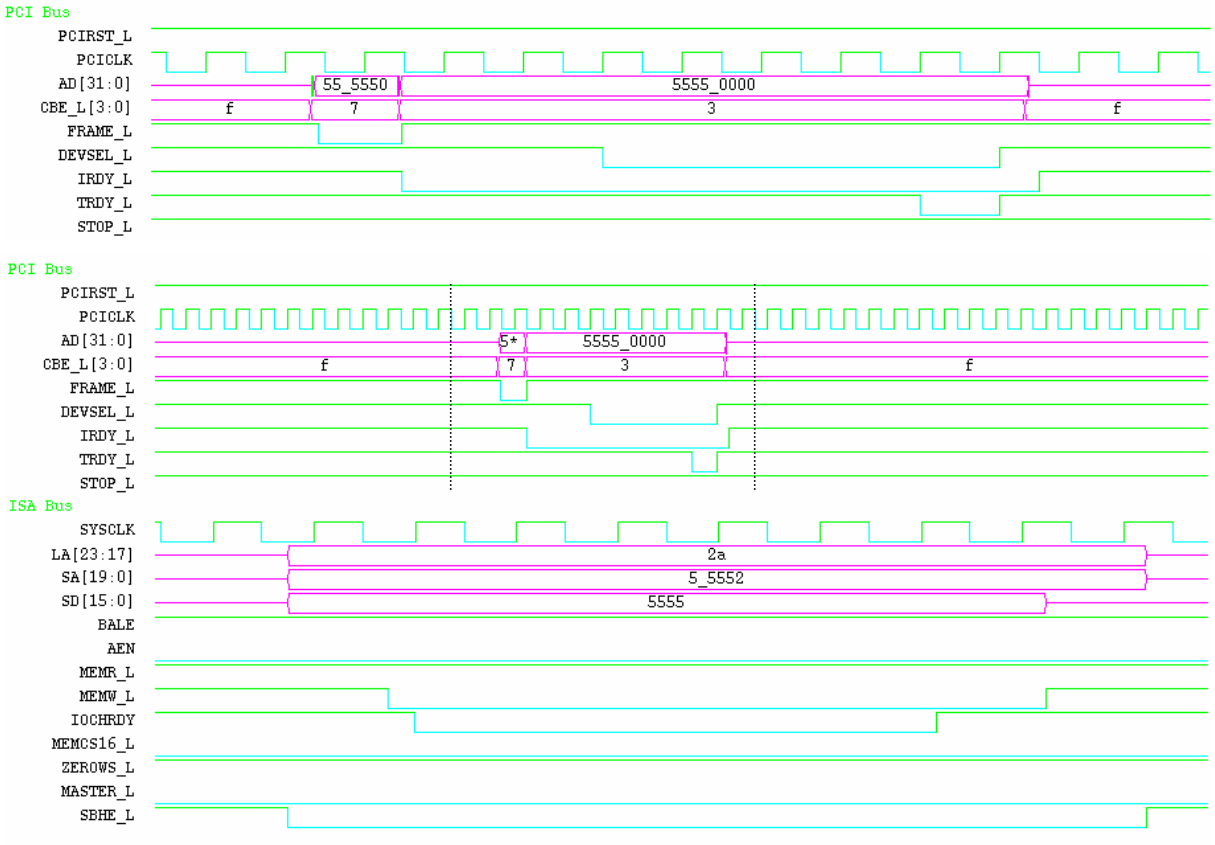


Figure 13-16: ISA Master Memory Write to PCI
with Even Address SA and SBHE#=0b

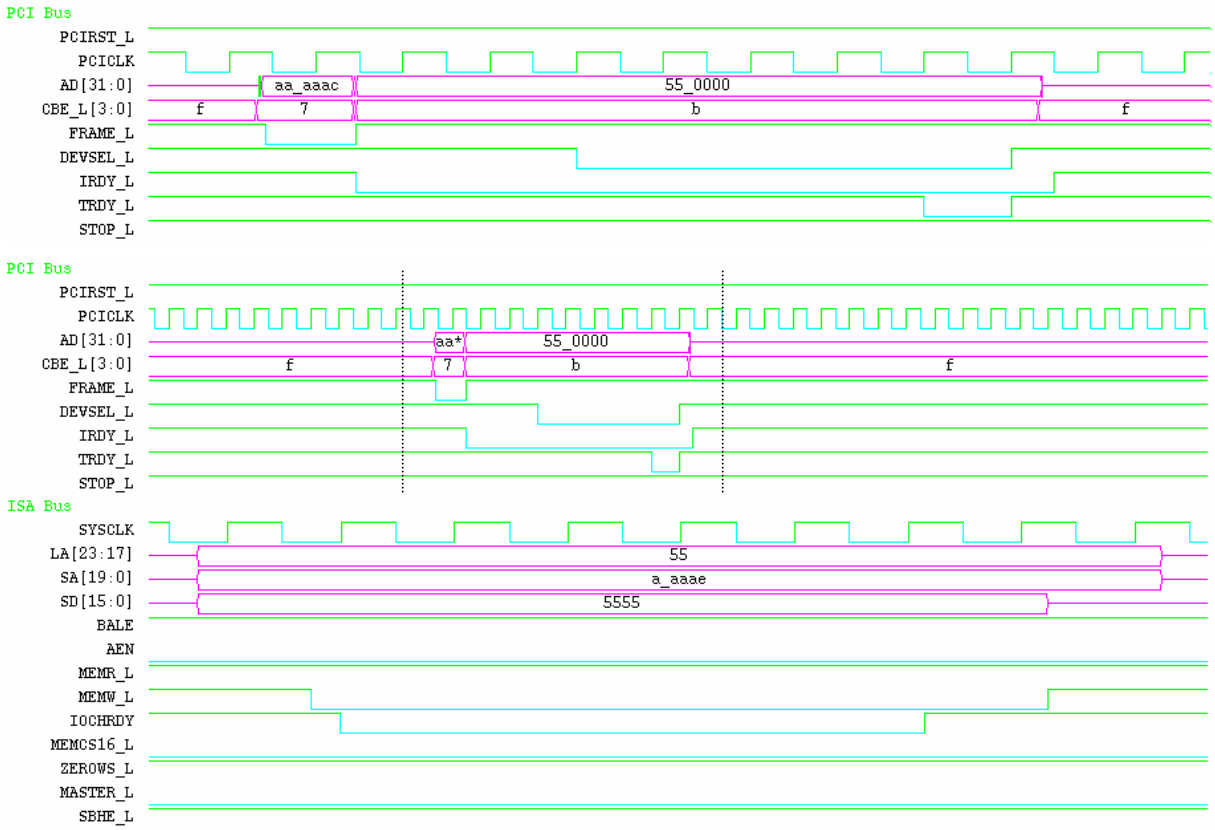


Figure 13-17: ISA Master Memory Write to PCI
with Even Address SA and SBHE#=1b

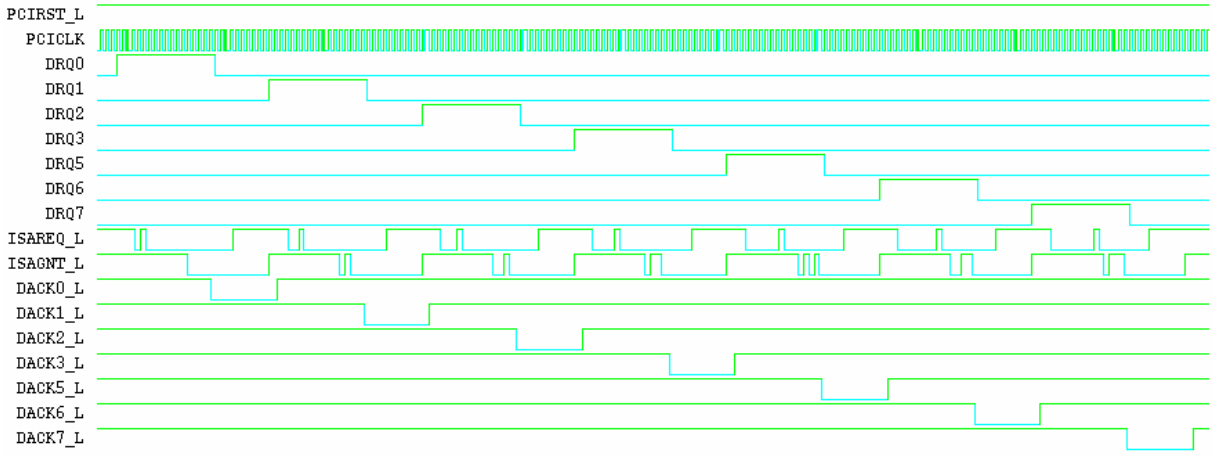


Figure 13-18: DRQn/DACKn# Coding in PC/PCI DMA Function

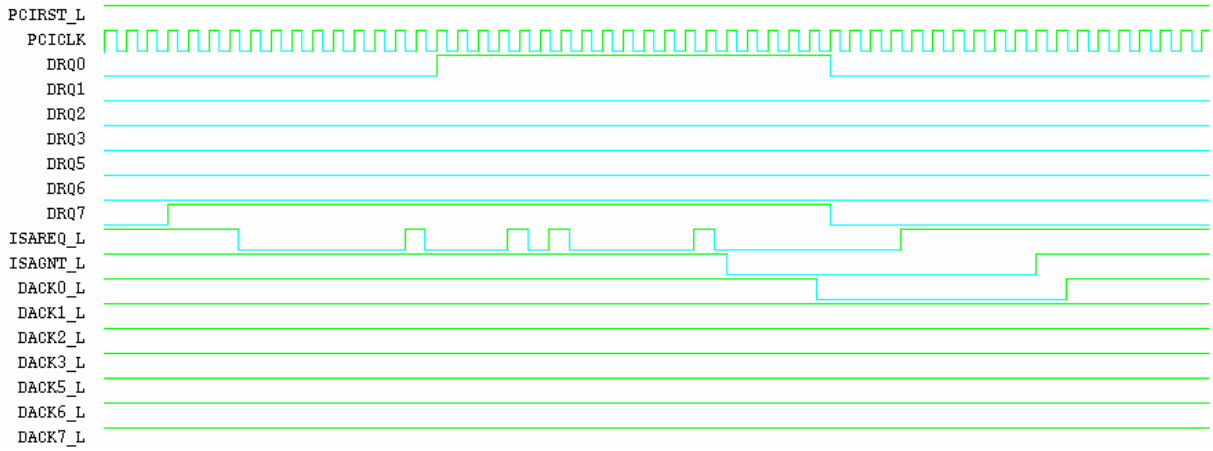


Figure 13-19: DRQn/DACKn# Coding in PC/PCI DMA Function
with Drive ISAREQ# Inactive for One Clock to Signal New Request Information

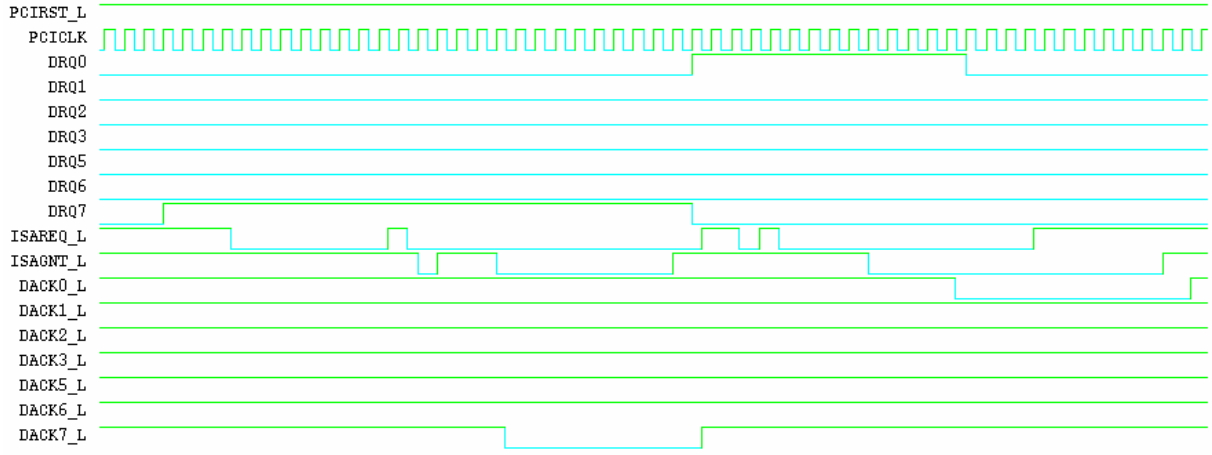
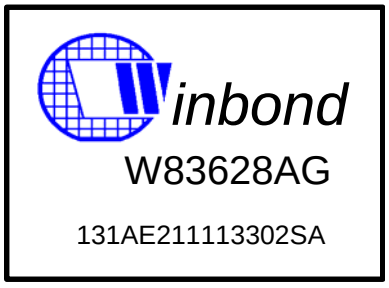
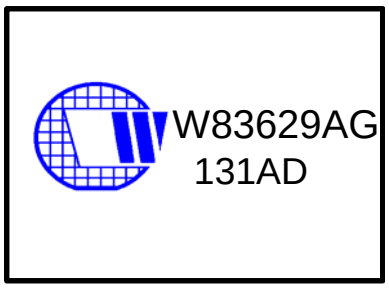


Figure 13-20: DRQn/DACKn# Coding in PC/PCI DMA Function
with Drive ISAREQ# Inactive for Two Clocks to Signal New Request Information (Previous DRQn had been granted the bus)

15. TOP MARKING SPECIFICATION

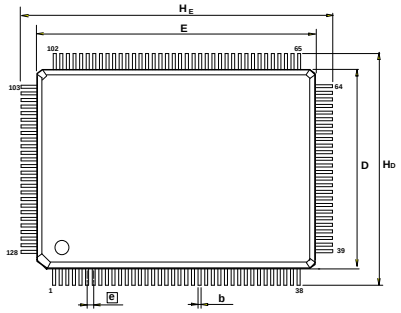


1st line: Chip logo
2nd line: The type number: W83628AG （**the "G" means Pb-free package**）
3th line: The tracking code 131 A E 211113302SA
131: Packages made in '01, week 31
A: Assembly house ID;
E: IC revision. A means version A; B means version B
21111330: Wafer production series lot number
2SA: Nuvoton internal use.



1nd line: The type number: W83629AG （**the "G" means Pb-free package**）
2th line: The tracking code 131 AD
131: Packages made in '01, week 31
A: Assembly house ID.
D: IC revision. A means version A; B means version B.

16. PACKAGE DIMENSIONS 1 FOR W83628AG (128-PIN PQFP)

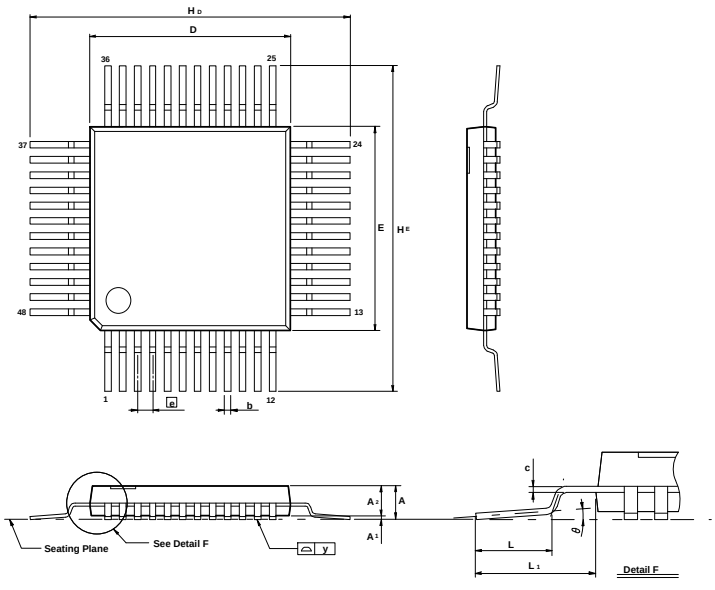


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:

1.Dimension D & E do not include interlead flash.
2.Dimension b does not include dambar protrusion/intrusion .
3.Controlling dimension : Millimeter
4.General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

17. PACKAGE DIMENSIONS 2 FOR W83629AG (48-PIN LQFP)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

Important Notice

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Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.