



UF840

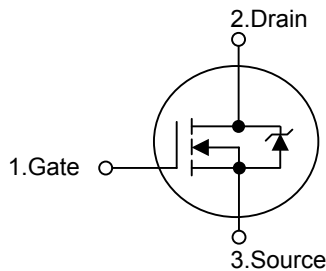
Power MOSFET

**8A, 500V, 0.85Ω, N-CHANNEL
POWER MOSFET****DESCRIPTION**

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

FEATURES

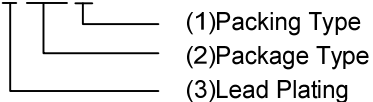
- * 8A, 500V, Low $R_{DS(ON)}=0.85\Omega$
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

SYMBOL**ORDERING INFORMATION**

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free Plating	Halogen Free		1	2	3	
UF840-TA3-T	UF840L-TA3-T	UF840G-TA3-T	TO-220	G	D	S	Tube
UF840-TF1-T	UF840L-TF1-T	UF840G-TF1-T	TO-220F1	G	D	S	Tube
UF840-TF3-T	UF840L-TF3-T	UF840G-TF3-T	TO-220F	G	D	S	Tube
UF840-TQ2-R	UF840L-TQ2-R	UF840G-TQ2-R	TO-263	G	D	S	Tape Reel
UF840-TQ2-T	UF840L-TQ2-T	UF840G-TQ2-T	TO-263	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

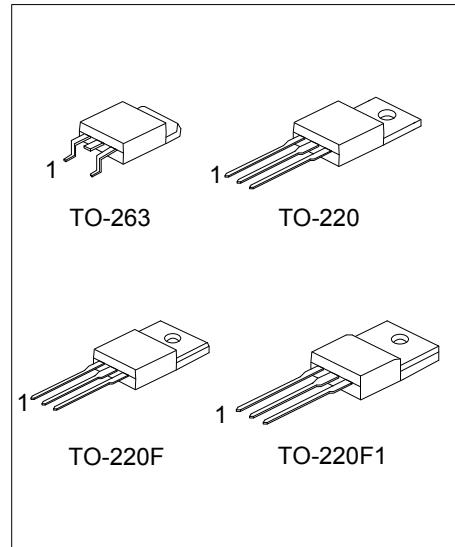
UF840L-TA3-T



(1) R: Tape Reel, T: Tube

(2) TA3: TO-220, TF1: TO-220F1, TF3: TO-220F
TQ2: TO-263

(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn



Lead-free: UF840L

Halogen-free: UF840G

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J = 25°C ~ 125°C)		V _{DSS}	500	V
Drain to Gate Voltage (R _{GS} = 20kΩ, T _J = 25°C ~ 125°C)		V _{DGR}	500	V
Gate to Source Voltage		V _{GSS}	±30	V
Drain Current	Continuous	I _D	8.0	A
	Pulsed	I _{DM}	32	A
Power Dissipation (T _C = 25°C)	TO-220	P _D	134	W
	TO-220F/TO-220F1		44	W
	TO-263		134	W
Single Pulse Avalanche Energy		E _{AS}	510	mJ
Operating Temperature		T _{OPR}	-55 ~ +150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ _{JA}	62.5	°C/W
	TO-220F/TO-220F1		62.5	°C/W
	TO-263		62.5	°C/W
Junction to Case	TO-220	θ _{JC}	0.93	°C/W
	TO-220F/TO-220F1		2.86	°C/W
	TO-263		0.93	°C/W

■ ELECTRICAL SPECIFICATIONS (T_a = 25°C, unless Otherwise Specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V	500			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA	2		4	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} > I _{D(ON)} × R _{DS(ON)MAX} , V _{GS} = 10V	8			A
Drain-Source Leakage Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			25	μA
		V _{DS} = 0.8 × Rated BV _{DSS} , V _{GS} = 0V, T _J = 125°C			250	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±30V			±100	nA
Static Drain-Source On-State Resistance (Note 1)	R _{DS(ON)}	I _D = 4.4A, V _{GS} = 10V		0.8	0.85	Ω
Turn-On Delay Time	t _{DLY(ON)}	V _{DD} = 250V, I _D ≈ 8A, R _G = 9.1Ω, R _L = 30Ω (Note 2)		15	21	ns
Turn-Off Delay Time	t _{DLY(OFF)}			50	74	ns
Turn-On Rise Time	t _R			21	35	ns
Turn-Off Fall Time	t _F			20	30	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, I _D = 8A, V _{DS} = 0.8 × Rated BV _{DSS} I _{G(REF)} = 1.5mA (Note 3)		42	63	nC
Gate-Source Charge	Q _{GS}			7		nC
Gate-Drain Charge	Q _{GD}			22		nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz		1225		pF
Output Capacitance	C _{OSS}			200		pF
Reverse Transfer Capacitance	C _{RSS}			85		pF

Note : 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

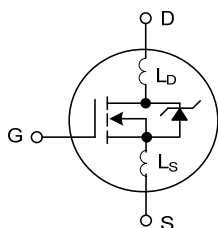
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Drain Inductance					
Measured from the contact screw on tab to center of die	L _D		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
Source Inductance					
Measured from the source lead(6mm from header) to source bond pad	L _S		7.5		nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

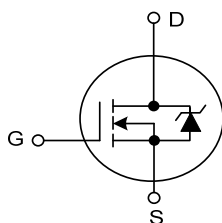


■ SOURCE TO DRAIN DIODE SPECIFICATIONS

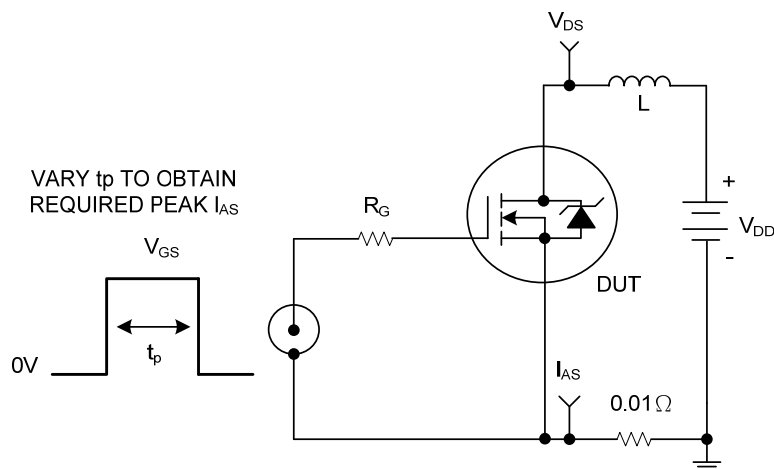
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage(Note 1)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $V_{GS} = 0\text{V}$			2	V
Continuous Source to Drain Current	I_{SD}	Note 2			8	A
Pulse Source to Drain Current	I_{SDM}				32	A
Reverse Recovery Time	t_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	210	475	970	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	2	4.6	8.2	μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

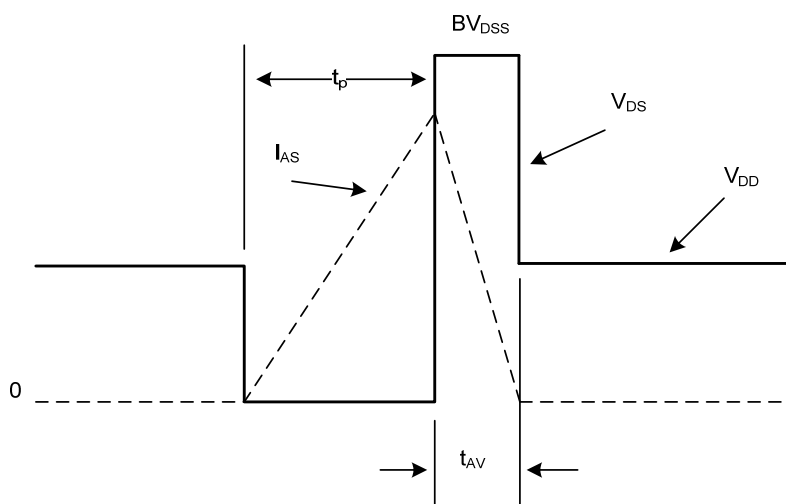
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



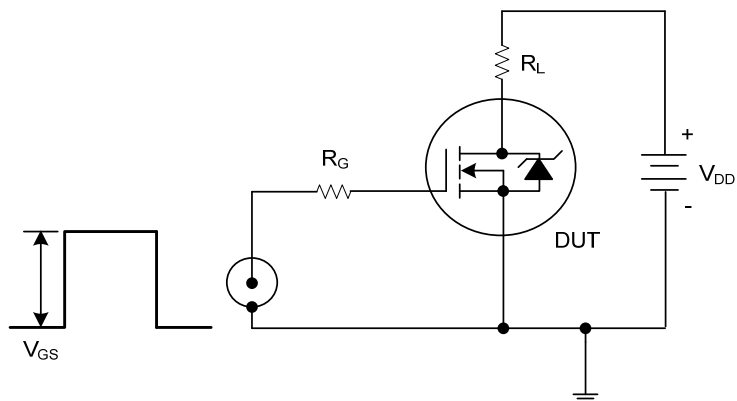
■ TEST CIRCUITS AND WAVEFORMS



UNCLAMPED ENERGY TEST CIRCUIT

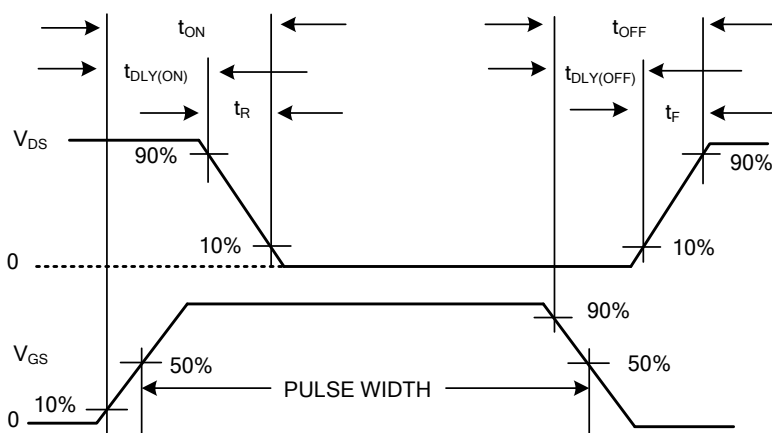


UNCLAMPED ENERGY WAVEFORMS

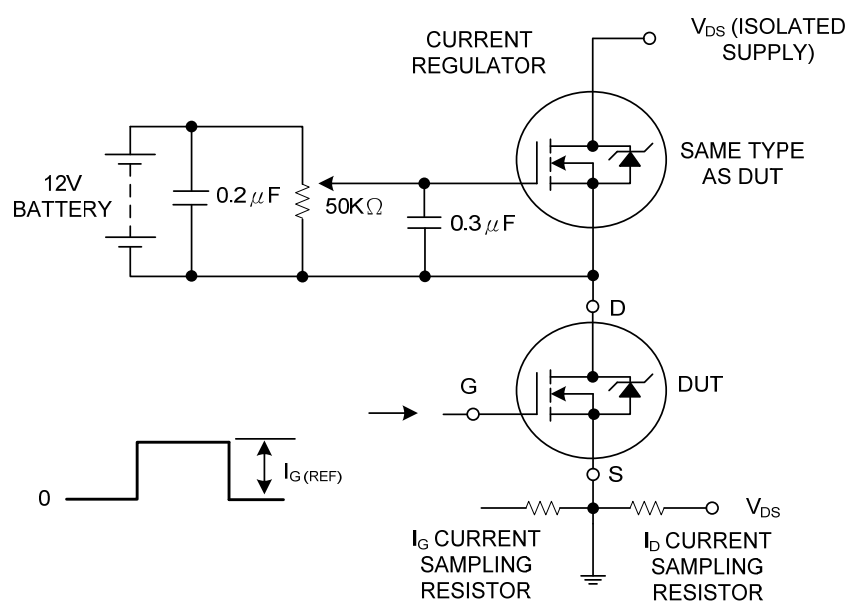


SWITCHING TIME TEST CIRCUIT

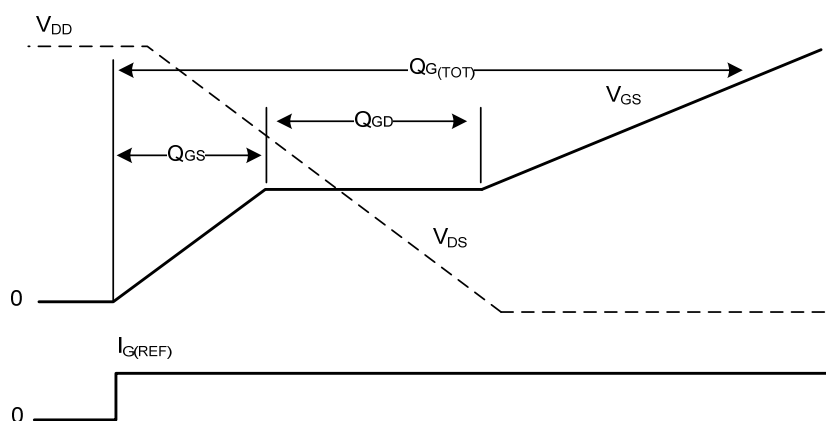
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



RESISTIVE SWITCHING WAVEFORMS

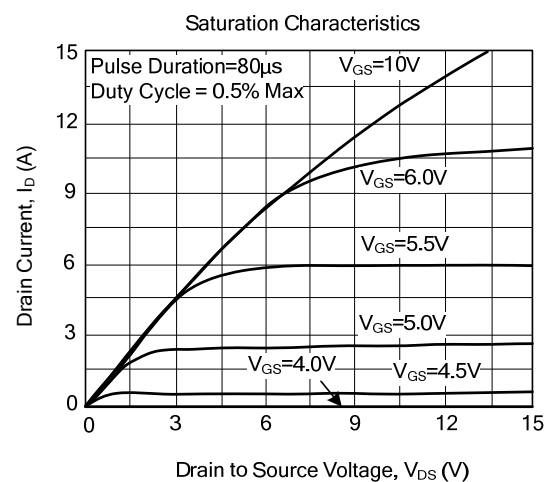
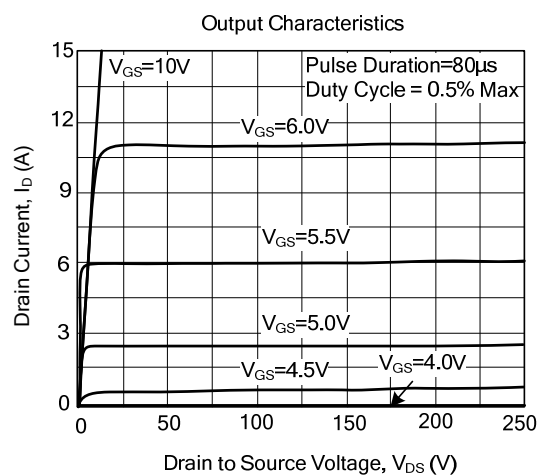
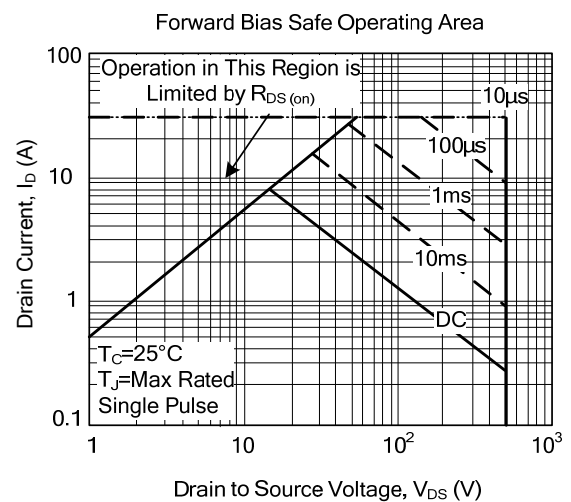
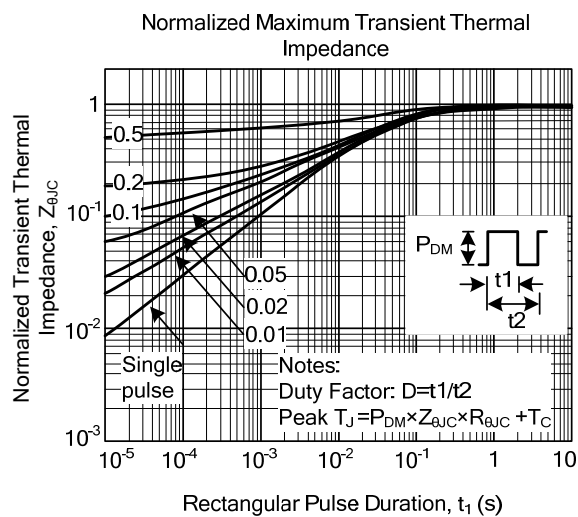
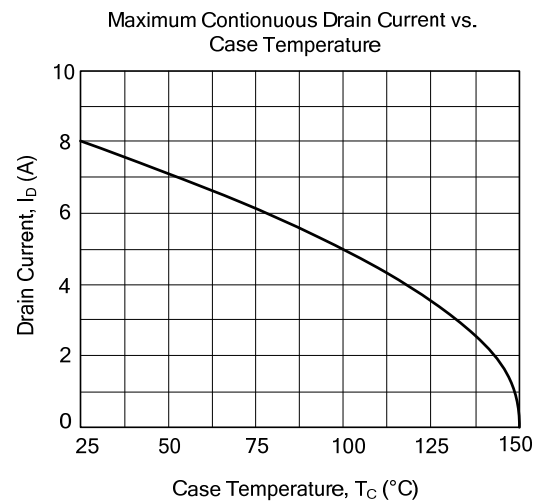
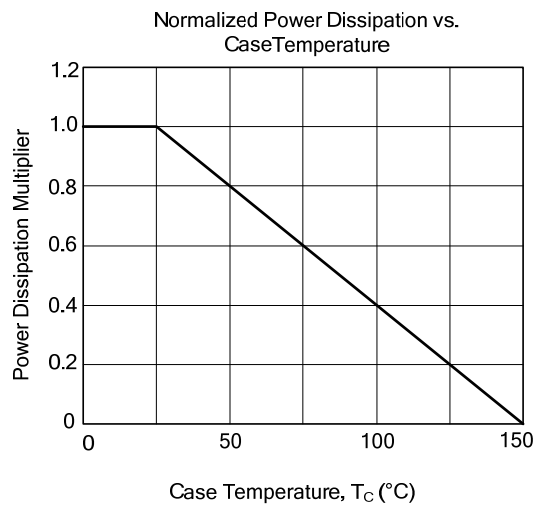


GATE CHARGE TEST CIRCUIT

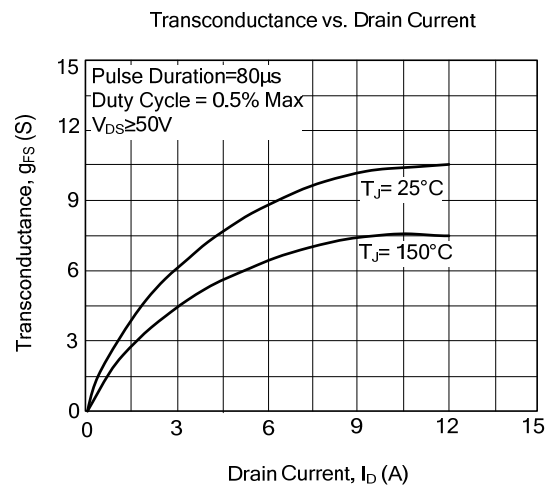
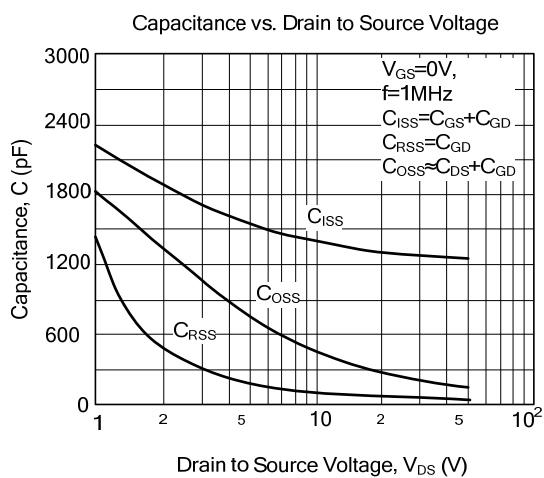
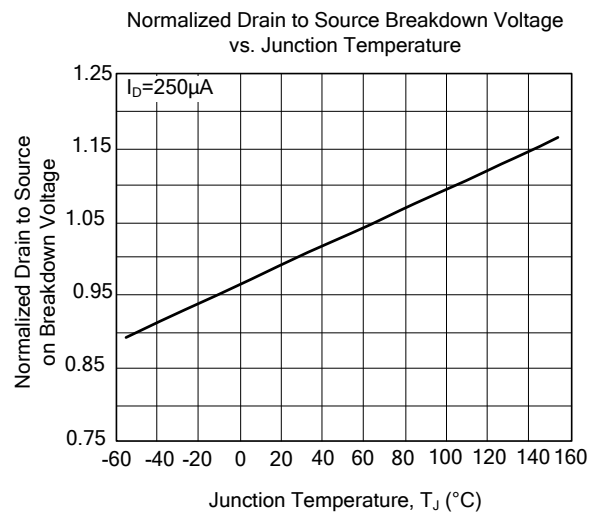
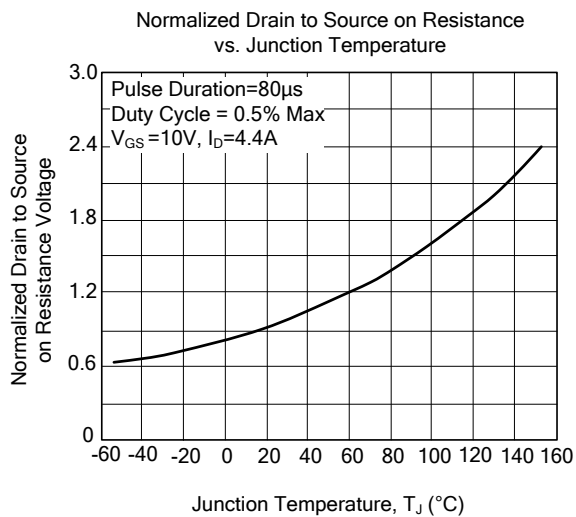
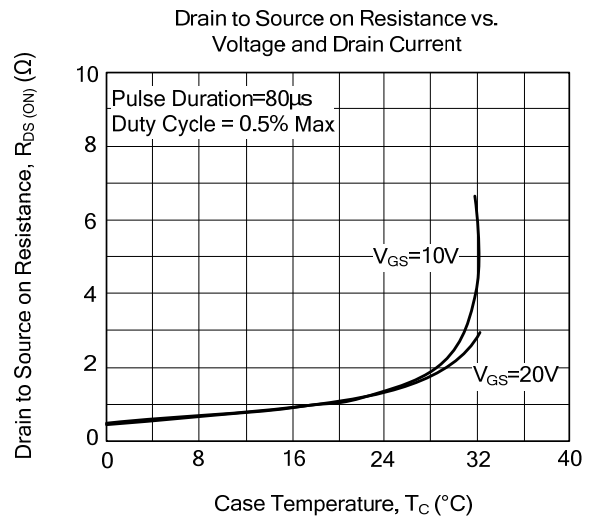
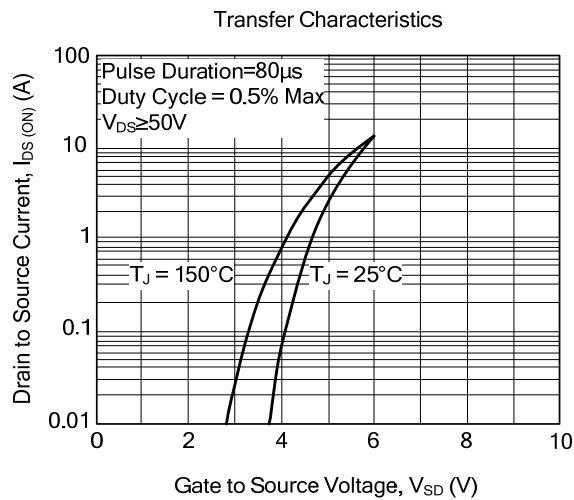


GATE CHARGE WAVEFORMS

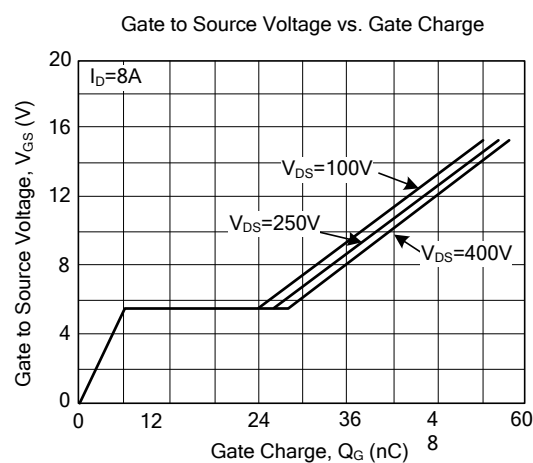
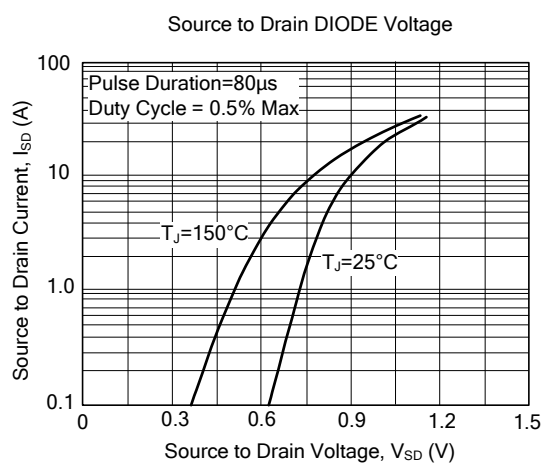
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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