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## FDMA520PZ

### Single P-Channel PowerTrench<sup>®</sup> MOSFET –20V, –7.3A, 30m $\Omega$

#### Features

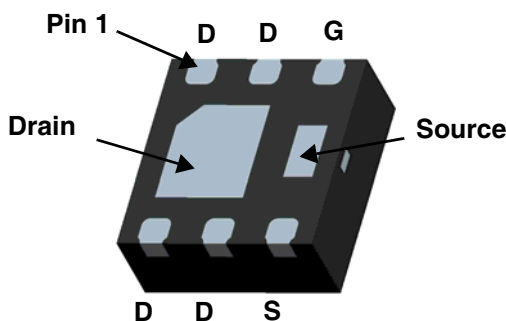
- Max  $r_{DS(on)}$  = 30m $\Omega$  at  $V_{GS} = -4.5V$ ,  $I_D = -7.3A$
- Max  $r_{DS(on)}$  = 53m $\Omega$  at  $V_{GS} = -2.5V$ ,  $I_D = -5.5A$
- Low profile - 0.8mm maximum - in the new package MicroFET 2X2 mm
- HBM ESD protection level > 3kV typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant



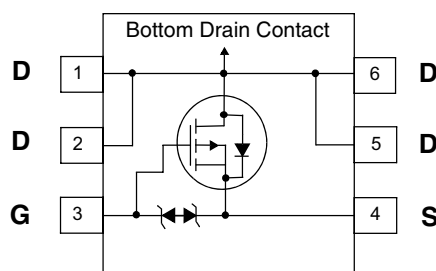
#### General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



#### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	–20	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current –Continuous (Note 1a)	–7.3	A
	–Pulsed	–24	
$P_D$	Power Dissipation (Note 1a)	2.4	W
	Power Dissipation (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
520	FDMA520PZ	MicroFET 2X2	7"	8mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-8.4		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V}$ , $V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$ , $V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\mu\text{A}$	-0.6	-1.1	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		3.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{V}$ , $I_D = -7.3\text{A}$		26	30	m $\Omega$
		$V_{GS} = -2.5\text{V}$ , $I_D = -5.5\text{A}$		42	53	
		$V_{GS} = -4.5\text{V}$ , $I_D = -7.3\text{A}$ , $T_J = 125^\circ\text{C}$		36	55	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{V}$ , $I_D = -7.3\text{A}$		22		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$		1235	1645	pF
$C_{oss}$	Output Capacitance			255	340	pF
$C_{rss}$	Reverse Transfer Capacitance			225	340	pF

**Switching Characteristics**

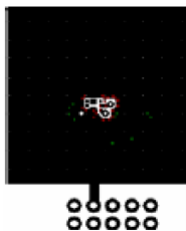
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{V}$ , $I_D = -7.3\text{A}$ $V_{GS} = -4.5\text{V}$ , $R_{GEN} = 6\Omega$		10	20	ns
$t_r$	Rise Time			29	47	ns
$t_{d(off)}$	Turn-Off Delay Time			83	133	ns
$t_f$	Fall Time			74	119	ns
$Q_g$	Total Gate Charge	$V_{DD} = -5\text{V}$ , $I_D = -7.3\text{A}$ $V_{GS} = -4.5\text{V}$		14	20	nC
$Q_{gs}$	Gate to Source Gate Charge			2.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			4.4		nC

**Drain-Source Diode Characteristics**

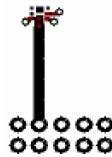
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-2	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = -2\text{A}$		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -7.3\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}$		30	45	ns
$Q_{rr}$	Reverse Recovery Charge			22	33	nC

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.



a.  $52^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $145^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3: The diode connected between the gate and the source serves only as protection against ESD. No gate overvoltage rating is implied.

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

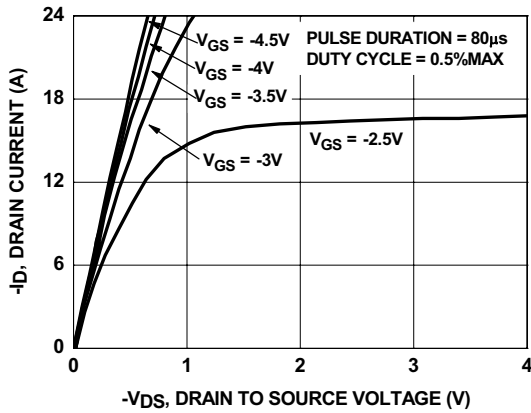


Figure 1. On-Region Characteristics

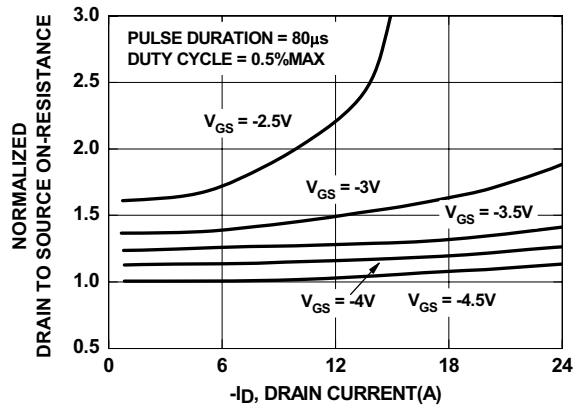


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

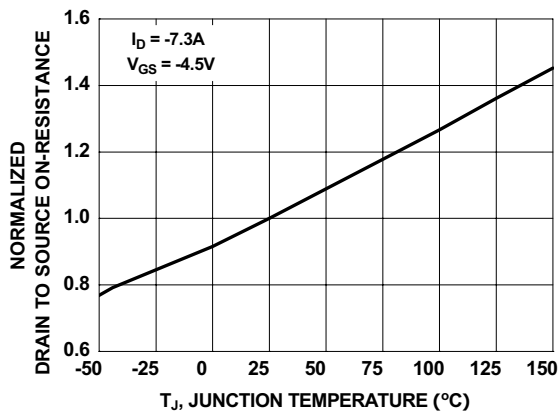


Figure 3. Normalized On-Resistance vs Junction Temperature

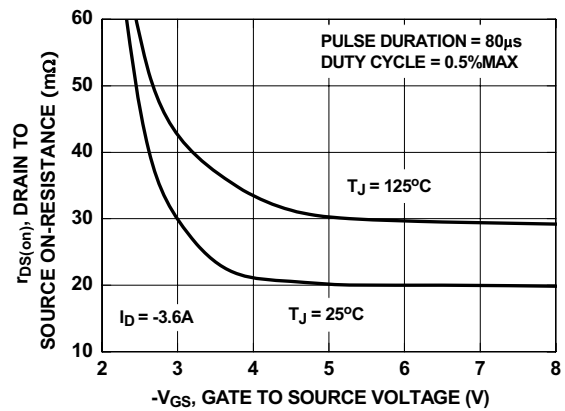


Figure 4. On-Resistance vs Gate to Source Voltage

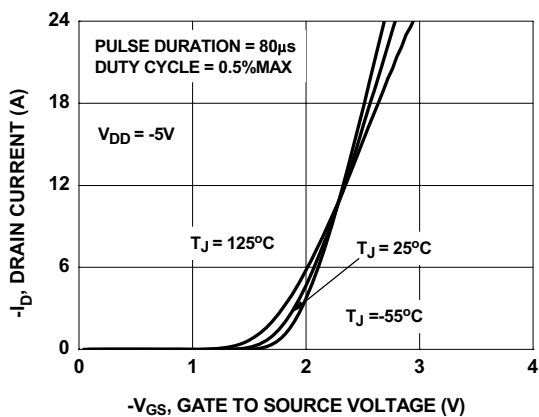


Figure 5. Transfer Characteristics

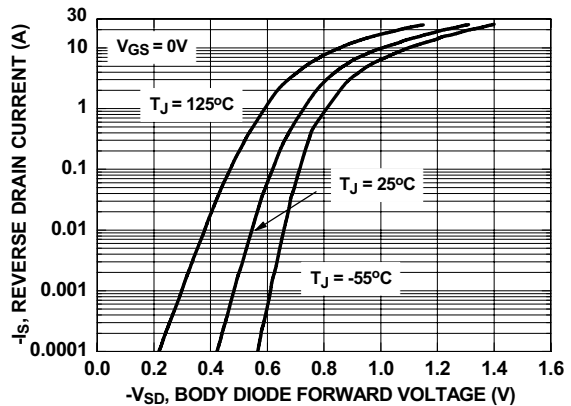


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

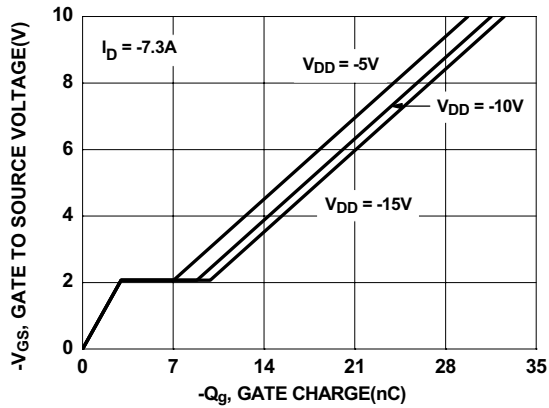


Figure 7. Gate Charge Characteristics

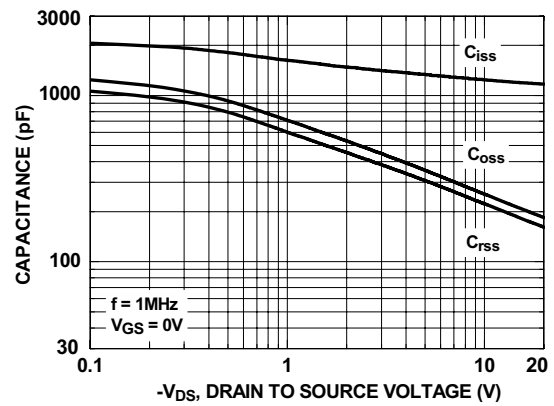


Figure 8. Capacitance vs Drain to Source Voltage

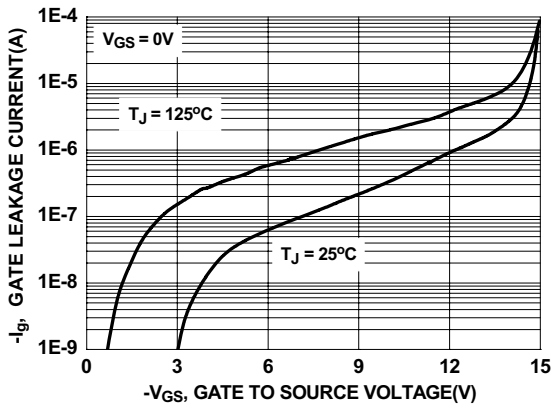


Figure 9. Gate Leakage Current vs Gate to Source Voltage

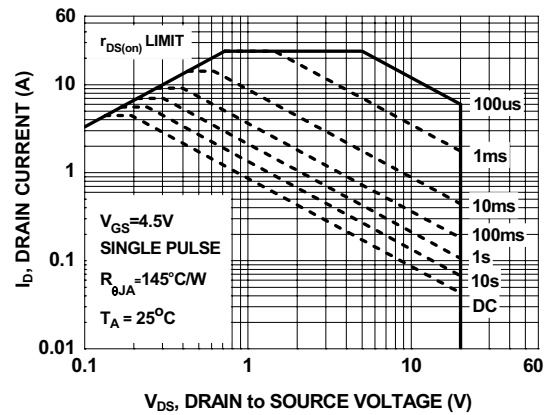


Figure 10. Forward Bias Safe Operating Area

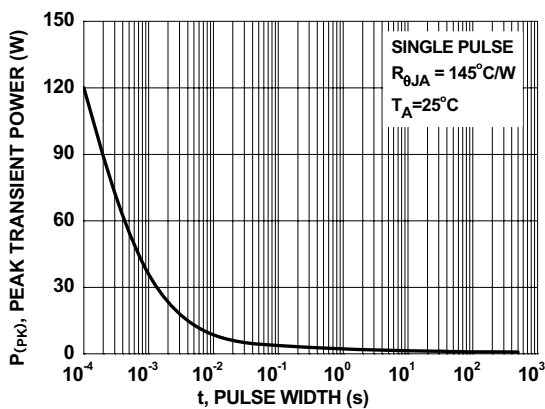


Figure 11. Single Pulse Maximum Power Dissipation

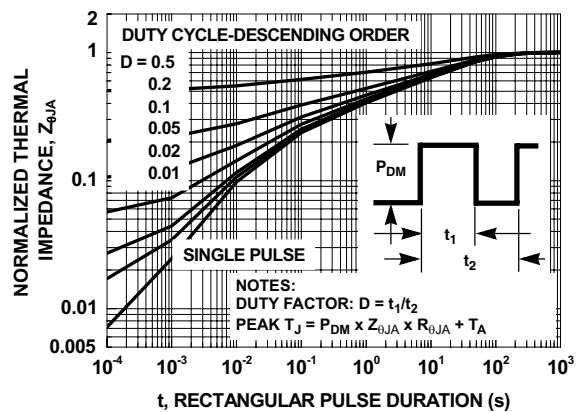
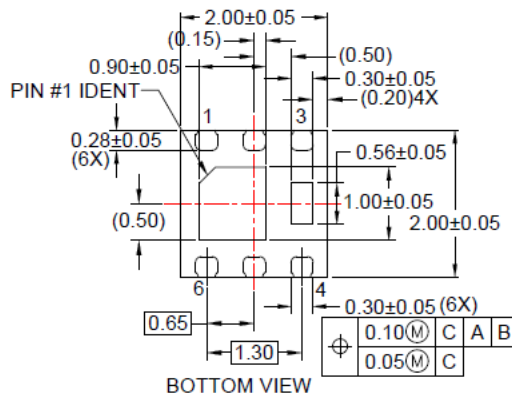
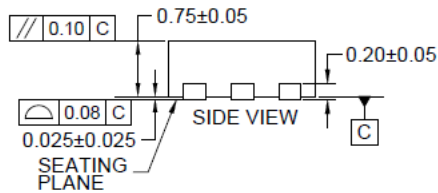
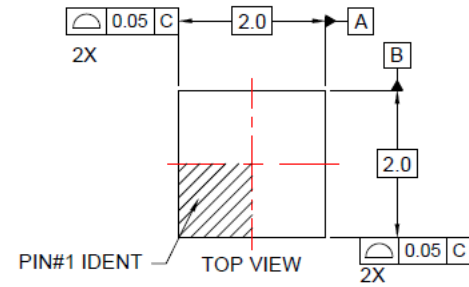


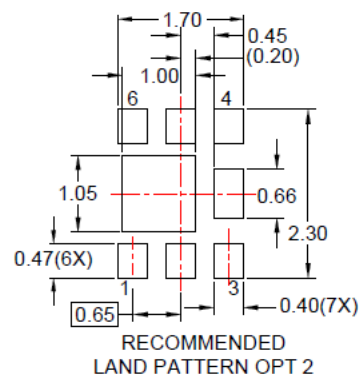
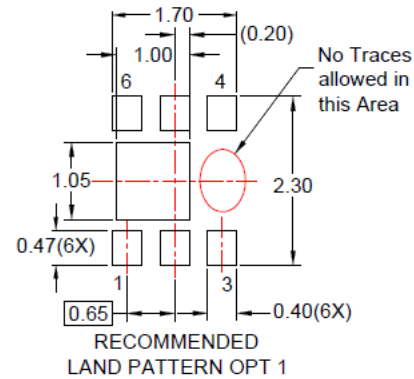
Figure 12. Transient Thermal Response Curve

## Dimensional Outline and Pad Layout



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- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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