

SILICON CONTROLLED RECTIFIER

Qualified per MIL-PRF-19500 / 276

Devices

Qualified Level

2N2323	2N2324	2N2326	2N2328	
2N2323S	2N2324S	2N2326S	2N2328S	2N2329
2N2323A	2N2324A	2N2326A	2N2328A	2N2329S
2N2323AS	2N2324AS	2N2326AS	2N2328AS	

JAN
JANTX
JANTXV

MAXIMUM RATINGS

Ratings	Sym	2N2323,S/ 2N2323A,S	2N2324,S/ 2N2324A,S	2N2326,S/ 2N2326A,S	2N2328,S/ 2N2328A,S	2N2329,S	Unit
Reverse Voltage	V_{RM}	50	100	200	300	400	Vdc
Working Peak Reverse Voltage	V_{RM}	75	150	300	400	500	Vpk
Forward Blocking Voltage	V_{FBXM}	50 ^(3/4)	100 ^(3/4)	200 ^(3/4)	300 ^(3/4)	400 ⁽³⁾	Vpk
Average Forward Current ⁽¹⁾	I_O	0.22					Adc
Forward Current Surge Peak ⁽²⁾	I_{FSM}	15					Adc
Cathode-Gate Current	V_{KGM}	6					Vpk
Operating Temperature	T_{op}	-65 to +125					°C
Storage Junction Temp	T_{stg}	-65 to +150					°C

- 1) This average forward current is for an ambient temperature of 80°C and 180 electrical degrees of conduction.
- 2) Surge current is non-recurrent. The rate of rise of peak surge current shall not exceed 40 A during the first 5 μ s after switching from the 'off' (blocking) to the 'on' (conducting) state. This is measured from the point where the thyristor voltage has decayed to 90% of its initial blocking value.
- 3) Gate connected to cathode through 1,000 ohm resistor.
- 4) Gate connected to cathode through 2,000 ohm resistor.



TO-5

*See appendix A
for package outline

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min.	Max.	Unit
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SUBGROUP 2 TESTING

Reverse Blocking Current $R_2 = 1 \text{ k}\mu$ $R_2 = 2 \text{ k}\mu$ $V_R = 50 \text{ Vdc}$ $V_R = 100 \text{ Vdc}$ $V_R = 200 \text{ Vdc}$ $V_R = 300 \text{ Vdc}$ $V_R = 400 \text{ Vdc}$	2N2323 thru 2N2329 2N2323S thru 2N2329S 2N2323A thru 2N2328A 2N2323AS thru 2N2328AS 2N2323, S, A, AS 2N2324, S, A, AS 2N2326, S, A, AS 2N2328, S, A, AS 2N2329, S,	I_{RBX1}	10	μAdc
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2N2323, A, AS, S; 2N2324, A, AS, S; 2N2326, A, AS, S; 2N2328, A, AS, S; 2N232, S JAN SERIES

ELECTRICAL CHARACTERISTICS (con't)

Characteristics	Symbol	Min.	Max.	Unit
Forward Blocking Current $R_2 = 1\text{ k}\Omega$ 2N2323 thru 2N2329 2N2323S thru 2N2329S $R_2 = 2\text{ k}\Omega$ 2N2323A thru 2N2328A 2N2323AS thru 2N2328AS $V_R = 50\text{ Vdc}$ 2N2323, S, A, AS $V_R = 100\text{ Vdc}$ 2N2324, S, A, AS $V_R = 200\text{ Vdc}$ 2N2326, S, A, AS $V_R = 300\text{ Vdc}$ 2N2328, S, A, AS $V_R = 400\text{ Vdc}$ 2N2329, S	I_{FBX1}		10	μAdc
Reverse Gate Current $V_{KG} = 6\text{ Vdc}$	I_{KG}		200	μAdc
Gate Trigger Voltage and Current $V_2 = V_{FBX} = 6\text{ Vdc}$; $R_L = 100\text{ }\Omega$ $R_e = 1\text{ k}\Omega$ 2N2323 thru 2N2329 and 2N2323S thru 2N2329S $R_e = 2\text{ k}\Omega$ 2N2323A thru 2N2328A and 2N2323AS thru 2N2328AS	V_{GT1} I_{GT1} V_{GT1} I_{GT1}	0.35 0.35	0.80 200 0.60 20	Vdc μAdc Vdc μAdc

SUBGROUP 4 TESTING

Exponential Rate of Voltage Rise $T_A = 125^\circ\text{C}$ $50\text{ }\Omega \leq R_L \leq 400\text{ }\Omega$, $C = 0.1\text{ to }1.0\text{ }\mu\text{F}$, repetition rate = 60 pps, test duration = 15 seconds $dv/dt = 1.8\text{ v}/\mu\text{s}$, $R_3 = 1\text{ k}\Omega$ 2N2323 thru 2N2329 and 2N2323S thru 2N2329S $dv/dt = 0.7\text{ v}/\mu\text{s}$, $R_3 = 2\text{ k}\Omega$ 2N2323A thru 2N2328A and 2N2323AS thru 2N2328AS $V_{AA} = 50\text{ Vdc}$ 2N2323, S, A, AS $V_{AA} = 100\text{ Vdc}$ 2N2324, S, A, AS $V_{AA} = 200\text{ Vdc}$ 2N2326, S, A, AS $V_{AA} = 300\text{ Vdc}$ 2N2328, S, A, AS $V_{AA} = 400\text{ Vdc}$ 2N2329, S	V_{FBX}	47 95 190 285 380		Vdc
Forward "on" Voltage $i_{FM} = 4\text{a (pk)}$ (pulse), pulse width = 8.5 ms, max; duty cycle = 2% max	V_{FM}		2.2	V(pk)
Holding Current $V_{AA} = 24\text{ Vdc}$ max, $I_{F1} = 100\text{ mAdc}$, $I_{F2} = 10\text{ mAdc}$ Gate trigger source voltage = 6 Vdc, trigger pulse width = 25 μs min., $R_2 = 330\text{ }\Omega$ $R_3 = 1\text{ k}\Omega$ 2N2323 thru 2N2329 and 2N2323S thru 2N2329S $R_3 = 2\text{ k}\Omega$ 2N2323A thru 2N2328A and 2N2323AS thru 2N2328AS	I_{HOX}		2.0	mAdc