SM72441 Programmable Maximum Power Point Tracking Controller for Photovoltaic Solar Panels

Check for Samples: SM72441

FEATURES

- **Renewable Energy Grade**
- **Programmable Maximum Power Point Tracking**
- **Photovoltaic Solar Panel Voltage and Current Diagnostic**
- **Single Inductor Four Switch Buck-boost Converter Control**
- **VOUT Overvoltage Protection**
- **Over-Current Protection**

PACKAGE

- **TSSOP-28**

DESCRIPTION

The SM72441 is a programmable MPPT controller capable of controlling four PWM gate drive signals for a 4-switch buck-boost converter. Along with SM72295 (Photovoltaic Full Bridge Driver) it creates a solution for an MPPT configured DC-DC converter with efficiencies up to 98.5%. Integrated into the chip is an 8-channel, 12 bit A/D converter used to sense input and output voltage and current, as well as board configuration. Externally programmable values include maximum output voltage and current as well as different settings on slew rate, and soft-start.

Block Diagram

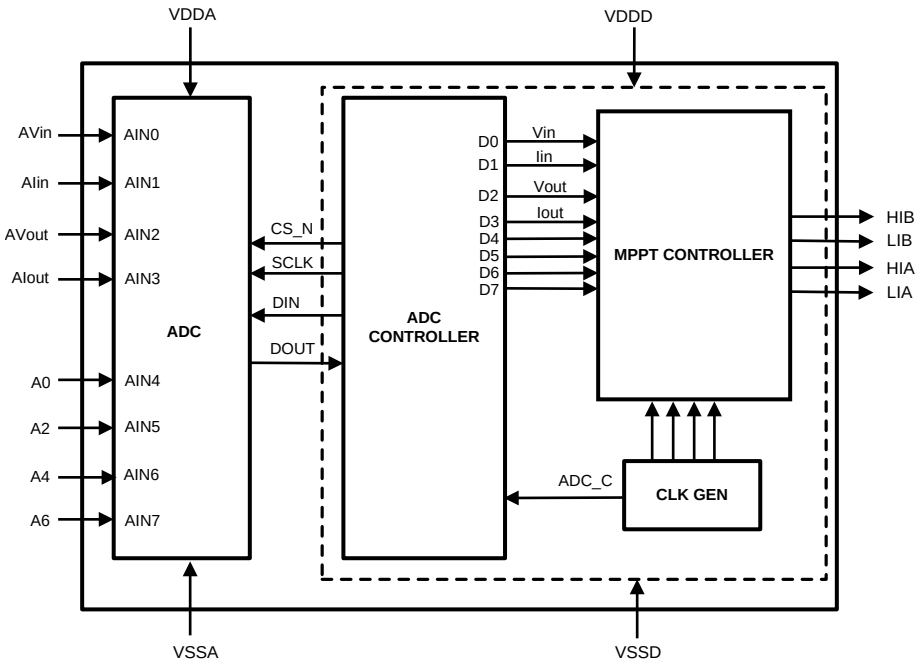


Figure 1. Block Diagram

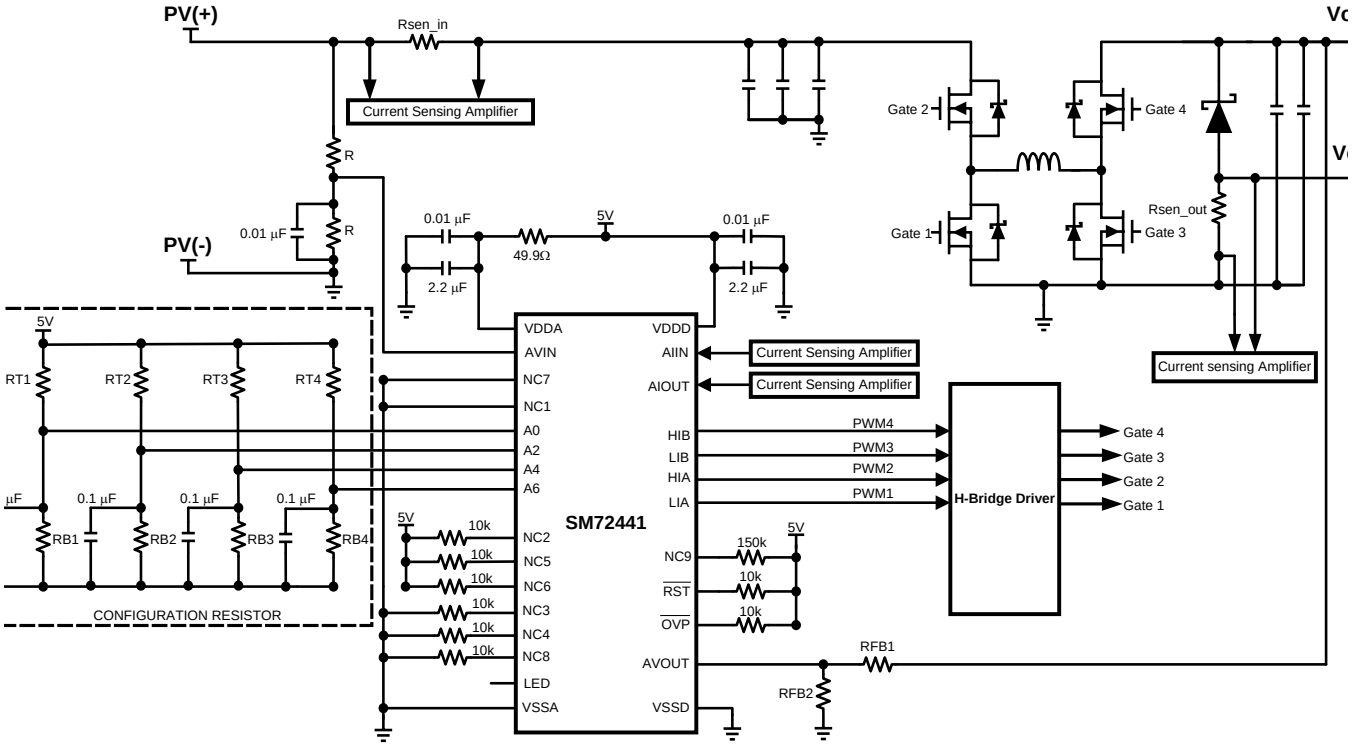


Figure 2. Typical Application Circuit

Connection Diagram

Top View

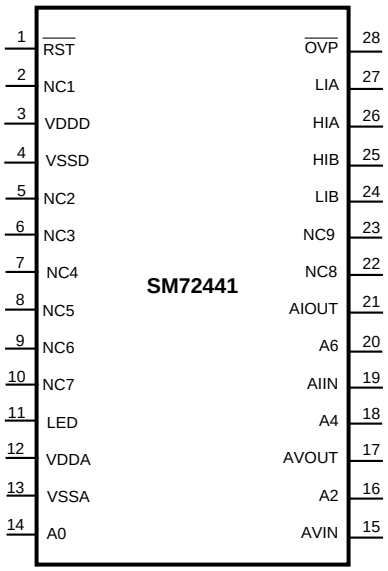


Figure 3. TSSOP-28 Package
See Package Drawing PW0028A

Pin Descriptions

Pin	Name	Description
1	$\overline{\text{RST}}$	Active low signal. External reset input signal to the digital circuit.
2	NC1	No Connect. This pin should be grounded.
3	VDDD	Digital supply voltage. This pin should be connected to a 5V supply, and bypassed to VSSD with a 0.1uF monolithic ceramic capacitor.
4	VSSD	Digital ground. The ground return for the digital supply and signals.
5	NC2	No Connect. This pin should be pulled up to the 5V supply using 10k resistor.
6	NC3	No Connect. This pin should be grounded using a 10k resistor.
7	NC4	No Connect. This pin should be grounded using a 10k resistor.
8	NC5	No Connect. This pin should be pulled up to 5V supply using 10k resistor.
9	NC6	No Connect. This pin should be pulled up to 5V supply using 10k resistor.
10	NC7	No Connect. This pin should be grounded.
11	LED	LED pin outputs a pulse during normal operation.
12	VDDA	Analog supply voltage. This voltage is also used as the reference voltage. This pin should be connected to a 5V supply, and bypassed to VSSA with a 1uF and 0.1uF monolithic ceramic capacitor.
13	VSSA	Analog ground. The ground return for the analog supply and signals.
14	A0	A/D Input Channel 0. Connect a resistor divider to 5V supply to set the maximum output voltage. Please refer to application section for more information on setting the resistor value.
15	AVIN	A/D Input to sense input voltage.
16	A2	A/D Input Channel 2. Connect a resistor divider to 5V supply to set MPPT update rate. Please refer to application section for more information on setting the resistor value.
17	AVOUT	A/D Input to sense the output voltage.
18	A4	A/D Input Channel 4. Connect a resistor divider to 5V supply to set the maximum output current. Please refer to application section for more information on setting the resistor value.
19	AIIN	A/D Input to sense input current.
20	A6	A/D Input Channel 6. Connect a resistor divider to 5V supply to set the maximum output voltage slew rate. Please refer to application section for more information on setting the resistor value.
21	AIOUT	A/D Input to sense the output current.

Pin Descriptions (continued)

Pin	Name	Description
22	NC8	No Connect. This pin should be grounded using a 10k resistor.
23	NC9	No Connect. This pin should be connected with 150k pull-up resistor to 5V supply.
24	LIB	Low side boost PWM output.
25	HIB	High side boost PWM output.
26	HIA	High side buck PWM output.
27	LIA	Low side buck PWM output.
28	$\overline{OVP}$	Overvoltage Protection Pin. Active Low. SM72441 will reset once voltage on this pin drops below its threshold voltage.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Analog Supply Voltage V_A (VDDA -VSSA)		-0.3 to 6.0V
Analog Supply Voltage V_D (VDDD -VSSD)		-0.3 to V_A +0.3V, max 6.0V
Voltage on Any Pin to GND		-0.3 to V_A +0.3V
Input Current at Any Pin (Note 3)		±10 mA
Package Input Current (Note 3)		±20 mA
Storage Temperature Range		-65°C to +150°C
ESD Rating(3)	Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Recommended Operating Conditions

Operating Temperature	-40°C to 105°C
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+4.75V to V_A
Digital Input Voltage	0 to V_A
Analog Input Voltage	0 to V_A
Junction Temperature	-40°C to 125°C

Electrical Characteristics

Specifications in standard typeface are for T_J = 25°C, and those in boldface type apply over the full operating junction temperature range.(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INPUT CHARACTERISTICS						
AVin, Alin AVout, Alout	Input Range		-	0 to V_A	-	V
I_{DCL}	DC Leakage Current		-	-	**±1**	µA
C_{INA}	Input Capacitance(2)	Track Mode	-	33	-	pF
		Hold Mode	-	3	-	pF
V_{ERR}	DC Voltage Measurement Accuracy			0.1		%
DIGITAL INPUT CHARACTERISTICS						
V_{IL}	Input Low Voltage		-	-	**0.8**	V
V_{IH}	Input High Voltage		**2.8**	-	-	V
C_{IND}	Digital Input Capacitance(2)		-	2	**4**	pF
I_{IN}	Input Current		-	±0.01	**±1**	µA
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA $V_A = V_D$ = 5V	**V_D-0.5**	-	-	V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA to 1.0 mA $V_A = V_D$ = 5V	-	-	**0.4**	V
I_{OZH} , I_{OZL}	Hi-Impedance Output Leakage Current	$V_A = V_D$ = 5V			**±1**	µA
C_{OUT}	Hi-Impedance Output Capacitance(2)			2	**4**	pF
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)						
V_A ,V_D	Analog and Digital Supply Voltages	$V_A \geq V_D$	**4.75**	5	**5.25**	V
$I_A + I_D$	Total Supply Current	$V_A = V_D$ = 4.75V to 5.25V	7	10	**15**	mA
P_C	Power Consumption	$V_A = V_D$ = 4.75V to 5.25V		50	**78**	mW
PWM OUTPUT CHARACTERISTICS						
f_{PWM}	PWM switching frequency			210		kHz
t_{DEAD}	Dead time			38		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instrument's Average Outgoing Quality Level (AOQL).

(2) Not tested. Specified by design.

OPERATION DESCRIPTION

OVERVIEW

The SM72441 is a programmable MPPT controller capable of outputting four PWM gate drive signals for a 4-switch buck-boost converter. Refer to the Typical Application Circuit diagram (Figure 2).

The SM72441 uses an advanced digital controller to generate its PWM signals. A maximum power point tracking (MPPT) algorithm monitors the input current and voltage and controls the PWM duty cycle to maximize energy harvested from the photovoltaic module. MPPT performance is very fast. Convergence to the maximum power point of the module typically occurs within 0.01s. This enables the controller to maintain optimum performance under fast-changing irradiance conditions.

Transitions between buck, boost, and buck-boost modes are smoothed, and advanced digital PWM dithering techniques are employed to increase effective PWM resolution. Output voltage and current limiting functionality are integrated into the digital control logic. The controller is capable of handling both shorted and no-load conditions and will recover smoothly from both.

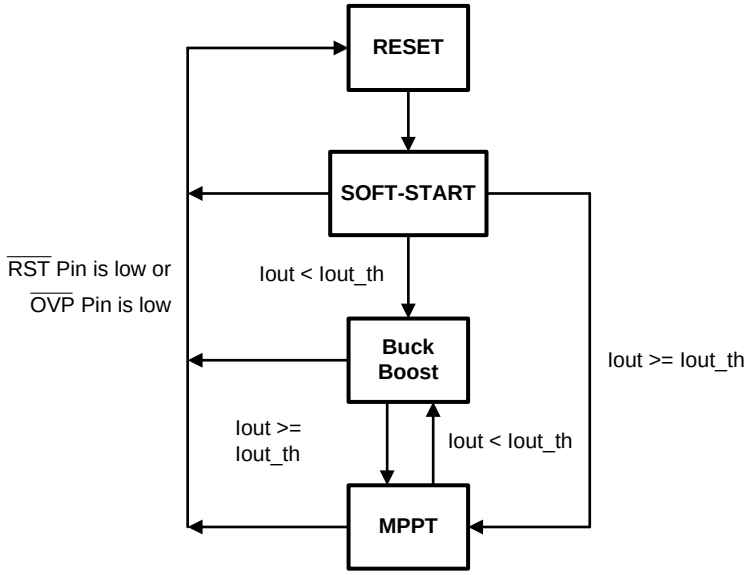


Figure 4. High Level State Diagram for Startup

STARTUP

SM72441 has a soft start feature that will ramp its output voltage for a fixed time of 250ms. MPPT mode will be entered during soft start if the load current exceeded the minimum current threshold. Otherwise, buck-boost operation is entered after soft-start is finished where the ratio between input and output voltage is 1:1. Refer to Figure 4 for a high level state diagram of startup. The current threshold to transition between MPPT to standby (buck-boost) mode and vice versa can be set by feeding the output of current sensing amplifier (Figure 2) to the AIIN and AIOUT pin. For an appropriate voltage level, refer to the AIIN AND AIOUT PIN section of this datasheet.

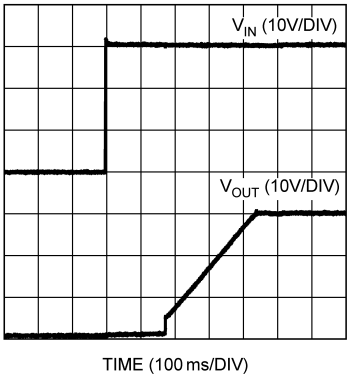


Figure 5. Start-Up Waveforms of Controlled Output

MAXIMUM OUTPUT VOLTAGE

Maximum output voltage on the SM72441 is set by resistor divider ratio on pin A0. (Please refer to Figure 2 Typical Application Circuit).

$$V_{OUT\_MAX} = 5 \times \frac{RB1}{RT1 + RB1} \times \frac{(RFB1 + RFB2)}{RFB2} \quad (1)$$

Where RT1 and RB1 are the resistor divider on the ADC pin A0 and RFB1 and RFB2 are the output voltage feedback resistors. A typical value for RFB2 is about 2 kΩ.

CURRENT LIMIT SETTING

Maximum output current can be set by changing the resistor divider on A4 (pin 18). (Refer to Figure 2). Overcurrent at the output is detected when the voltage on AIOUT (pin 21) equals to the voltage on A4 (pin 18). The voltage on A4 can be set by a resistor divider connected to 5V whereas a current sense amplifier output can be used to set the voltage on AIOUT.

AIIN AND AIOUT PIN

These two pins are used to set current threshold from standby (buck-boost mode) to MPPT mode and from MPPT mode into standby mode.

In order to transition from standby to MPPT mode, the following conditions have to be satisfied:

1) AIIN and AIOUT voltage > 0.488V

2) Iout < Iout_max

On the other hand, in order to transition from MPPT to standby mode, the following condition have to be satisfied:

1) AIIN and AIOUT voltage < 0.293V

2) Iout < Iout_max

Current limit is triggered when AIOUT (pin 21) voltage is equal to A4 (pin 18).

AVIN PIN

AVIN pin is an A/D input to sense the input voltage of SM72441. A resistor divider can be used to scale the max voltage to about 4V, which is 80% of the full scale of the A/D input.

CONFIGURABLE SETTINGS

The voltage on A0 sets the max output voltage; whereas the voltage on A2 enables MPPT update rate and limits the max boost ratio when output current is below the standby threshold. Output current limit is set by the voltage on A4 and output voltage slew rate limit is set on A6. In order to set a slew rate limit of 125V/sec, the ratio of the two resistors in A6 should be 9:1.

The low current condition is detected if the voltage on AIIN is less than 0.488V (rising) and 0.293 (falling) + ΔI or if the voltage on AIOUT is less than 0.488 V (rising) and 0.293 (falling) + ΔI. If low current is detected, the converter operates in standby mode and limit the maximum duty cycle to either a 1 (buck-boost), 1.15 (boost) or 1.25 (boost) conversion ratio (programmable). In this case no MPPT will be performed.

The actual value of current will depend on the gain of the current sensing amplifier circuitry that feeds the AIIN and AIOUT pins.

For more complete information on the various settings based on the voltage level of A2, please refer to Table 1 below. Vfs denotes the full scale voltage of the ADC which is equal to VDDA where VDDA is a reference voltage to analog ground.

A typical value for top configuration resistors (RT1 to RT4) should be 20 kΩ.

Table 1. List of Configurable Modes on ADC Channel 2

ADC Channel 2	MPPT Update Time	Slew Rate Detection	Low Current Detection	Initial Boost Ratio	Delta I
0 < VADC2 < Vfs/16	1.2 ms	Disabled	Disabled	N/A	N/A
1Vfs/16 < VADC2 <2Vfs/16	38 ms	Disabled	Disabled	N/A	N/A
2Vfs/16 < VADC2 <3Vfs/16	77 ms	Disabled	Disabled	N/A	N/A
3Vfs/16 < VADC2 <4Vfs/16	38 ms	Enabled	Disabled	N/A	N/A
4Vfs/16 < VADC2 <5Vfs/16	38 ms	Enabled	Enabled	1.15	60 (0.3 A)
5Vfs/16 < VADC2 <6Vfs/16	38 ms	Enabled	Enabled	1.15	90 (0.45 A)
6Vfs/16 < VADC2 <7Vfs/16	38 ms	Enabled	Enabled	1.15	120(0.6 A)
7Vfs/16 < VADC2 <8Vfs/16	38 ms	Enabled	Enabled	1.25	60
8Vfs/16 < VADC2 <9Vfs/16	38 ms	Enabled	Enabled	1.25	90
9Vfs/16 < VADC2 <10Vfs/16	38 ms	Enabled	Enabled	1.25	120
10Vfs/16 < VADC2 <11Vfs/16	77 ms	Enabled	Enabled	1.15	60
11Vfs/16 < VADC2 <12Vfs/16	77 ms	Enabled	Enabled	1.15	90
12Vfs/16 < VADC2 <13Vfs/16	77 ms	Enabled	Enabled	1.15	120
13Vfs/16 < VADC2 <14Vfs/16	77 ms	Enabled	Enabled	1.25	60
14Vfs/16 < VADC2 <15Vfs/16	77 ms	Enabled	Enabled	1.25	90
15Vfs/16 < VADC2 <16Vfs/16	77 ms	Enabled	Enabled	1.25	120

RESET PIN

When the reset pin is pulled low, the chip will cease its normal operation and turn-off all of its PWM outputs. Below is an oscilloscope capture of a forced reset condition.

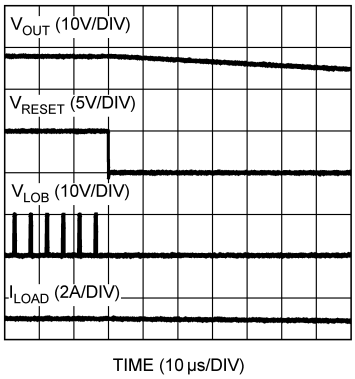


Figure 6. Reset Operational Behavior

As seen in Figure 6, the initial value for output voltage and load current are 28V and 1A respectively. After the reset pin is grounded, both the output voltage and load current decreases immediately. MOSFET switching on the buck-boost converter also stops immediately. V_{LOB} indicates the low side boost output from the SM72295.

ANALOG INPUT

An equivalent circuit for one of the ADC input channels is shown in Figure 7. Diode D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0V to V_A. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 7 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch; it is typically 500Ω. Capacitor C2 is the ADC sampling capacitor; it is typically 30 pF. The ADC will deliver best performance when driven by a low-impedance source (less than 100Ω). This is especially important when sampling dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonic and noise in the input. These filters are often referred to as anti-aliasing filters.

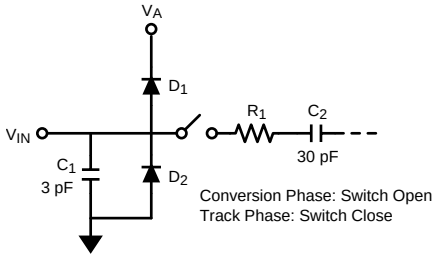


Figure 7. Equivalent Input Circuit

DIGITAL INPUTS AND OUTPUTS

The digital input signals have an operating range of 0V to V_A, where V_A = VDDA - VSSA. They are not prone to latch-up and may be asserted before the digital supply V_D, where V_D = VDDD - VSSD, without any risk. The digital output signals operating range is controlled by V_D. The output high voltage is V_D – 0.5V (min) while the output low voltage is 0.4V (max).

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SM72441MT/NOPB	Active	Production	TSSOP (PW) | 28	48 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441
SM72441MT/NOPB.A	Active	Production	TSSOP (PW) | 28	48 | TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441
SM72441MTE/NOPB	Active	Production	TSSOP (PW) | 28	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441
SM72441MTE/NOPB.A	Active	Production	TSSOP (PW) | 28	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441
SM72441MTX/NOPB	Active	Production	TSSOP (PW) | 28	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441
SM72441MTX/NOPB.A	Active	Production	TSSOP (PW) | 28	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	S72441

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

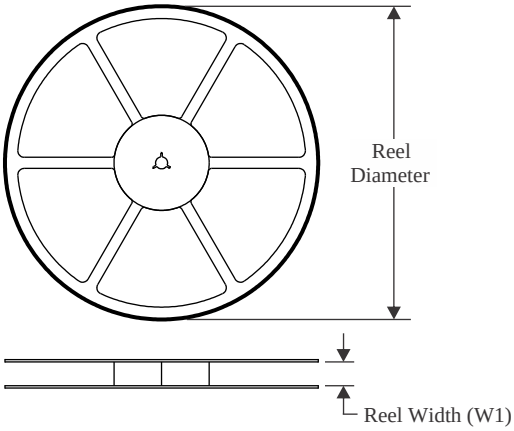
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

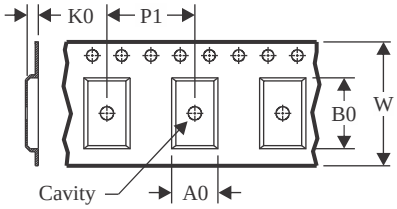
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

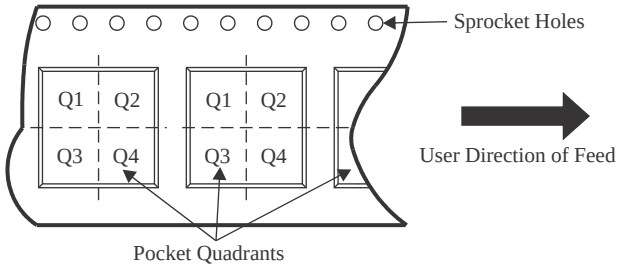


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

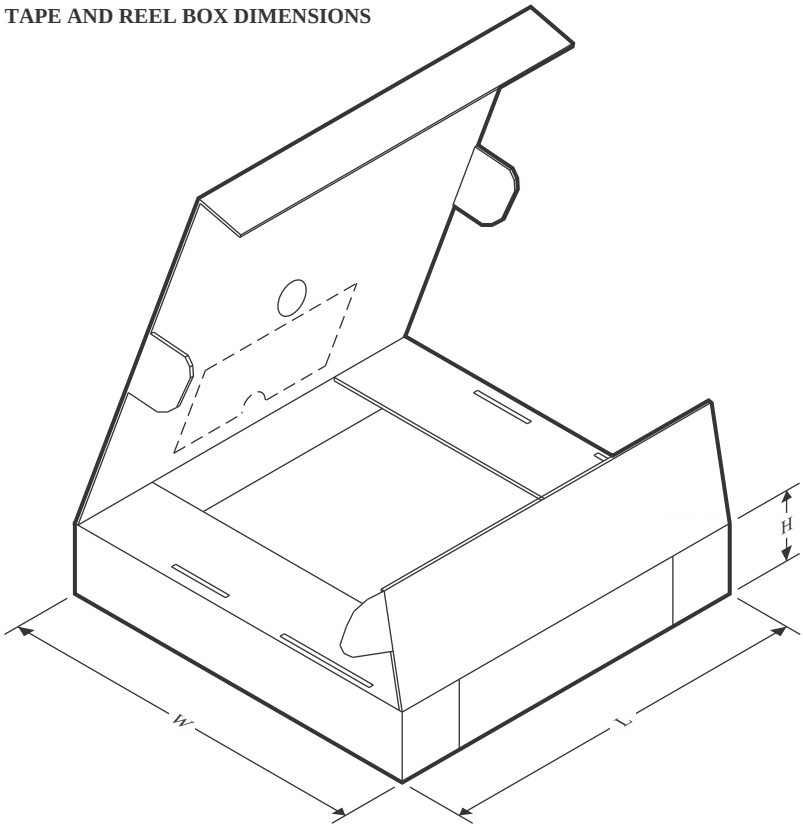
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM72441MTE/NOPB	TSSOP	PW	28	250	178.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1
SM72441MTX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1

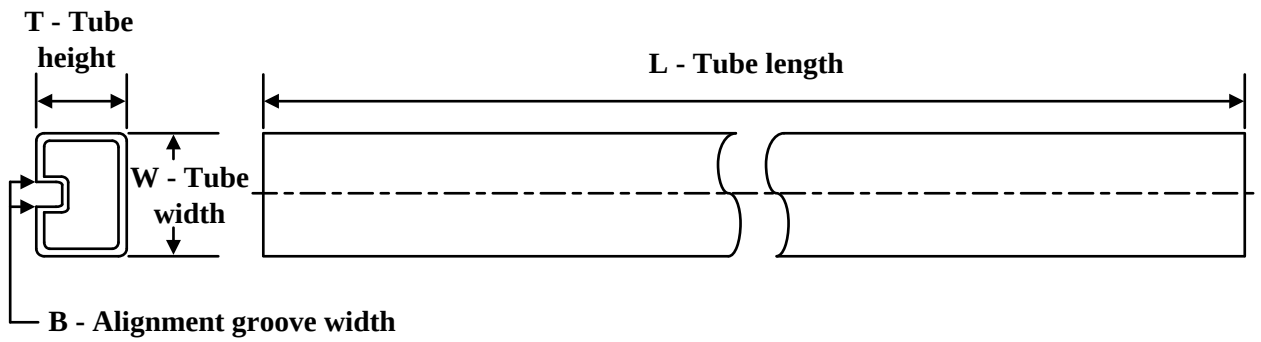
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM72441MTE/NOPB	TSSOP	PW	28	250	208.0	191.0	35.0
SM72441MTX/NOPB	TSSOP	PW	28	2500	356.0	356.0	36.0

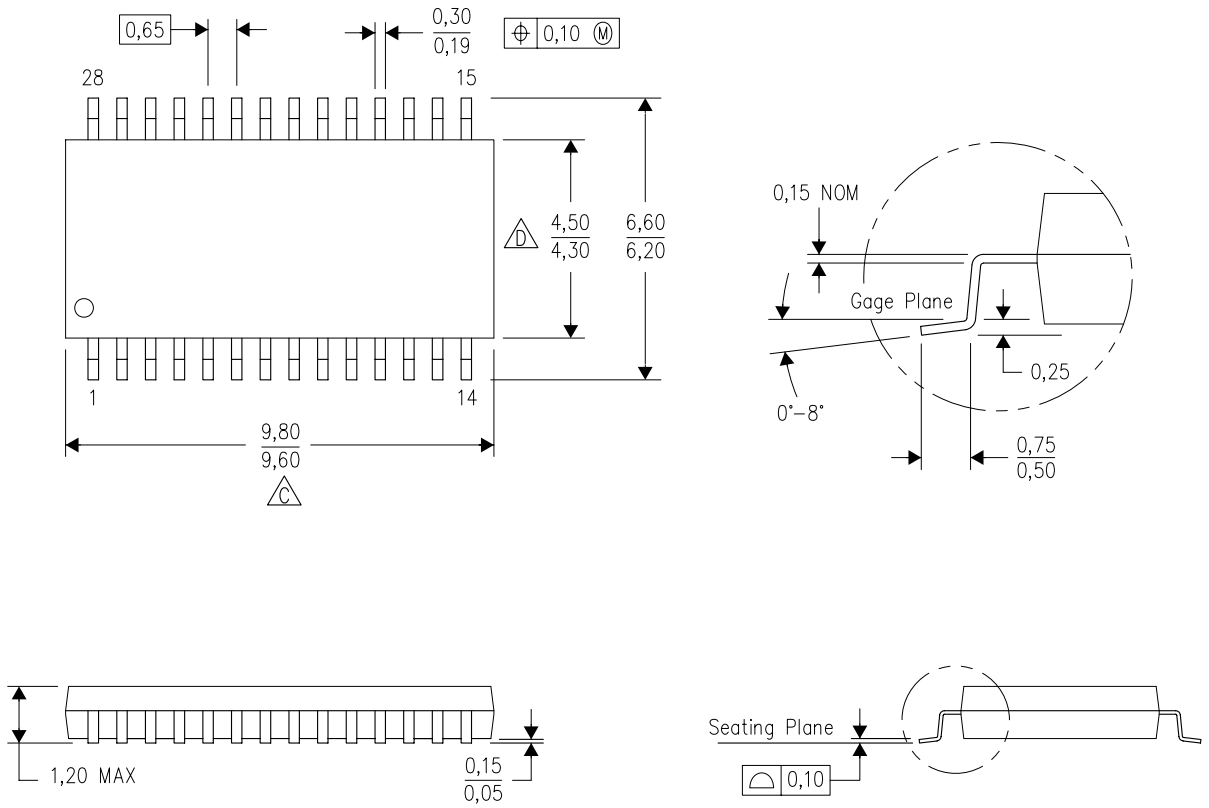
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SM72441MT/NOPB	PW	TSSOP	28	48	495	8	2514.6	4.06
SM72441MT/NOPB.A	PW	TSSOP	28	48	495	8	2514.6	4.06

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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