

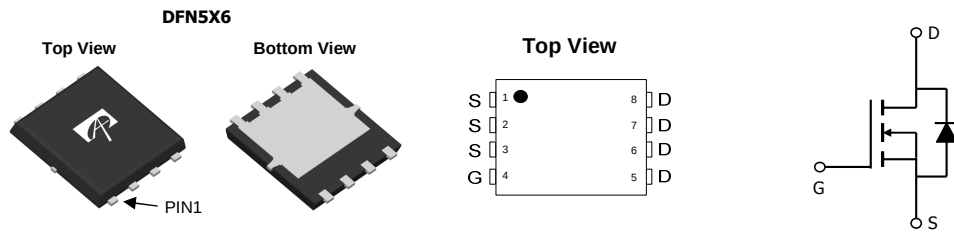
General Description

The AON6482 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	28A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 37m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 42m Ω

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	28	A
		18	
Pulsed Drain Current ^C	I_{DM}	70	
Continuous Drain Current	I_{DSM}	5.5	A
		4.4	
Avalanche Current ^C	I_{AS}, I_{AR}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	61	mJ
Power Dissipation ^B	P_D	63	W
		25	
Power Dissipation ^A	P_{DSM}	2.5	W
		1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14.2	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		42	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	2	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.6	2.1	2.7	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	70			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =10A T _J =125°C		29 59	37 71	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		45		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ⁶				60	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz	1300	1630	2000	pF
C _{oss}	Output Capacitance		70	100	130	pF
C _{rss}	Reverse Transfer Capacitance		30	50	70	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.75	1.1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =10A	26	34	44	nC
Q _{g(4.5V)}	Total Gate Charge		14	18	22	nC
Q _{gs}	Gate Source Charge		4	6	8	nC
Q _{gd}	Gate Drain Charge		5	9	13	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =5Ω, R _{GEN} =3Ω		7		ns
t _r	Turn-On Rise Time			7		ns
t _{D(off)}	Turn-Off DelayTime			29		ns
t _f	Turn-Off Fall Time			7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, dI/dt=500A/μs	22	32	42	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, dI/dt=500A/μs	140	200	260	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

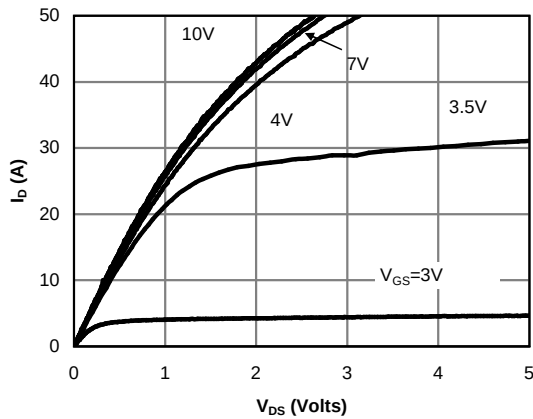


Fig 1: On-Region Characteristics (Note E)

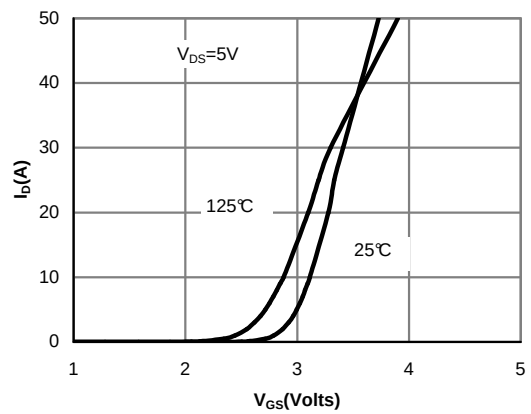


Figure 2: Transfer Characteristics (Note E)

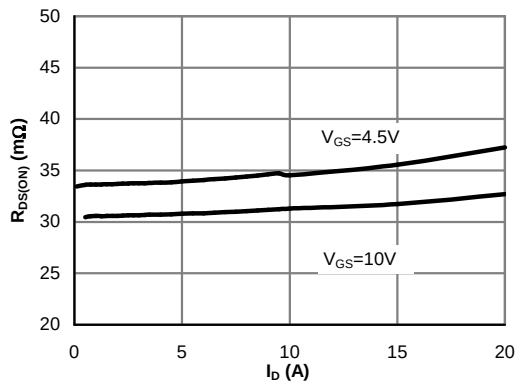


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

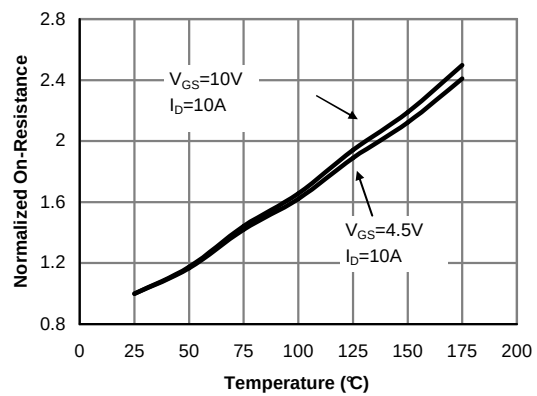


Figure 4: On-Resistance vs. Junction Temperature (Note E)

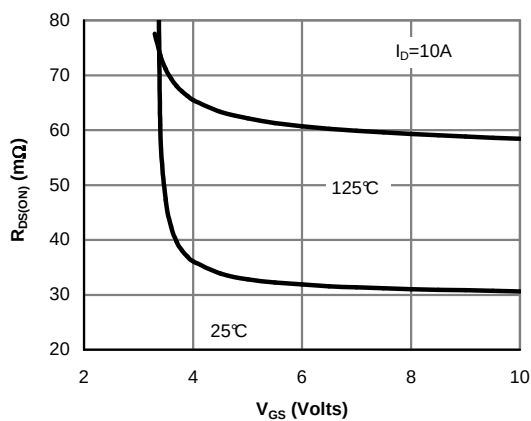


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

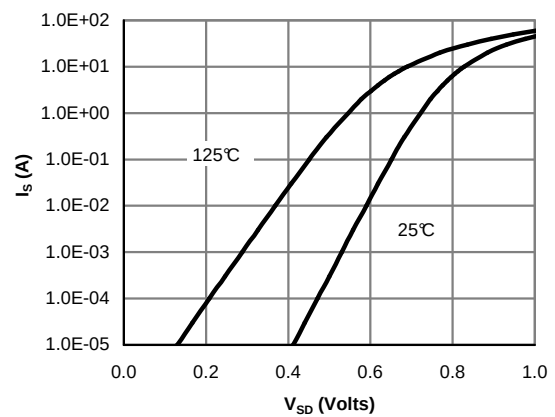


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

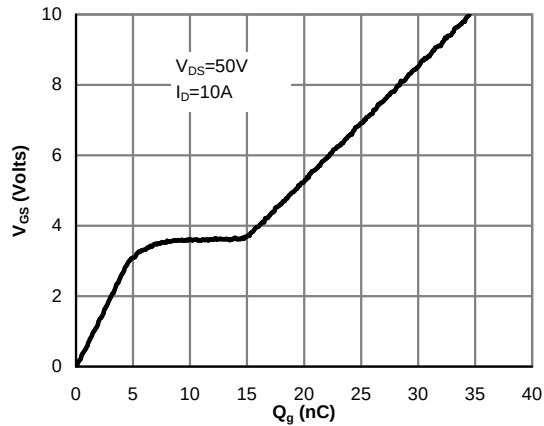


Figure 7: Gate-Charge Characteristics

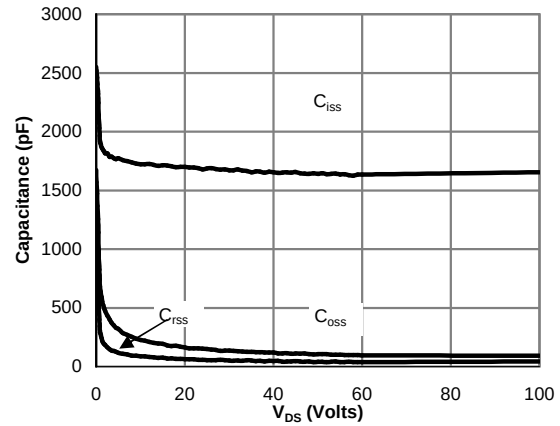


Figure 8: Capacitance Characteristics

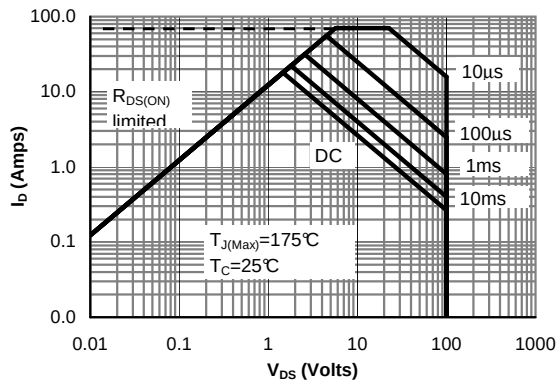


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

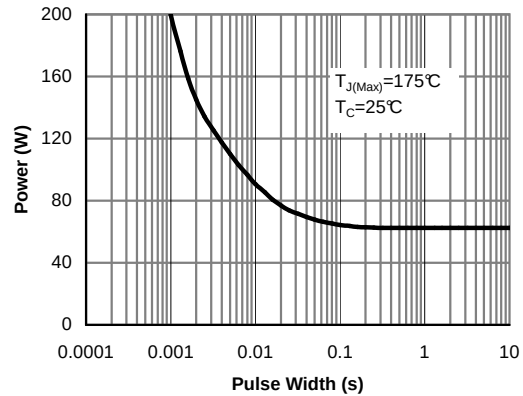


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

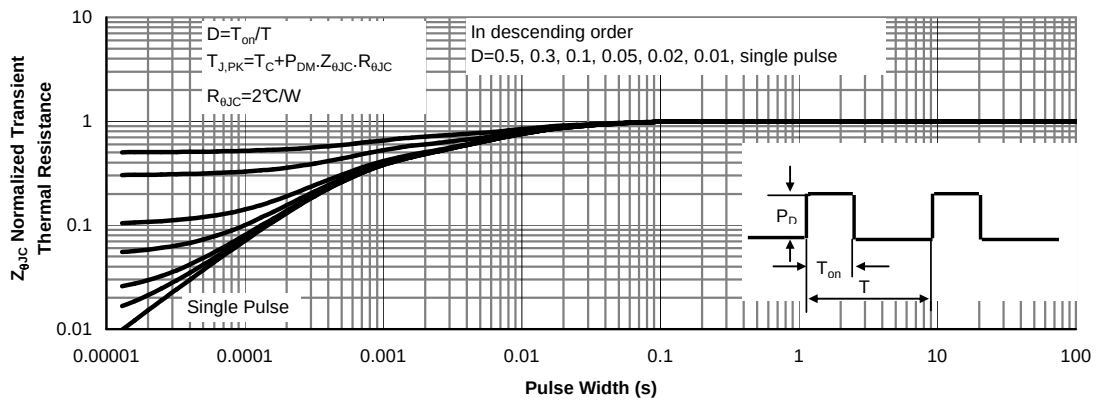


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

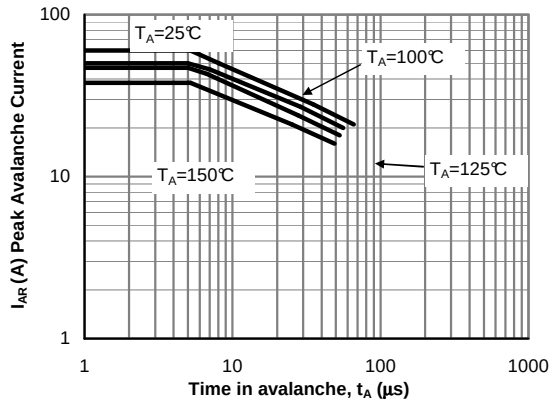


Figure 12: Single Pulse Avalanche capability (Note C)

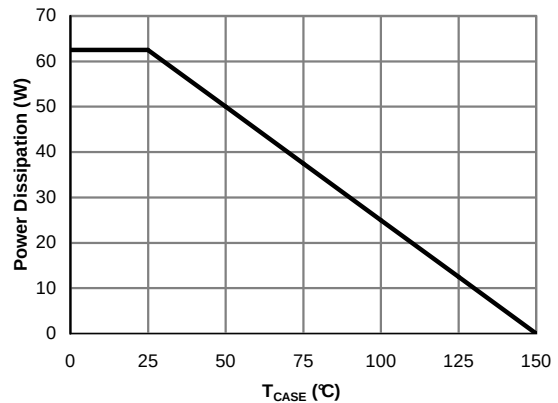


Figure 13: Power De-rating (Note F)

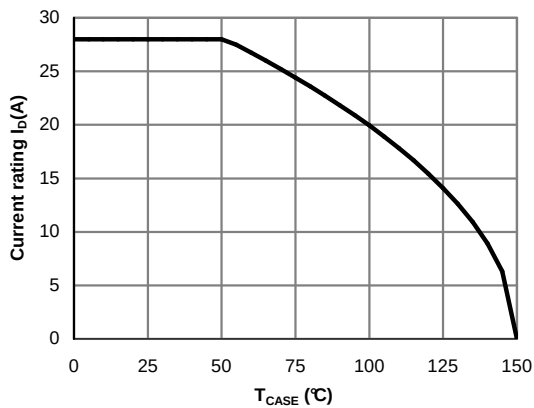


Figure 14: Current De-rating (Note F)

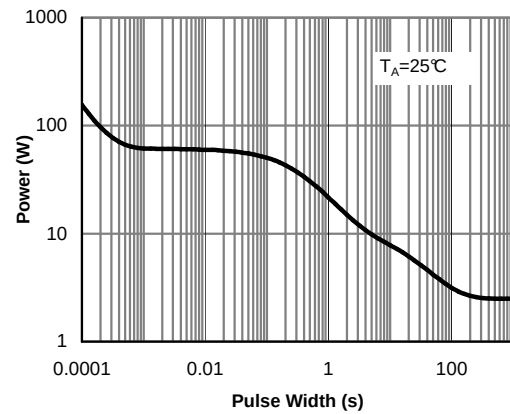


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

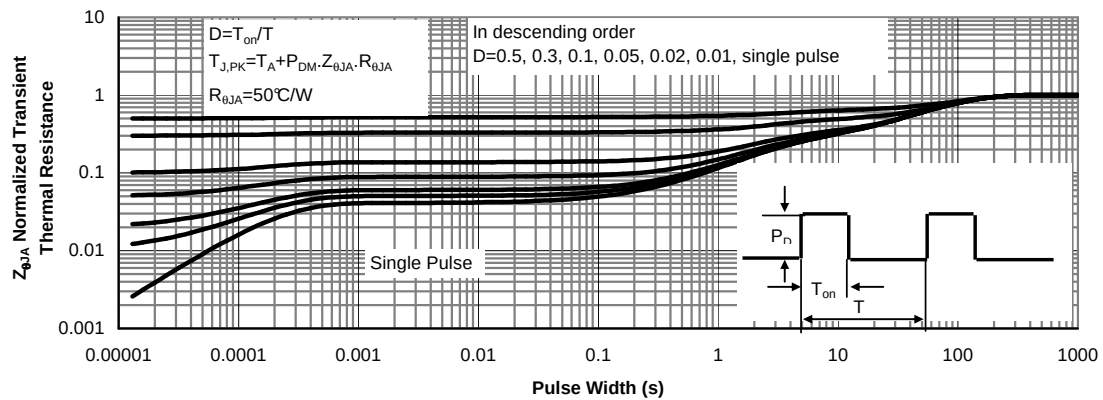
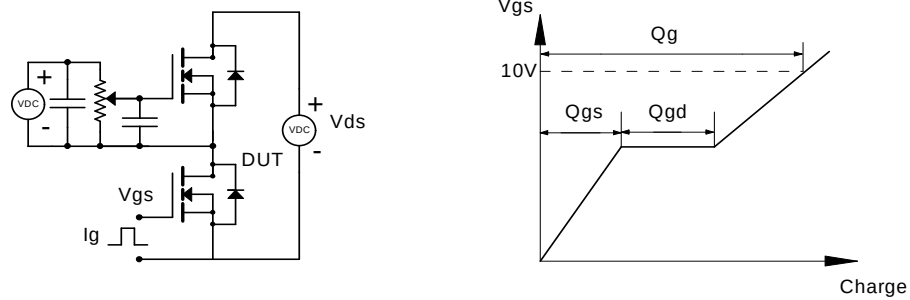
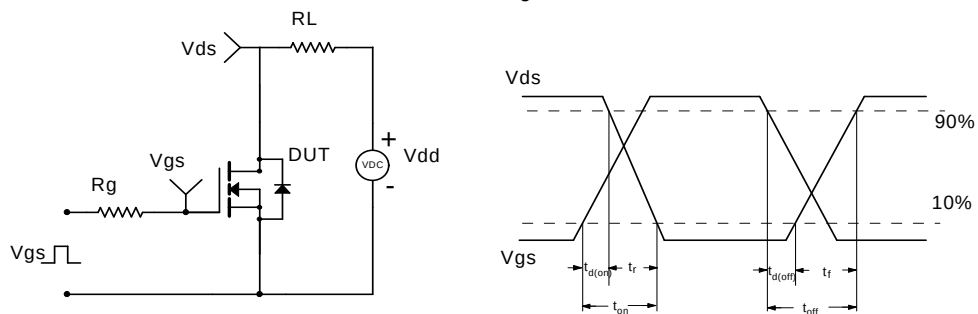


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

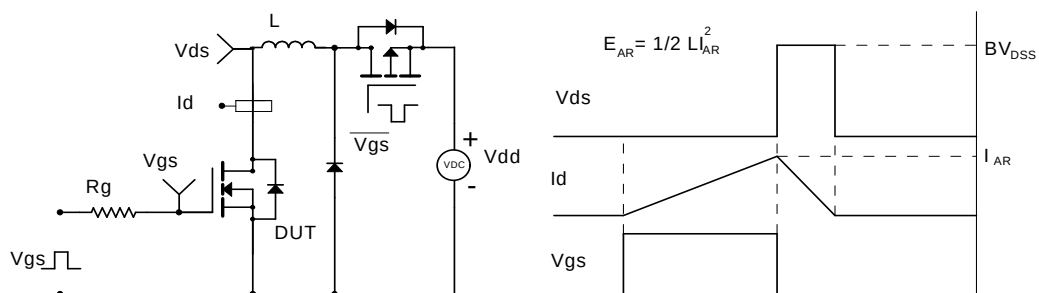
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

