



## LM7121 235-MHz Tiny Low Power Voltage Feedback Amplifier

### 1 Features

- (Typical Unless Otherwise Noted).  $V_S = \pm 15\text{ V}$
- Easy to use Voltage Feedback Topology
- Stable with Unlimited Capacitive Loads
- Tiny SOT23-5 Package — Typical Circuit Layout Takes Half the Space Of SO-8 Designs
- Unity Gain Frequency: 175 MHz
- Bandwidth ( $-3\text{ dB}$ ,  $A_V = +1$ ,  $R_L = 100\Omega$ ): 235 MHz
- Slew Rate: 1300V/ $\mu\text{s}$
- Supply Voltages:
  - SO-8: 5 V to  $\pm 15\text{ V}$
  - SOT23-5: 5 V to  $\pm 5\text{ V}$
- Characterized for: +5 V,  $\pm 5\text{ V}$ ,  $\pm 15\text{ V}$
- Low Supply Current: 5.3 mA

### 2 Applications

- Scanners, Color Fax, Digital Copiers
- PC Video Cards
- Cable Drivers
- Digital Cameras
- ADC/DAC Buffers
- Set-top Boxes

### 3 Description

The LM7121 is a high performance operational amplifier which addresses the increasing AC performance needs of video and imaging applications, and the size and power constraints of portable applications.

The LM7121 can operate over a wide dynamic range of supply voltages, from 5 V (single supply) up to  $\pm 15\text{ V}$  (see [Application and Implementation](#) for more details). It offers an excellent speed-power product delivering 1300 V/ $\mu\text{s}$  and 235 MHz Bandwidth ( $-3\text{ dB}$ ,  $A_V = +1$ ). Another key feature of this operational amplifier is stability while driving unlimited capacitive loads.

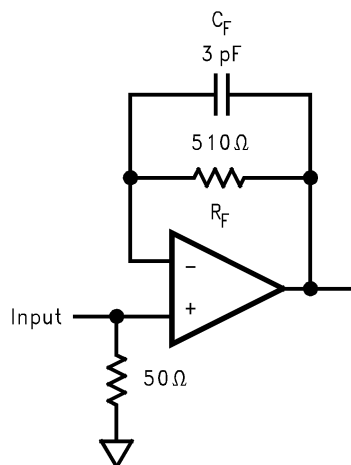
Due to its tiny SOT23-5 package, the LM7121 is ideal for designs where space and weight are the critical parameters. The benefits of the tiny package are evident in small portable electronic devices, such as cameras, and PC video cards. Tiny amplifiers are so small that they can be placed anywhere on a board close to the signal source or near the input to an A/D converter.

#### Device Information<sup>(1)</sup>

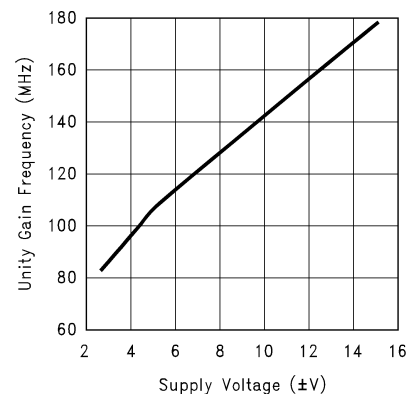
| PART NUMBER | PACKAGE    | BODY SIZE (NOM)            |
|-------------|------------|----------------------------|
| LM7121      | SOT-23 (5) | 2.921 mm $\times$ 1.651 mm |
|             | SOIC (8)   | 4.902 mm $\times$ 3.912 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Circuit for  $A_V = +1$  Operation  
( $V_S = 6\text{ V}$ )



Unity Gain Frequency vs. Supply Voltage



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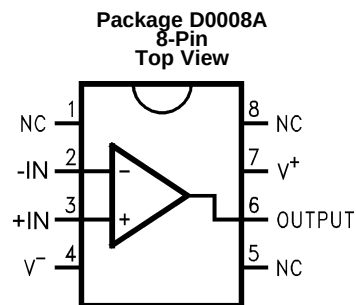
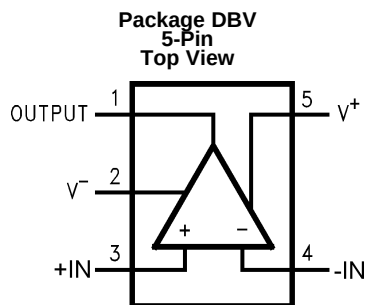
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (August 1999) to Revision A                                                                                                                                                                                                                                                                                                                        | Page     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <ul style="list-style-type: none"> <li>Added, updated, or renamed the following sections: Device Information Table, <i>Pin Configuration and Functions</i>, <i>Application and Implementation</i>; <i>Power Supply Recommendations</i> ; <i>Layout</i>; <i>Device and Documentation Support</i>; <i>Mechanical, Packaging, and Ordering Information</i> .....</li> </ul> | <b>1</b> |
| <ul style="list-style-type: none"> <li>Deleted <math>T_J = 25^{\circ}\text{C}</math> from Electrical Characteristics tables .....</li> </ul>                                                                                                                                                                                                                             | <b>5</b> |

## 5 Pin Configuration and Functions



**Pin Functions**

| PIN            |        |        | I/O | DESCRIPTION         |
|----------------|--------|--------|-----|---------------------|
| NAME           | NUMBER |        |     |                     |
|                | DBV    | D0008A |     |                     |
| -IN            | 4      | 2      | I   | Inverting input     |
| +IN            | 3      | 3      | I   | Non-inverting input |
| N/C            | —      | 5, 8   | —   | No connection       |
| OUTPUT         | 1      | 6      | O   | Output              |
| V <sup>-</sup> | 2      | 4      | I   | Negative supply     |
| V <sup>+</sup> | 5      | 7      | I   | Positive supply     |

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                               | MIN | MAX                   | UNIT |
|-----------------------------------------------|-----|-----------------------|------|
| Differential Input Voltage <sup>(2)</sup>     |     | ±2                    | V    |
| Voltage at Input/Output Pins                  |     | (V+)-1.4,<br>(V-)+1.4 | V    |
| Supply Voltage (V+-V-)                        |     | 36                    | V    |
| Output Short Circuit to Ground <sup>(3)</sup> |     | Continuous            |      |
| Lead Temperature (soldering, 10 sec)          |     | 260                   | °C   |
| Junction Temperature <sup>(4)</sup>           |     | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (3) The maximum power dissipation is a function of  $T_{J(max)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly into a PC board.
- (4) Typical Values represent the most likely parametric norm.

### 6.2 Handling Ratings

|                                                                                                                 | MIN | MAX  | UNIT |
|-----------------------------------------------------------------------------------------------------------------|-----|------|------|
| $T_{stg}$ Storage temperature range                                                                             | -65 | +150 | °C   |
| $V_{(ESD)}$ Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup> |     | 2000 | V    |

- (1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process. Human body model, 1.5 k in series with 100 pF.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                             | MIN | NOM | MAX | UNIT |
|-----------------------------|-----|-----|-----|------|
| Operating Temperature Range | -40 |     | 85  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                          | D0008A (8) | DBV (5) | UNIT |
|--------------------------------------------------------|------------|---------|------|
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 165        | 325     | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 ±15V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = +15\text{V}$ ,  $V^- = -15\text{V}$ ,  $V_{\text{CM}} = V_{\text{O}} = 0\text{V}$  and  $R_{\text{L}} > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER       |                                       | TEST CONDITIONS                                                              | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT                 |
|-----------------|---------------------------------------|------------------------------------------------------------------------------|--------------------|--------------------------------|----------------------|
| $V_{\text{OS}}$ | Input Offset Voltage                  |                                                                              | 0.9                | 8<br><b>15</b>                 | mV<br>max            |
| $I_{\text{B}}$  | Input Bias Current                    |                                                                              | 5.2                | 9.5<br><b>12</b>               | $\mu\text{A}$<br>max |
| $I_{\text{OS}}$ | Input Offset Current                  |                                                                              | 0.04               | 4.3<br><b>7</b>                | $\mu\text{A}$<br>max |
| $R_{\text{IN}}$ | Input Resistance                      | Common Mode                                                                  | 10                 |                                | $\text{M}\Omega$     |
|                 |                                       | Differential Mode                                                            | 3.4                |                                | $\text{M}\Omega$     |
| $C_{\text{IN}}$ | Input Capacitance                     | Common Mode                                                                  | 2.3                |                                | pF                   |
| CMRR            | Common Mode Rejection Ratio           | $-10\text{V} \leq V_{\text{CM}} \leq 10\text{V}$                             | 93                 | 73<br><b>70</b>                | dB<br>min            |
| +PSRR           | Positive Power Supply Rejection Ratio | $10\text{V} \leq V^+ \leq 15\text{V}$                                        | 86                 | 70<br><b>68</b>                | dB<br>min            |
| -PSRR           | Negative Power Supply Rejection Ratio | $-15\text{V} \leq V^- \leq -10\text{V}$                                      | 81                 | 68<br><b>65</b>                | dB<br>min            |
| $V_{\text{CM}}$ | Input Common-Mode Voltage Range       | CMRR $\geq 70\text{ dB}$                                                     | 13                 | 11                             | V min                |
|                 |                                       |                                                                              | -13                | -11                            | V max                |
| $A_{\text{V}}$  | Large Signal Voltage Gain             | $R_{\text{L}} = 2\text{ k}\Omega$ , $V_{\text{O}} = 20\text{ V}_{\text{PP}}$ | 72                 | 65<br><b>57</b>                | dB<br>min            |
| $V_{\text{O}}$  | Output Swing                          | $R_{\text{L}} = 2\text{ k}\Omega$                                            | 13.4               | 11.1<br><b>10.8</b>            | V<br>min             |
|                 |                                       |                                                                              | -13.4              | -11.2<br><b>-11.0</b>          | V<br>max             |
|                 |                                       | $R_{\text{L}} = 150\ \Omega$                                                 | 10.2               | 7.75<br><b>7.0</b>             | V<br>min             |
|                 |                                       |                                                                              | -7.0               | -5.0<br><b>-4.8</b>            | V<br>max             |
| $I_{\text{SC}}$ | Output Short Circuit Current          | Sourcing                                                                     | 71                 | 54<br><b>44</b>                | mA<br>min            |
|                 |                                       | Sinking                                                                      | 52                 | 39<br><b>34</b>                | mA<br>min            |
| $I_{\text{S}}$  | Supply Current                        |                                                                              | 5.3                | 6.6<br><b>7.5</b>              | mA<br>max            |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

## 6.6 ±15V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = 15\text{V}$ ,  $V^- = -15\text{V}$ ,  $V_{\text{CM}} = V_{\text{O}} = 0\text{V}$  and  $R_{\text{L}} > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER                       |                                   | TEST CONDITIONS                                                                                    | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT                    |
|---------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------|--------------------|--------------------------------|-------------------------|
| SR                              | Slew Rate <sup>(3)</sup>          | $A_{\text{V}} = +2$ , $R_{\text{L}} = 1\text{ k}\Omega$ , $V_{\text{O}} = 20\text{ V}_{\text{PP}}$ | 1300               |                                | V/ $\mu\text{s}$        |
| GBW                             | Unity Gain-Bandwidth              | $R_{\text{L}} = 1\text{ k}\Omega$                                                                  | 175                |                                | MHz                     |
| $\phi_{\text{m}}$               | Phase Margin                      |                                                                                                    | 63                 |                                | Deg                     |
| f (–3 dB)                       | Bandwidth <sup>(4)(5)</sup>       | $R_{\text{L}} = 100\ \Omega$ , $A_{\text{V}} = +1$                                                 | 235                |                                | MHz                     |
|                                 |                                   | $R_{\text{L}} = 100\ \Omega$ , $A_{\text{V}} = +2$                                                 | 50                 |                                |                         |
| $t_{\text{s}}$                  | Settling Time                     | 10 $V_{\text{PP}}$ Step, to 0.1%, $R_{\text{L}} = 500\ \Omega$                                     | 74                 |                                | ns                      |
| $t_{\text{r}}$ , $t_{\text{f}}$ | Rise and Fall Time <sup>(5)</sup> | $A_{\text{V}} = +2$ , $R_{\text{L}} = 100\ \Omega$ , $V_{\text{O}} = 0.4\text{ V}_{\text{PP}}$     | 5.3                |                                | ns                      |
| $A_{\text{D}}$                  | Differential Gain                 | $A_{\text{V}} = +2$ , $R_{\text{L}} = 150\ \Omega$                                                 | 0.3%               |                                |                         |
| $\phi_{\text{D}}$               | Differential Phase                | $A_{\text{V}} = +2$ , $R_{\text{L}} = 150\ \Omega$                                                 | 0.65               |                                | Deg                     |
| $e_{\text{n}}$                  | Input-Referred Voltage Noise      | f = 10 kHz                                                                                         | 17                 |                                | nV / $\sqrt{\text{Hz}}$ |
| $i_{\text{n}}$                  | Input-Referred Current Noise      | f = 10 kHz                                                                                         | 1.9                |                                | pA / $\sqrt{\text{Hz}}$ |
| T.H.D.                          | Total Harmonic Distortion         | 2 $V_{\text{PP}}$ Output, $R_{\text{L}} = 150\ \Omega$ ,<br>$A_{\text{V}} = +2$ , f = 1 MHz        | 0.065%             |                                |                         |
|                                 |                                   | 2 $V_{\text{PP}}$ Output, $R_{\text{L}} = 150\ \Omega$ ,<br>$A_{\text{V}} = +2$ , f = 5 MHz        | 0.52%              |                                |                         |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Unity gain operation for  $\pm 5\text{V}$  and  $\pm 15\text{V}$  supplies is with a feedback network of 510  $\Omega$  and 3 pF in parallel (see [Application and Implementation](#)). For +5V single supply operation, feedback is a direct short from the output to the inverting input.

(5)  $A_{\text{V}} = +2$  operation with 2 k $\Omega$  resistors and 2 pF capacitor from summing node to ground.

## 6.7 ±5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = 5\text{V}$ ,  $V^- = -5\text{V}$ ,  $V_{\text{CM}} = V_{\text{O}} = 0\text{V}$  and  $R_{\text{L}} > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER       |                                       | TEST CONDITIONS                                | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT                 |
|-----------------|---------------------------------------|------------------------------------------------|--------------------|--------------------------------|----------------------|
| $V_{\text{OS}}$ | Input Offset Voltage                  |                                                | 1.6                | 8<br><b>15</b>                 | mV<br>max            |
| $I_{\text{B}}$  | Input Bias Current                    |                                                | 5.5                | 9.5<br><b>12</b>               | $\mu\text{A}$<br>max |
| $I_{\text{OS}}$ | Input Offset Current                  |                                                | 0.07               | 4.3<br><b>7.0</b>              | $\mu\text{A}$<br>max |
| $R_{\text{IN}}$ | Input Resistance                      | Common Mode                                    | 6.8                |                                | M $\Omega$           |
|                 |                                       | Differential Mode                              | 3.4                |                                | M $\Omega$           |
| $C_{\text{IN}}$ | Input Capacitance                     | Common Mode                                    | 2.3                |                                | pF                   |
| CMRR            | Common Mode Rejection Ratio           | $-2\text{V} \leq V_{\text{CM}} \leq 2\text{V}$ | 75                 | 65<br><b>60</b>                | dB<br>min            |
| +PSRR           | Positive Power Supply Rejection Ratio | $3\text{V} \leq V^+ \leq 5\text{V}$            | 89                 | 65<br><b>60</b>                | dB<br>min            |
| –PSRR           | Negative Power Supply Rejection Ratio | $-5\text{V} \leq V^- \leq -3\text{V}$          | 78                 | 65<br><b>60</b>                | dB<br>min            |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

## ±5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $V^+ = 5V$ ,  $V^- = -5V$ ,  $V_{CM} = V_O = 0V$  and  $R_L > 1M\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER |                                 | TEST CONDITIONS                    | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT      |
|-----------|---------------------------------|------------------------------------|--------------------|--------------------------------|-----------|
| $V_{CM}$  | Input Common Mode Voltage Range | CMRR $\geq 60$ dB                  | 3                  | 2.5                            | V<br>min  |
|           |                                 |                                    | -3                 | -2.5                           | V<br>max  |
| $A_V$     | Large Signal Voltage Gain       | $R_L = 2k\Omega$ , $V_O = 3V_{PP}$ | 66                 | 60<br><b>58</b>                | dB<br>min |
| $V_O$     | Output Swing                    | $R_L = 2k\Omega$                   | 3.62               | 3.0<br><b>2.75</b>             | V<br>min  |
|           |                                 |                                    | -3.62              | -3.0<br><b>-2.70</b>           | V<br>max  |
|           |                                 | $R_L = 150\Omega$                  | 3.1                | 2.5<br><b>2.3</b>              | V<br>min  |
|           |                                 |                                    | -2.8               | -2.15<br><b>-2.00</b>          | V<br>max  |
| $I_{SC}$  | Output Short Circuit Current    | Sourcing                           | 53                 | 38<br><b>33</b>                | mA<br>min |
|           |                                 | Sinking                            | 29                 | 21<br><b>19</b>                | mA<br>min |
| $I_S$     | Supply Current                  |                                    | 5.1                | 6.4<br><b>7.2</b>              | mA<br>max |

## 6.8 ±5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = 5V$ ,  $V^- = -5V$ ,  $V_{CM} = V_O = 0V$  and  $R_L > 1M\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER     |                                   | TEST CONDITIONS                                                    | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT             |
|---------------|-----------------------------------|--------------------------------------------------------------------|--------------------|--------------------------------|------------------|
| SR            | Slew Rate <sup>(3)</sup>          | $A_V = +2$ , $R_L = 1k\Omega$ , $V_O = 6V_{PP}$                    | 520                |                                | V/ $\mu$ s       |
| GBW           | Unity Gain-Bandwidth              | $R_L = 1k\Omega$                                                   | 105                |                                | MHz              |
| $\phi_m$      | Phase Margin                      | $R_L = 1k\Omega$                                                   | 74                 |                                | Deg              |
| $f$ (-3 dB)   | Bandwidth <sup>(4)(5)</sup>       | $R_L = 100\Omega$ , $A_V = +1$                                     | 160                |                                | MHz              |
|               |                                   | $R_L = 100\Omega$ , $A_V = +2$                                     | 50                 |                                | MHz              |
| $t_s$         | Settling Time                     | 5 $V_{PP}$ Step, to 0.1%, $R_L = 500\Omega$                        | 65                 |                                | ns               |
| $t_r$ , $t_f$ | Rise and Fall Time <sup>(5)</sup> | $A_V = +2$ , $R_L = 100\Omega$ , $V_O = 0.4V_{PP}$                 | 5.8                |                                | ns               |
| $A_D$         | Differential Gain                 | $A_V = +2$ , $R_L = 150\Omega$                                     | 0.3%               |                                |                  |
| $\phi_D$      | Differential Phase                | $A_V = +2$ , $R_L = 150\Omega$                                     | 0.65               |                                | Deg              |
| $e_n$         | Input-Referred Voltage Noise      | $f = 10$ kHz                                                       | 17                 |                                | nV / $\sqrt{Hz}$ |
| $i_n$         | Input-Referred Current Noise      | $f = 10$ kHz                                                       | 2                  |                                | pA / $\sqrt{Hz}$ |
| T.H.D.        | Total Harmonic Distortion         | 2 $V_{PP}$ Output, $R_L = 150\Omega$ ,<br>$A_V = +2$ , $f = 1$ MHz | 0.1%               |                                |                  |
|               |                                   | 2 $V_{PP}$ Output, $R_L = 150\Omega$ ,<br>$A_V = +2$ , $f = 5$ MHz | 0.6                |                                |                  |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Unity gain operation for  $\pm 5V$  and  $\pm 15V$  supplies is with a feedback network of  $510\Omega$  and  $3pF$  in parallel (see [Application and Implementation](#)). For  $+5V$  single supply operation, feedback is a direct short from the output to the inverting input.

(5)  $A_V = +2$  operation with  $2k\Omega$  resistors and  $2pF$  capacitor from summing node to ground.

## LM7121

SNOS750A – AUGUST 1999 – REVISED OCTOBER 2014

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### 6.9 +5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1M\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER                                   | TEST CONDITIONS                     | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT    |
|---------------------------------------------|-------------------------------------|--------------------|--------------------------------|---------|
| $V_{OS}$ Input Offset Voltage               |                                     | 2.4                |                                | mV      |
| $I_B$ Input Bias Current                    |                                     | 4                  |                                | $\mu A$ |
| $I_{OS}$ Input Offset Current               |                                     | 0.04               |                                | $\mu A$ |
| $R_{IN}$ Input Resistance                   | Common Mode                         | 2.6                |                                | M       |
|                                             | Differential Mode                   | 3.4                |                                | M       |
| $C_{IN}$ Input Capacitance                  | Common Mode                         | 2.3                |                                | pF      |
| CMRR Common Mode Rejection Ratio            | $2V \leq V_{CM} \leq 3V$            | 65                 |                                | dB      |
| +PSRR Positive Power Supply Rejection Ratio | $4.6V \leq V^+ \leq 5V$             | 85                 |                                | dB      |
| –PSRR Negative Power Supply Rejection Ratio | $0V \leq V^- \leq 0.4V$             | 61                 |                                | dB      |
| $V_{CM}$ Input Common-Mode Voltage Range    | CMRR 45 dB                          | 3.5                |                                | V min   |
|                                             |                                     | 1.5                |                                | V max   |
| $A_V$ Large Signal Voltage Gain             | $R_L = 2k\Omega$ to $V^+/2$         | 64                 |                                | dB      |
| $V_O$ Output Swing                          | $R_L = 2k\Omega$ to $V^+/2$ , High  | 3.7                |                                | V       |
|                                             | $R_L = 2k\Omega$ to $V^+/2$ , Low   | 1.3                |                                |         |
|                                             | $R_L = 150\Omega$ to $V^+/2$ , High | 3.48               |                                |         |
|                                             | $R_L = 150\Omega$ to $V^+/2$ , Low  | 1.59               |                                |         |
| $I_{SC}$ Output Short Circuit Current       | Sourcing                            | 33                 |                                | mA      |
|                                             | Sinking                             | 20                 |                                | mA      |
| $I_S$ Supply Current                        |                                     | 4.8                |                                | mA      |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

### 6.10 +5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $V^+ = +5V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1M\Omega$ . **Boldface** limits apply at the temperature extremes.

| PARAMETER                                       | TEST CONDITIONS                                                  | TYP <sup>(1)</sup> | LM7121<br>LIMIT <sup>(2)</sup> | UNIT       |
|-------------------------------------------------|------------------------------------------------------------------|--------------------|--------------------------------|------------|
| SR Slew Rate <sup>(3)</sup>                     | $A_V = +2$ , $R_L = 1k\Omega$ to $V^+/2$ , $V_O = 1.8V_{PP}$     | 145                |                                | V/ $\mu s$ |
| GBW Unity Gain-Bandwidth                        | $R_L = 1k$ to $V^+/2$                                            | 80                 |                                | MHz        |
| $\phi_m$ Phase Margin                           | $R_L = 1k$ to $V^+/2$                                            | 70                 |                                | Deg        |
| f (–3 dB) Bandwidth <sup>(4)(5)</sup>           | $R_L = 100\Omega$ to $V^+/2$ , $A_V = +1$                        | 200                |                                | MHz        |
|                                                 | $R_L = 100\Omega$ to $V^+/2$ , $A_V = +2$                        | 45                 |                                |            |
| $t_r$ , $t_f$ Rise and Fall Time <sup>(5)</sup> | $A_V = +2$ , $R_L = 100\Omega$ , $V_O = 0.2V_{PP}$               | 8                  |                                | ns         |
| T.H.D. Total Harmonic Distortion                | 0.6 $V_{PP}$ Output, $R_L = 150\Omega$ , $A_V = +2$ , $f = 1MHz$ | 0.067%             |                                |            |
|                                                 | 0.6 $V_{PP}$ Output, $R_L = 150\Omega$ , $A_V = +2$ , $f = 5MHz$ | 0.33%              |                                |            |

(1) Typical Values represent the most likely parametric norm.

(2) All limits are ensured by testing or statistical analysis.

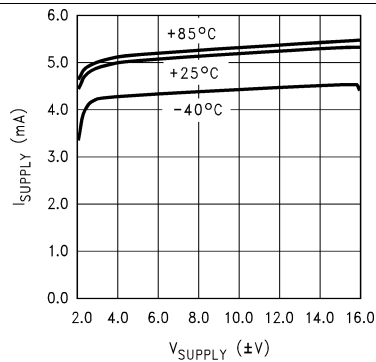
(3) Slew rate is the average of the rising and falling slew rates.

(4) Unity gain operation for  $\pm 5V$  and  $\pm 15V$  supplies is with a feedback network of  $510\Omega$  and  $3pF$  in parallel (see [Application and Implementation](#)). For +5V single supply operation, feedback is a direct short from the output to the inverting input.

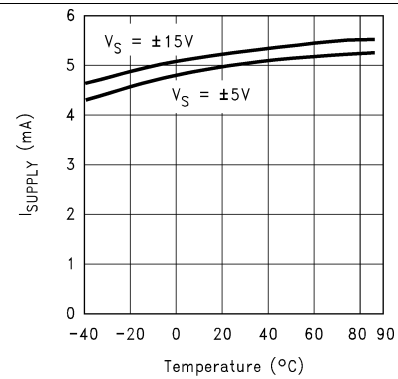
(5)  $A_V = +2$  operation with  $2k\Omega$  resistors and  $2pF$  capacitor from summing node to ground.



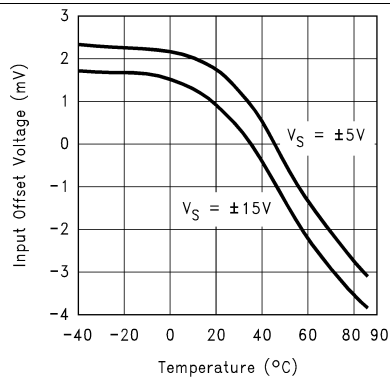
## 6.11 Typical Characteristics



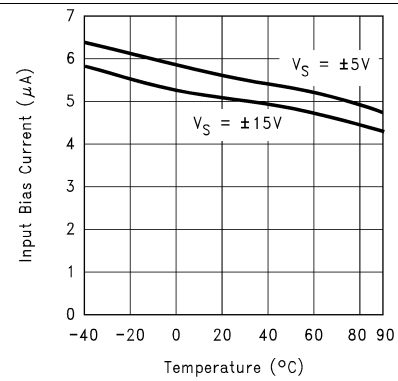
**Figure 1. Supply Current vs. Supply Voltage**



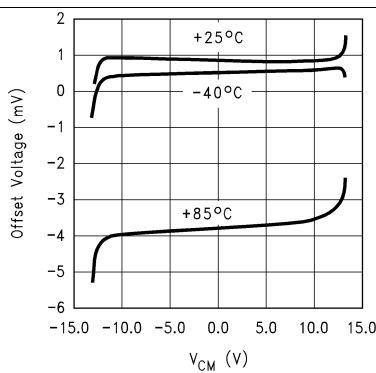
**Figure 2. Supply Current vs. Temperature**



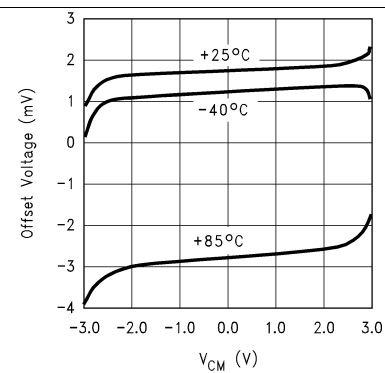
**Figure 3. Input Offset Voltage vs. Temperature**



**Figure 4. Input Bias Current vs. Temperature**

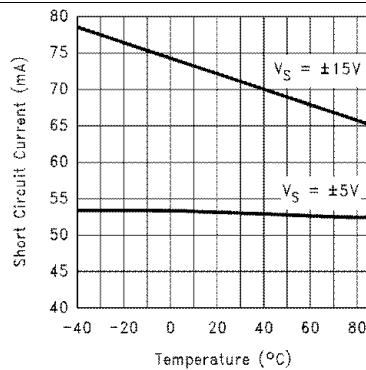
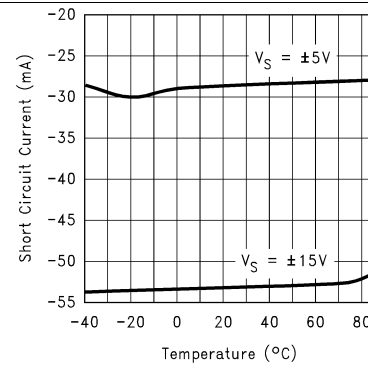
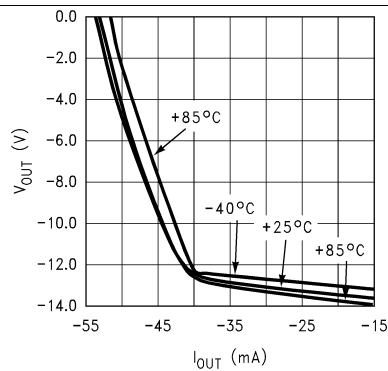
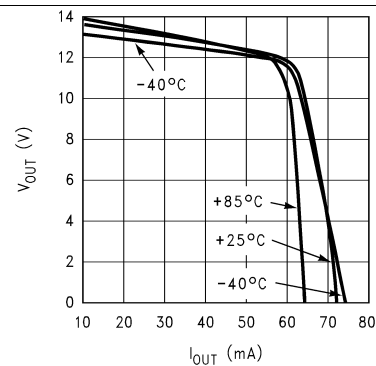
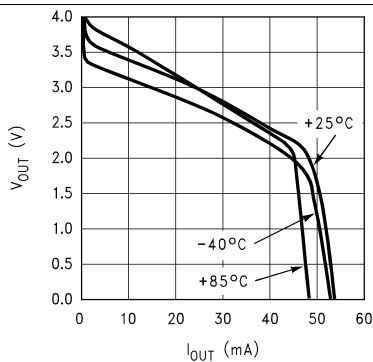
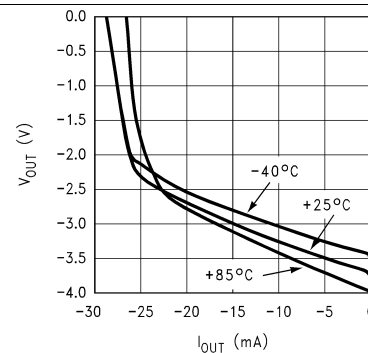


**Figure 5. Input Offset Voltage vs. Common Mode Voltage at  $V_S = \pm 15\text{ V}$**

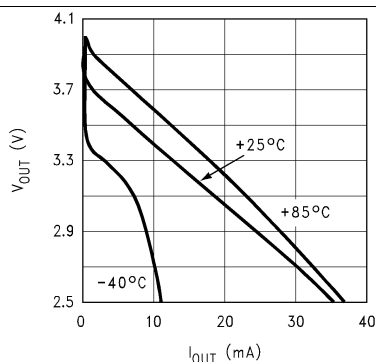


**Figure 6. Input Offset Voltage vs. Common Mode Voltage at  $V_S = \pm 5\text{ V}$**

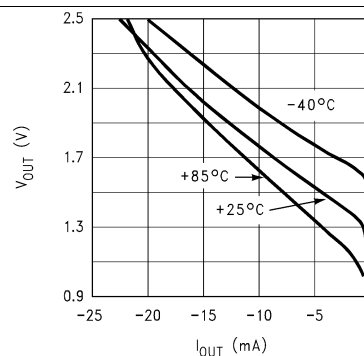
## Typical Characteristics (continued)


**Figure 7. Short Circuit Current vs. Temperature (Sourcing)**

**Figure 8. Short Circuit Current vs Temperature (Sinking)**

**Figure 9. Output Voltage vs Output Current  
( $I_{\text{SINK}}$ ,  $V_S = \pm 15 \text{ V}$ )**

**Figure 10. Output Voltage vs Output Current  
( $I_{\text{SOURCE}}$ ,  $V_S = \pm 15 \text{ V}$ )**

**Figure 11. Output Voltage vs Output Current  
( $I_{\text{SOURCE}}$ ,  $V_S = \pm 5 \text{ V}$ )**

**Figure 12. Output Voltage vs Output Current  
( $I_{\text{SINK}}$ ,  $V_S = \pm 5 \text{ V}$ )**

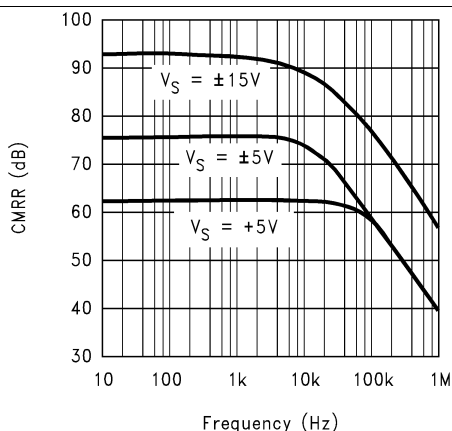
## Typical Characteristics (continued)



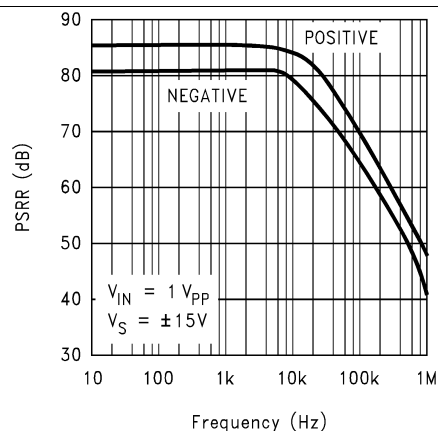
**Figure 13. Output Voltage vs. Output Current**  
( $I_{SOURCE}$ ,  $V_S = +5\text{ V}$ )



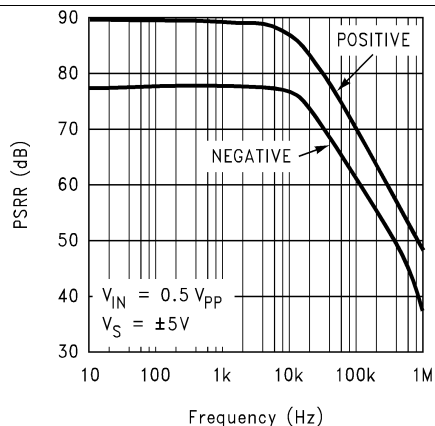
**Figure 14. Output Voltage vs. Output Current**  
( $I_{SINK}$ ,  $V_S = +5\text{ V}$ )



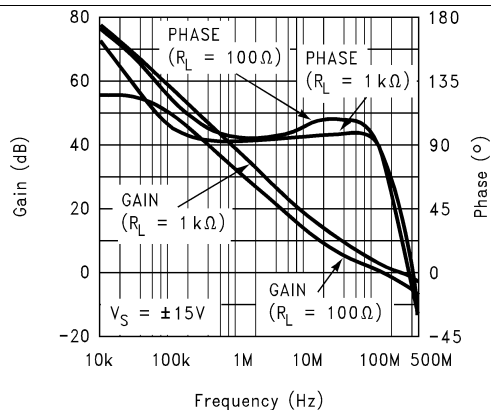
**Figure 15. CMRR vs. Frequency**



**Figure 16. PSRR vs. Frequency**

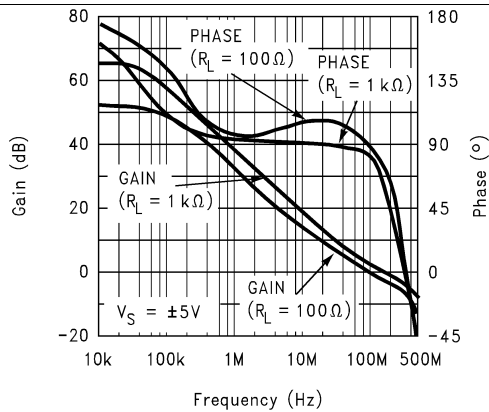
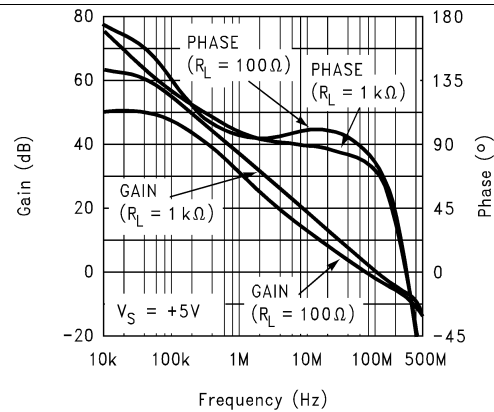
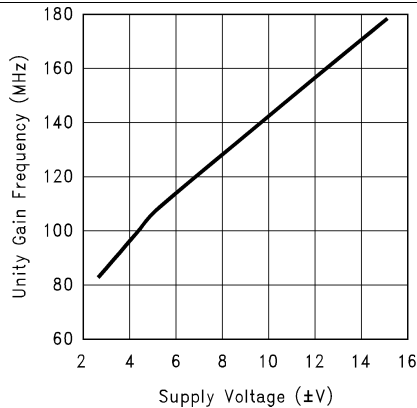
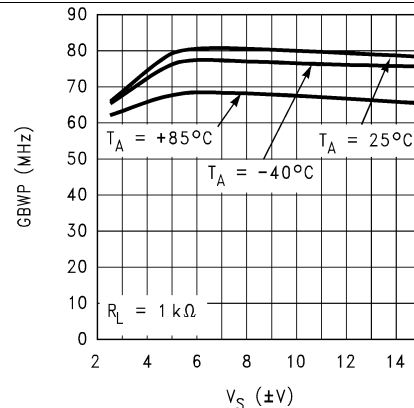
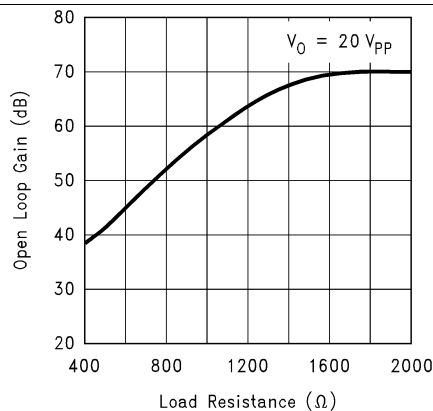
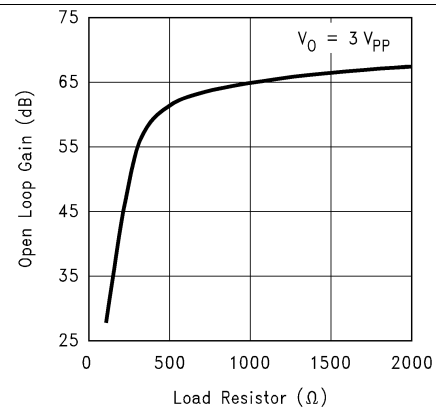


**Figure 17. PSRR vs. Frequency**

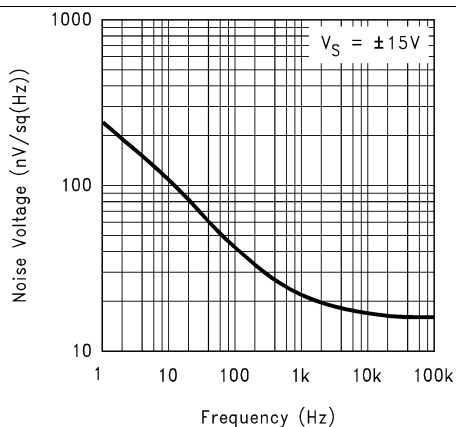


**Figure 18. Open Loop Frequency Response**

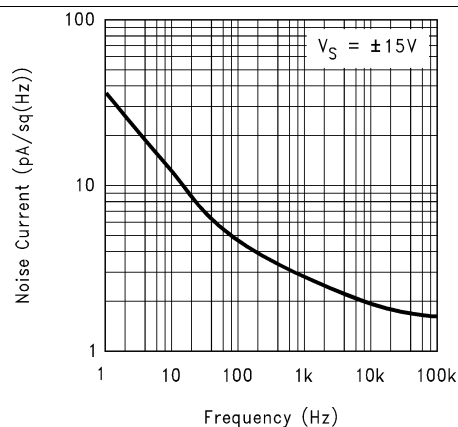
## Typical Characteristics (continued)


**Figure 19. Open Loop Frequency Response**

**Figure 20. Open Loop Frequency Response**

**Figure 21. Unity Gain Frequency vs. Supply Voltage**

**Figure 22. GBWP at 10 MHz vs. Supply Voltage**

**Figure 23. Large Signal Voltage Gain vs. Load,  $V_S = \pm 15V$** 

**Figure 24. Large Signal Voltage Gain vs. Load,  $V_S = \pm 5V$**

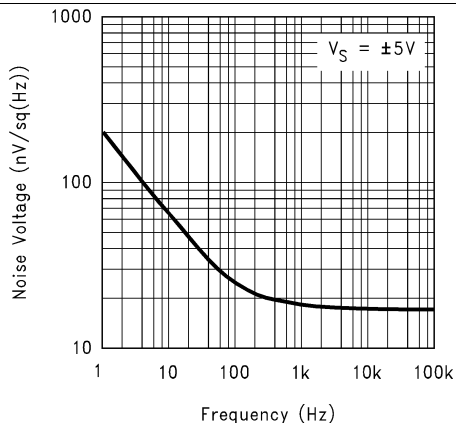
## Typical Characteristics (continued)



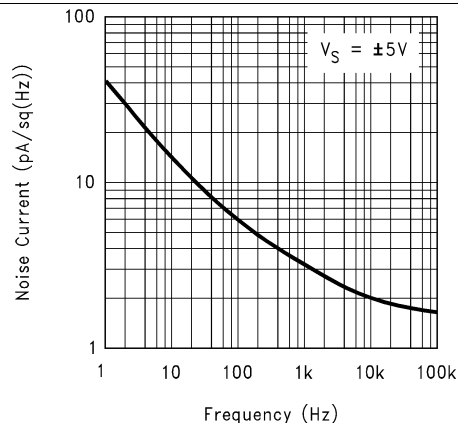
**Figure 25. Input Voltage Noise vs. Frequency**



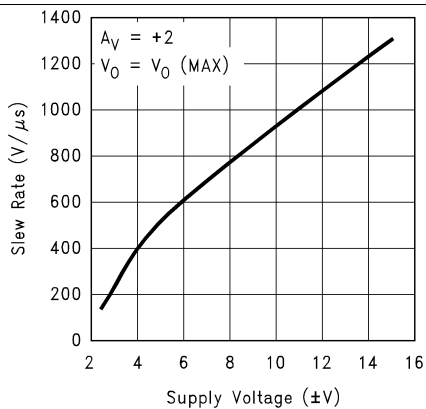
**Figure 26. Input Current Noise vs. Frequency**



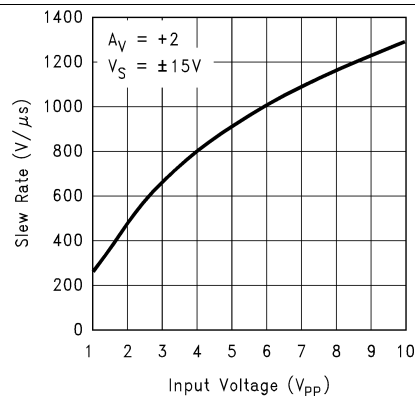
**Figure 27. Input Voltage Noise vs. Frequency**



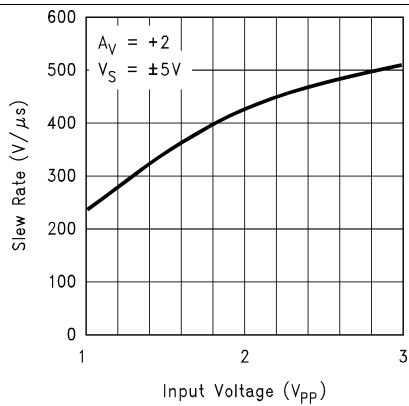
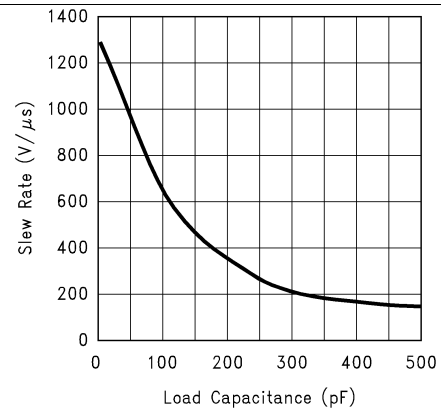
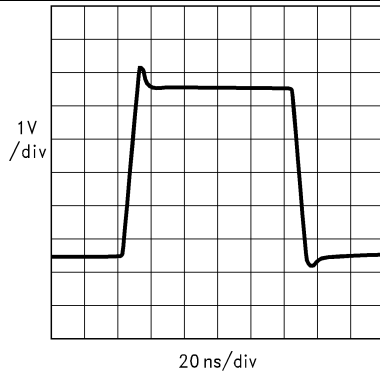
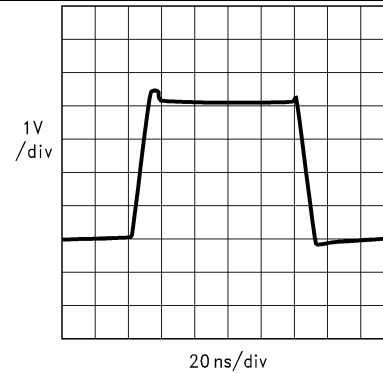
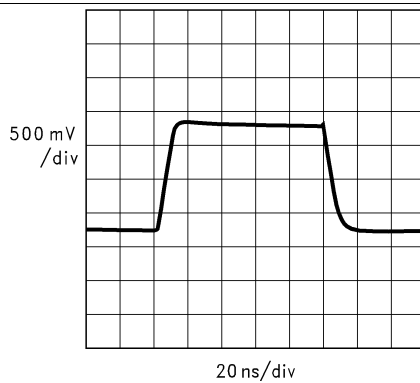
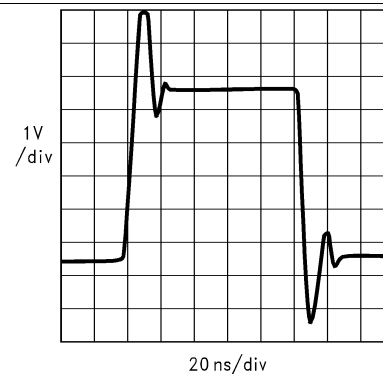
**Figure 28. Input Current Noise vs. Frequency**



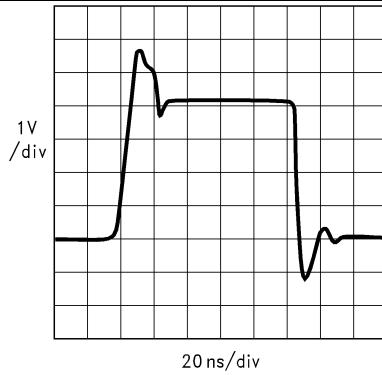
**Figure 29. Slew Rate vs. Supply Voltage**



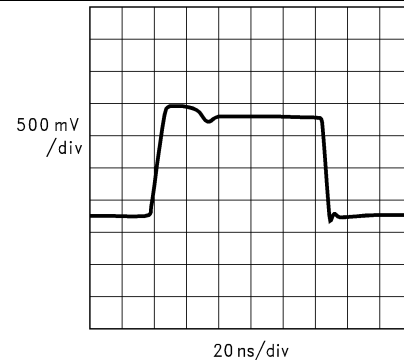
**Figure 30. Slew Rate vs. Input Voltage**

**Typical Characteristics (continued)**

**Figure 31. Slew Rate vs. Input Voltage**

**Figure 32. Slew Rate vs. Load Capacitance**

**Figure 33. Large Signal Pulse Response,  
 $A_V = -1$ ,  $V_S = \pm 15$  V**

**Figure 34. Large Signal Pulse Response,  
 $A_V = -1$ ,  $V_S = \pm 5$  V**

**Figure 35. Large Signal Pulse Response,  
 $A_V = -1$ ,  $V_S = +5$  V**

**Figure 36. Large Signal Pulse Response,  
 $A_V = +1$ ,  $V_S = \pm 15$  V**

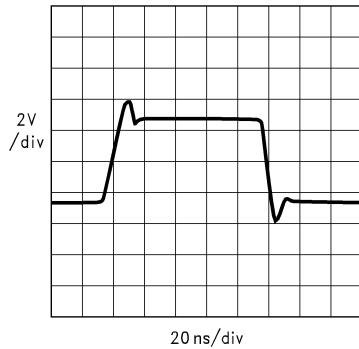
## Typical Characteristics (continued)



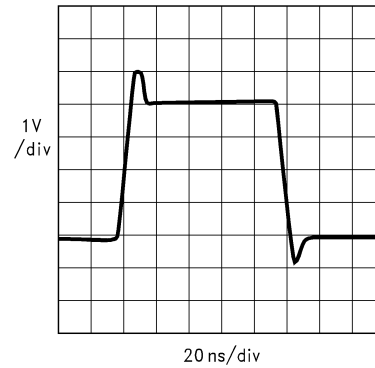
**Figure 37. Large Signal Pulse Response,**  
 $A_V = +1$ ,  $V_S = \pm 5$  V



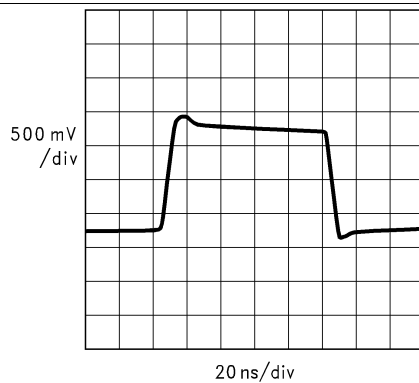
**Figure 38. Large Signal Pulse Response,**  
 $A_V = +1$ ,  $V_S = +5$  V



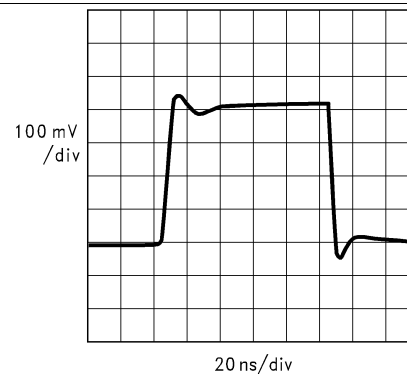
**Figure 39. Large Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = \pm 15$  V



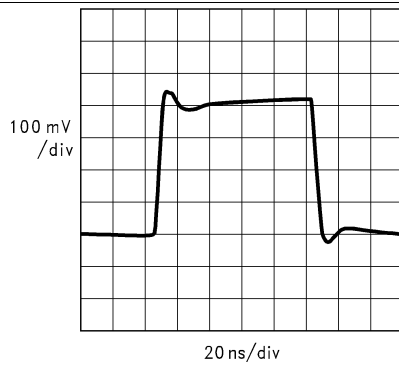
**Figure 40. Large Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = \pm 5$  V



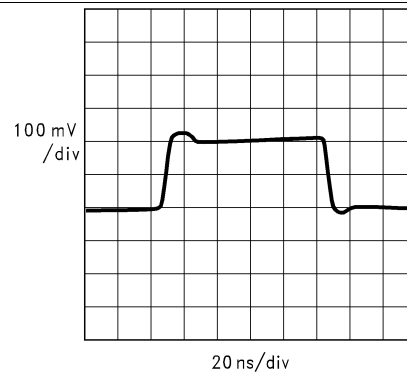
**Figure 41. Large Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = +5$  V



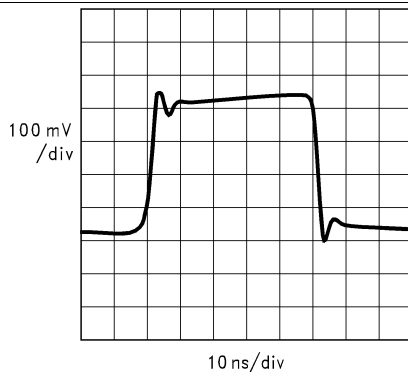
**Figure 42. Small Signal Pulse Response,**  
 $A_V = -1$ ,  $V_S = \pm 15$  V,  $R_L = 100 \Omega$

**Typical Characteristics (continued)**


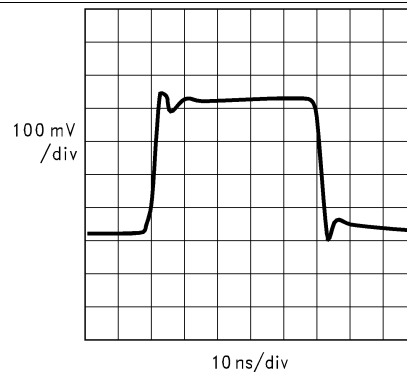
**Figure 43. Small Signal Pulse Response,**  
 $A_V = -1$ ,  $V_S = \pm 5$  V,  $R_L = 100 \Omega$



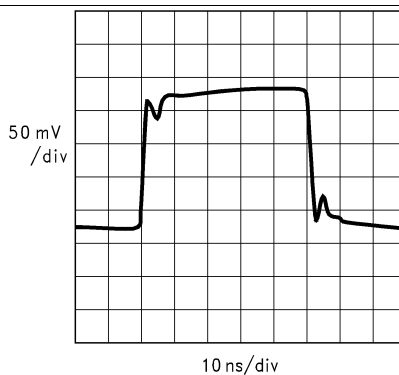
**Figure 44. Small Signal Pulse Response,**  
 $A_V = -1$ ,  $V_S = +5$  V,  $R_L = 100 \Omega$



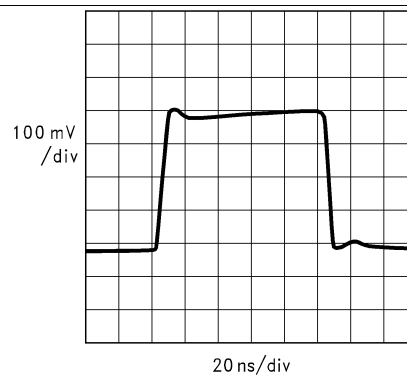
**Figure 45. Small Signal Pulse Response,**  
 $A_V = +1$ ,  $V_S = \pm 15$  V,  $R_L = 100 \Omega$



**Figure 46. Small Signal Pulse Response,**  
 $A_V = +1$ ,  $V_S = \pm 5$  V,  $R_L = 100 \Omega$



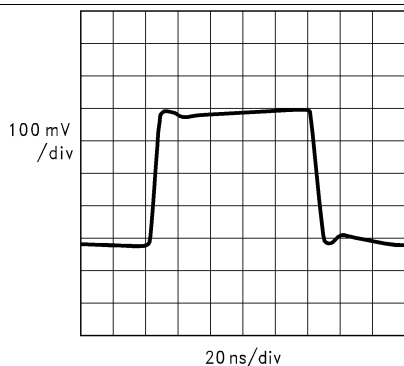
**Figure 47. Small Signal Pulse Response,**  
 $A_V = +1$ ,  $V_S = +5$  V,  $R_L = 100 \Omega$



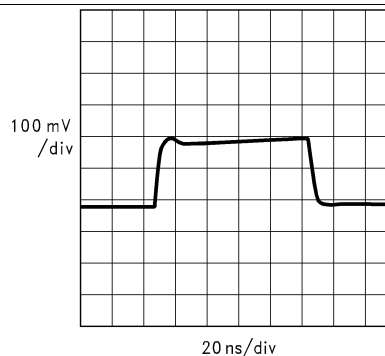
**Figure 48. Small Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = \pm 15$  V,  $R_L = 100 \Omega$



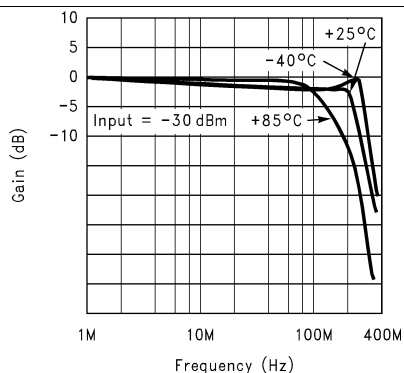
## Typical Characteristics (continued)



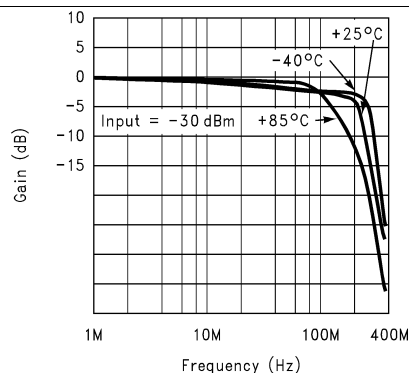
**Figure 49. Small Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = \pm 5$  V,  $R_L = 100$   $\Omega$



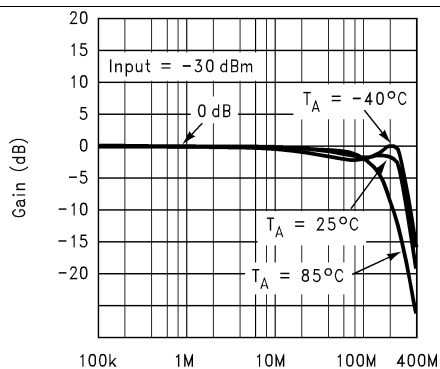
**Figure 50. Small Signal Pulse Response,**  
 $A_V = +2$ ,  $V_S = +5$  V,  $R_L = 100$   $\Omega$



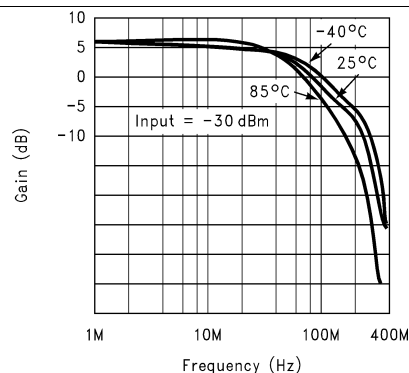
**Figure 51. Closed Loop Frequency Response vs. Temperature,**  
 $V_S = \pm 15$  V,  $A_V = +1$ ,  $R_L = 100$   $\Omega$



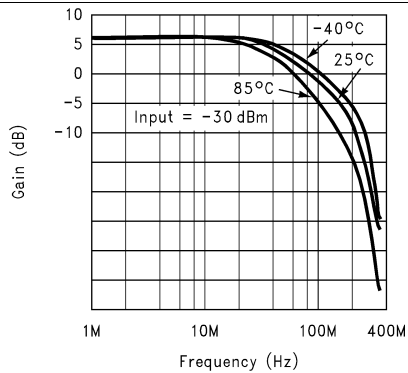
**Figure 52. Closed Loop Frequency Response vs. Temperature**  
 $V_S = \pm 5$  V,  $A_V = +1$ ,  $R_L = 100$   $\Omega$



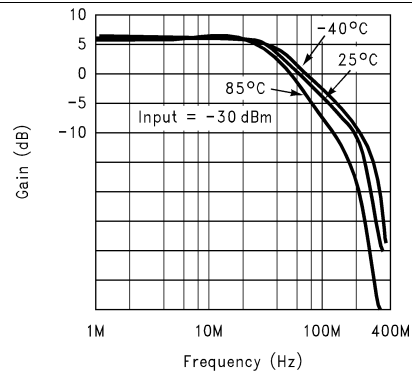
**Figure 53. Closed Loop Frequency Response vs. Temperature,**  
 $V_S = +5$  V,  $A_V = +1$ ,  $R_L = 100$   $\Omega$



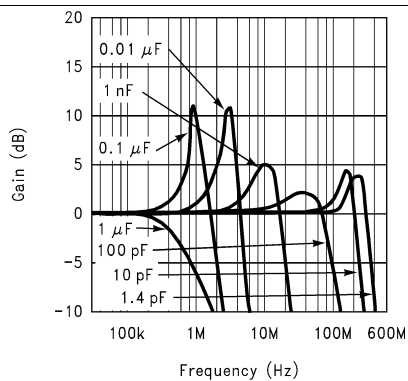
**Figure 54. Closed Loop Frequency Response vs. Temperature,**  
 $V_S = \pm 15$  V,  $A_V = +2$ ,  $R_L = 100$   $\Omega$

**Typical Characteristics (continued)**


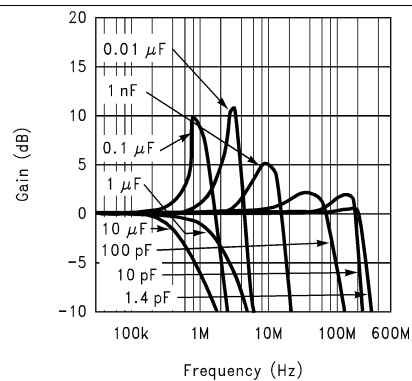
**Figure 55. Closed Loop Frequency Response vs. Temperature,**  
 $V_S = \pm 5\text{ V}$ ,  $A_V = +2$ ,  $R_L = 100\ \Omega$



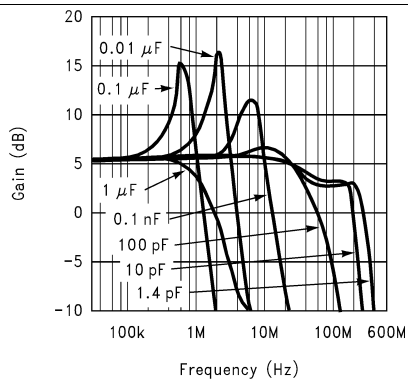
**Figure 56. Closed Loop Frequency Response vs. Temperature,**  
 $V_S = +5\text{ V}$ ,  $A_V = +2$ ,  $R_L = 100\ \Omega$



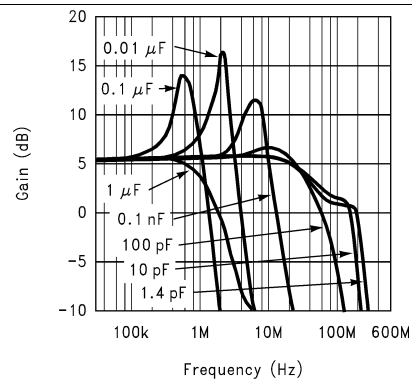
**Figure 57. Closed Loop Frequency Response vs. Capacitance Load**  
 $(A_V = +1, V_S = \pm 15\text{ V})$



**Figure 58. Closed Loop Frequency Response vs. Capacitive Load**  
 $(A_V = +1, V_S = \pm 5\text{ V})$

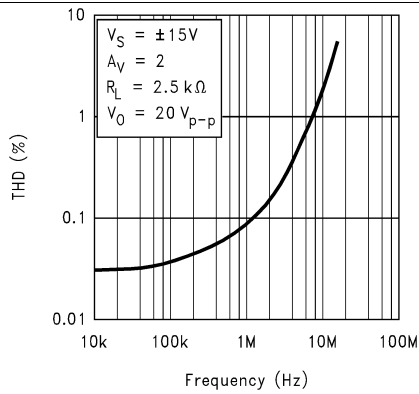


**Figure 59. Closed Loop Frequency Response vs. Capacitive Load**  
 $(A_V = +2, V_S = \pm 15\text{ V})$

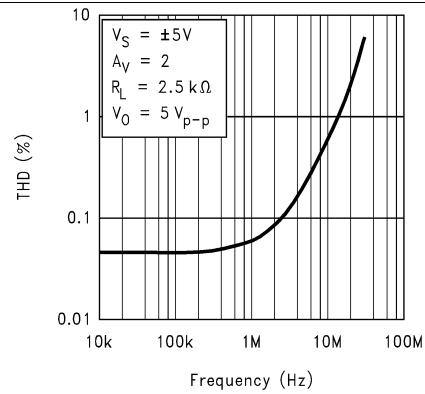


**Figure 60. Closed Loop Frequency Response vs. Capacitive Load**  
 $(A_V = +2, V_S = \pm 5\text{ V})$

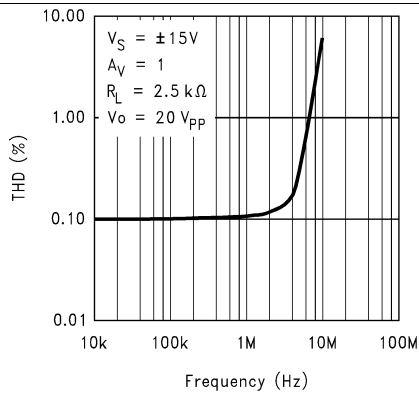
## Typical Characteristics (continued)



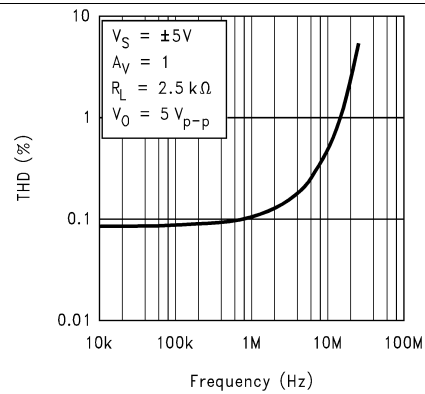
**Figure 61. Total Harmonic Distortion vs. Frequency**



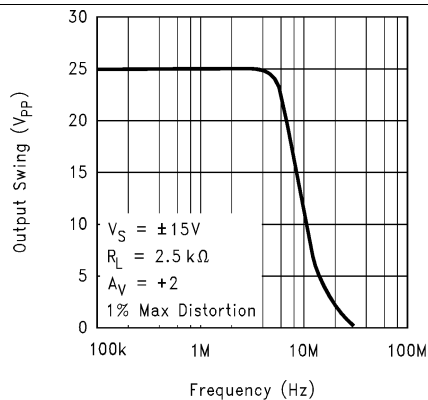
**Figure 62. Total Harmonic Distortion vs. Frequency**



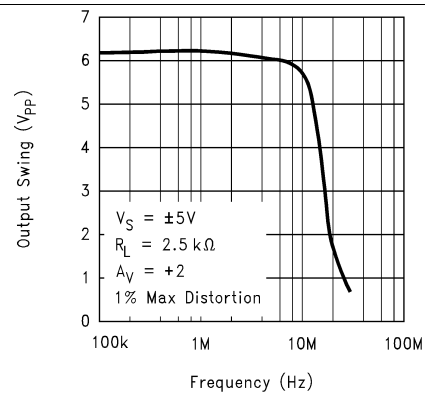
**Figure 63. Total Harmonic Distortion vs. Frequency**



**Figure 64. Total Harmonic Distortion vs. Frequency**



**Figure 65. Undistorted Output Swing vs. Frequency**



**Figure 66. Undistorted Output Swing vs. Frequency**

## Typical Characteristics (continued)

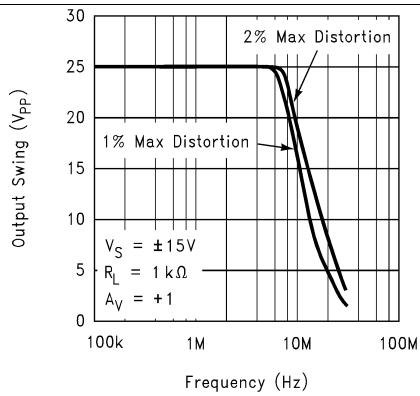


Figure 67. Undistorted Output Swing vs. Frequency

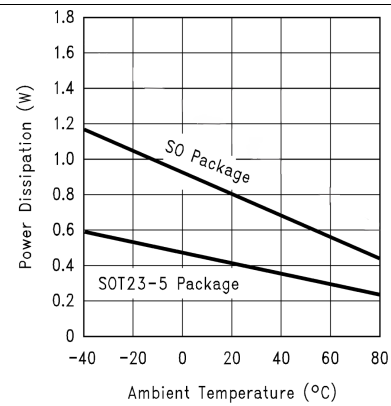


Figure 68. Total Power Dissipation vs. Ambient Temperature

## 7 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

[Table 1](#) depicts the maximum operating supply voltage for each package type

**Table 1. Maximum Supply Voltage Values**

|               | SOT-23 | SO-8  |
|---------------|--------|-------|
| Single Supply | 10 V   | 30 V  |
| Dual Supplies | ±5 V   | ±15 V |

Stable unity gain operation is possible with supply voltage of 5 V for all capacitive loads. This allows the possibility of using the device in portable applications with low supply voltages with minimum components around it.

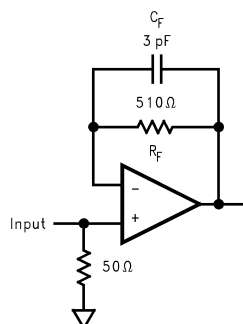
Above a supply voltage of 6 V ( $\pm 3$  V Dual supplies), an additional resistor and capacitor (shown in [Figure 69](#)) should be placed in the feedback path to achieve stability at unity gain over the full temperature range.

The package power dissipation should be taken into account when operating at high ambient temperatures and/or high power dissipative conditions. Refer to the power derating curves in the data sheet for each type of package.

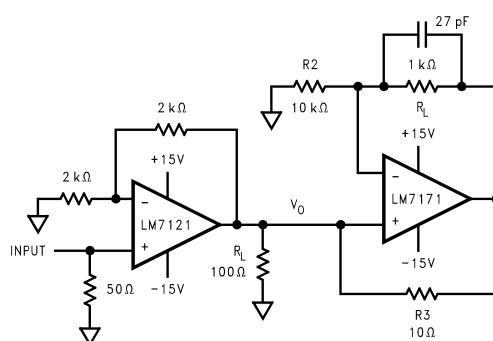
In determining maximum operable temperature of the device, make sure the total power dissipation of the device is considered; this includes the power dissipated in the device with a load connected to the output as well as the nominal dissipation of the op amp.

The device is capable of tolerating momentary short circuits from its output to ground but prolonged operation in this mode will damage the device, if the maximum allowed junction temperature is exceeded.

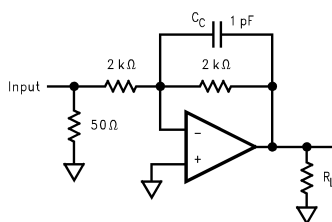
## 7.2 Typical Applications



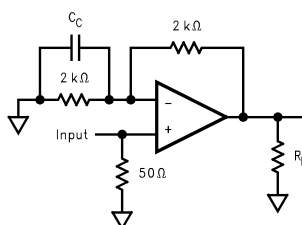
**Figure 69. Typical Circuit for  $A_V = +1$  Operation ( $V_S = 6$  V)**



**Figure 70. Simple Circuit to Improve Linearity and Output Drive Current**



**Figure 71.  $A_V = -1$**

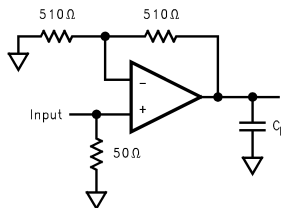


$C_C = 2$  pF for  $R_L = 100$  Ω

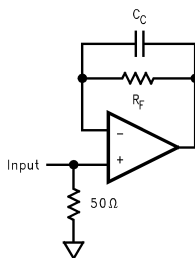
$C_C =$  Open for  $R_L =$  Open

**Figure 72.  $A_V = +2$**

## Typical Applications (continued)

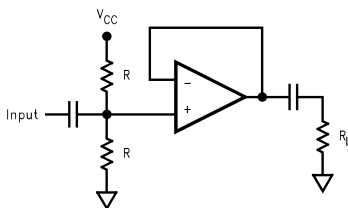


**Figure 73.  $A_V = +2$ , Capacitive Load**



$R_F = 0 \, \Omega$ ,  $C_C = \text{Open}$  for  $V_S < 6 \, \text{V}$   
 $R_F = 510 \, \Omega$ ,  $C_C = 3 \, \text{pF}$  for  $V_S \geq 6 \, \text{V}$

**Figure 74.  $A_V = +1$**



$R_F = 0 \, \Omega$ ,  $C_C = \text{Open}$  for  $V_S < 6 \, \text{V}$   
 $R_F = 510 \, \Omega$ ,  $C_C = 3 \, \text{pF}$  for  $V_S \geq 6 \, \text{V}$

**Figure 75.  $A_V = +1$ .  $V_S = +5 \, \text{V}$ , Single Supply Operation**

### 7.2.1 Design Requirements

#### 7.2.1.1 Current Boost Circuit

The circuit in [Figure 70](#) can be used to achieve good linearity along with high output current capability.

By proper choice of  $R_3$ , the LM7121 output can be set to supply a minimal amount of current, thereby improving its output linearity.

$R_3$  can be adjusted to allow for different loads:

$$R_3 = 0.1 R_L \quad (1)$$

[Figure 70](#) has been set for a load of  $100 \, \Omega$ . Reasonable speeds ( $< 30 \, \text{ns}$  rise and fall times) can be expected up to  $120 \, \text{mA}$  of load current (see [Figure 77](#) for step response across the load).

## Typical Applications (continued)

### 7.2.2 Detailed Design Procedure

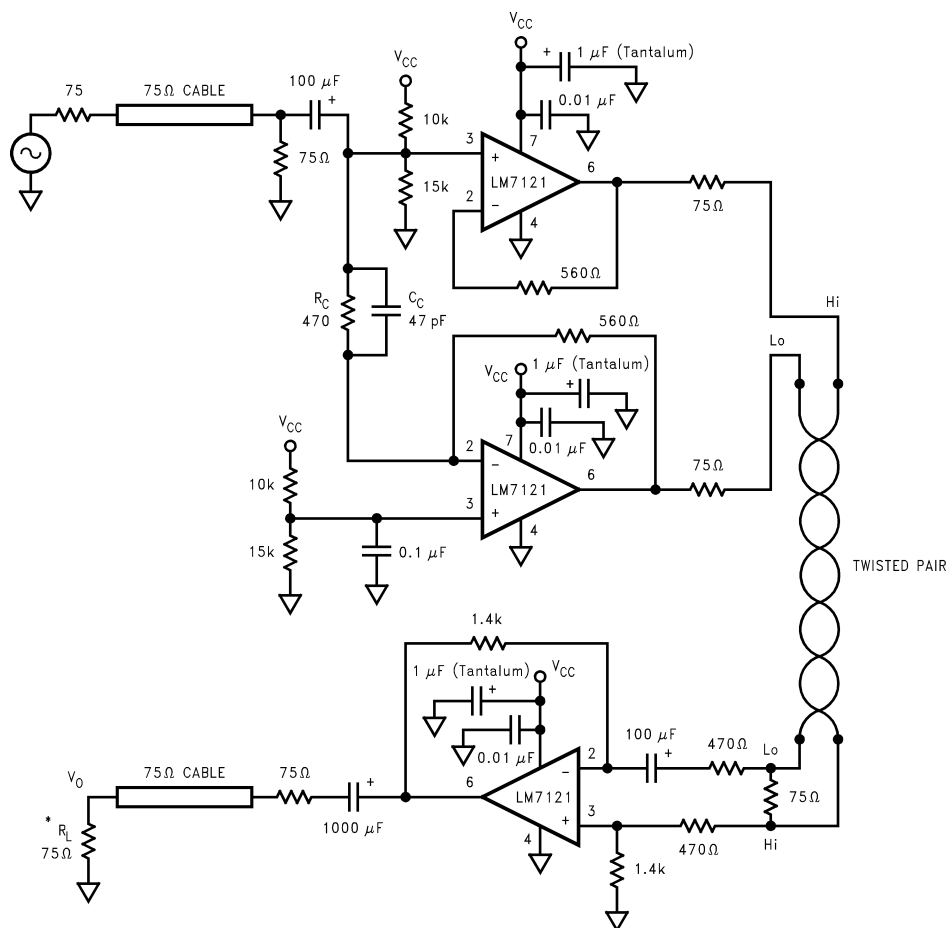
It is very important to keep the lead lengths to a minimum and to provide a low impedance current path by using a ground-plane on the board.

#### CAUTION

If  $R_L$  is removed, the current balance at the output of LM7121 would be disturbed and it would have to supply the full amount of load current. This might damage the part if power dissipation limit is exceeded.

#### 7.2.2.1 Color Video on Twisted Pairs Using Single Supply

The circuit shown in Figure 76 can be used to drive in excess of 25 meters length of twisted pair cable with no loss of resolution or picture definition when driving a NTSC monitor at the load end.



Pin numbers shown are for SO-8 package.

\* Input termination of NTSC monitor.

**Figure 76. Single Supply Differential Twisted Pair Cable Transmitter/Receiver,  
 $8.5\text{ V} \leq V_{CC} \leq 30\text{ V}$**



## Typical Applications (continued)

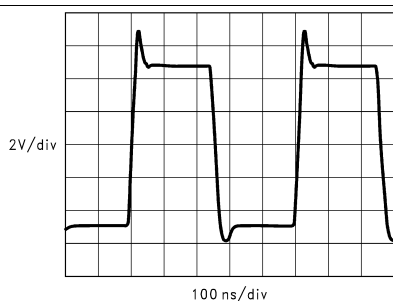
Differential Gain and Differential Phase errors measured at the load are less than 1% and 1° respectively

$R_G$  and  $C_C$  can be adjusted for various cable lengths to compensate for the line losses and for proper response at the output. Values shown correspond to a twisted pair cable length of 25 meters with about 3 turns/inch (see [Figure 78](#) for step response).

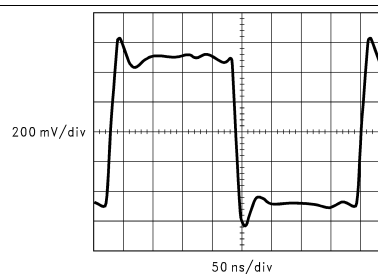
The supply voltage can vary from 8.5 V up to 30 V with the output rise and fall times under 12 ns. With the component values shown, the overall gain from the input to the output is about 1.

Even though the transmission line is not terminated in its nominal characteristic impedance of about 600  $\Omega$ , the resulting reflection at the load is only about 5% of the total signal and in most cases can be neglected. Using 75 termination instead, has the advantage of operating at a low impedance and results in a higher realizable bandwidth and signal fidelity.

### 7.2.3 Application Performance Plots



**Figure 77. Waveform across a 100- $\Omega$  Load**



**Figure 78. Step Response to a 1 V<sub>pp</sub> Input Signal Measured across the 75- $\Omega$  Load**

## 8 Device and Documentation Support

### 8.1 Trademarks

All trademarks are the property of their respective owners.

### 8.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM7121IM/NOPB</a>   | Active        | Production           | SOIC (D)   8     | 95   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LM71<br>21IM        |
| LM7121IM/NOPB.B                 | Active        | Production           | SOIC (D)   8     | 95   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LM71<br>21IM        |
| <a href="#">LM7121IM5/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   5 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | A03A                |
| LM7121IM5/NOPB.B                | Active        | Production           | SOT-23 (DBV)   5 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | A03A                |
| <a href="#">LM7121IM5X/NOPB</a> | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | A03A                |
| LM7121IM5X/NOPB.B               | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | A03A                |
| <a href="#">LM7121IMX/NOPB</a>  | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LM71<br>21IM        |
| LM7121IMX/NOPB.B                | Active        | Production           | SOIC (D)   8     | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LM71<br>21IM        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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