

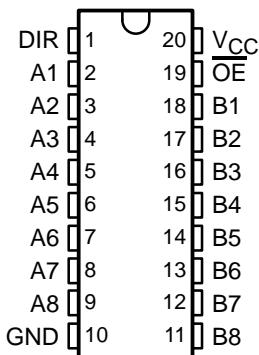
# SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS272A – NOVEMBER 1994 – REVISED JANUARY 2003

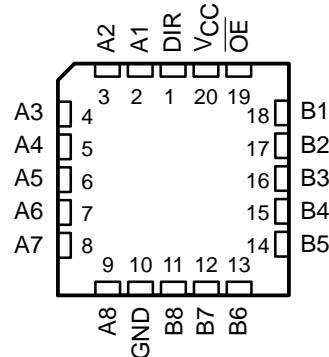
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 5.5 ns at 5 V
- 3-State Outputs Drive Bus Lines Directly
- pnp Inputs Reduce dc Loading

SN54ALS245A . . . J OR W PACKAGE  
SN54AS245 . . . J PACKAGE

SN74ALS245A . . . DB, DW, N, OR NS PACKAGE  
SN74AS245 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54ALS245A, SN54AS245 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS245A-1N
			SN74ALS245AN
			SN74AS245N
	SOIC – DW	Tube	SN74ALS245ADW
		Tape and reel	SN74ALS245ADWR
		Tube	SN74ALS245A-1DW
		Tape and reel	SN74ALS245A-1DWR
		Tube	SN74AS245DW
		Tape and reel	SN74AS245DWR
	SOP – NS	Tape and reel	SN74ALS245ANSR
		Tape and reel	SN74ALS245A-1NSR
		Tape and reel	SN74AS245NSR
	SSOP – DB	Tape and reel	SN74ALS245ADBR
-55°C to 125°C	CDIP – J	Tube	SNJ54ALS245AJ
			SNJ54AS245J
	CFP – W	Tube	SNJ54ALS245AW
			SNJ54ALS245AFK
	LCCC – FK	Tube	SNJ54ALS245AFK
			SNJ54AS245FK



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# **SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

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### **description/ordering information(continued)**

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

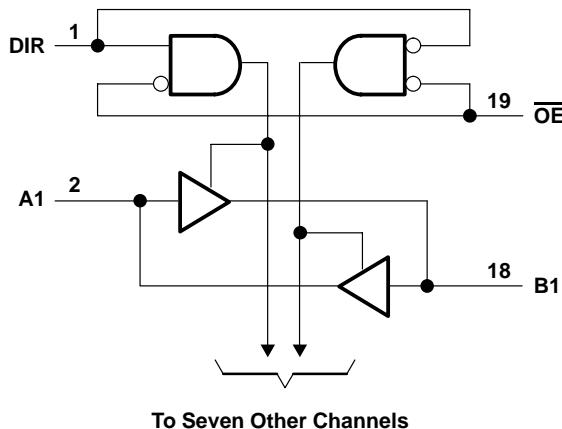
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The -1 version of the SN74ALS245A is identical to the standard version, except that the recommended maximum  $I_{OL}$  is increased to 48 mA. There is no -1 version of the SN54ALS245A.

## FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (SN54ALS245A, SN74ALS245A) (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
I/O ports .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



**SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 2)**

			SN54ALS245A			SN74ALS245A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.7			0.8	V
I <sub>OH</sub>	High-level output current				-12			-15	mA
I <sub>OL</sub>	Low-level output current				12			24	mA
								48 <sup>†</sup>	
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

<sup>†</sup> Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS245A			SN74ALS245A			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 2			V <sub>CC</sub> - 2			V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.2	2.4	3.2		
		I <sub>OH</sub> = -12 mA	2					
		I <sub>OH</sub> = -15 mA			2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4		V
		I <sub>OL</sub> = 24 mA			0.35	0.5		
		I <sub>OL</sub> = 48 mA <sup>†</sup>			0.35	0.5		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V		0.1		0.1	mA
	A or B ports		V <sub>I</sub> = 5.5 V		0.1		0.1	
I <sub>IH</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20		20		μA
	A or B ports <sup>§</sup>			20		20		
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.1		-0.1		mA
	A or B ports <sup>§</sup>			-0.1		-0.1		
I <sub>O</sub> <sup>¶</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-20	-112	-30	-112			mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	Outputs high	30	48	30	45		mA
		Outputs low	36	60	36	55		
		Outputs disabled	38	63	38	58		

<sup>†</sup> Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

<sup>‡</sup> All typical values are V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>¶</sup> The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.

# **SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R1 = 500\text{ }\Omega$ , $R2 = 500\text{ }\Omega$ , $T_A = \text{MIN to MAX}$				UNIT	
			SN54ALS245A		SN74ALS245A			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	B or A	1	19	3	10	ns	
$t_{PHL}$			1	14	3	10		
$t_{PZH}$	$\overline{OE}$	A or B	2	30	5	20	ns	
$t_{PZL}$			2	29	5	20		
$t_{PHZ}$	$\overline{OE}$	A or B	2	14	2	10	ns	
$t_{PLZ}$			2	30	4	15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (SN54AS245, SN74AS245)  
(unless otherwise noted)†**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
I/O ports .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 2)**

		SN54AS245			SN74AS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54AS245			SN74AS245			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2					
		$I_{OH} = -15 \text{ mA}$				2		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.3	0.55				V
		$I_{OL} = 64 \text{ mA}$			0.35	0.55		
$I_I$	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$		0.1		0.1		mA
		$V_I = 5.5 \text{ V}$		0.1		0.1		
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$		50		20		$\mu\text{A}$
				70		70		
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$		-0.5		-0.5		mA
				-0.75		-0.75		
$I_O^{\$}$	$V_{CC} = 5.5 \text{ V}$	$V_O = 2.25 \text{ V}$	-50	-150	-50	-150		mA
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$	Outputs high	62	97	62	97		mA
		Outputs low	95	143	95	143		
		Outputs disabled	79	123	79	123		

<sup>†</sup> All typical values are  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

<sup>§</sup> The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

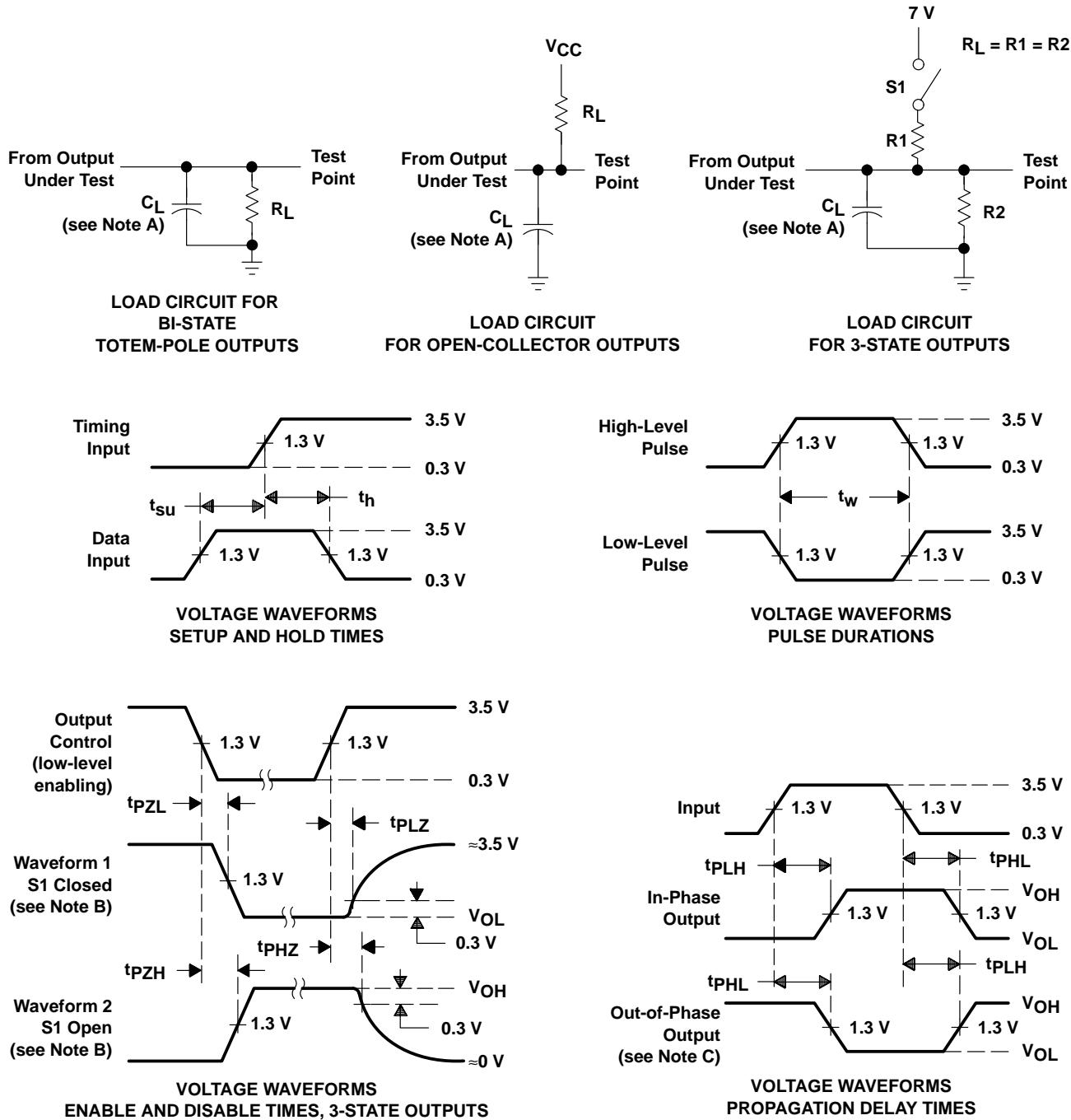
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $R1 = 500 \Omega$ , $R2 = 500 \Omega$ , $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS245		SN74AS245			
			MIN	MAX	MIN	MAX		
$t_{PLH}$	A or B	B or A	2	9.5	2	7.5	ns	
			2	9	2	7		
$t_{PHL}$	$\overline{OE}$	A or B	2	11	2	9	ns	
			2	10.5	2	8.5		
$t_{PZH}$	$\overline{OE}$	A or B	2	7.5	2	5.5	ns	
			2	12	2	9.5		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245  
OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
84030012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
8403001RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8403001SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN54ALS245AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN54AS245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN74ALS245A-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245A-1DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245A-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245A-1DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS245A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS245A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ADBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI
SN74ALS245ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS245AN3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS245ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS245ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS245ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
no Sb/Br)								
SN74AS245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS245AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS245AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS245AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS245FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54AS245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

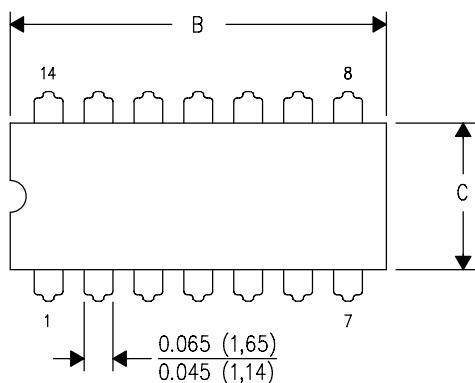
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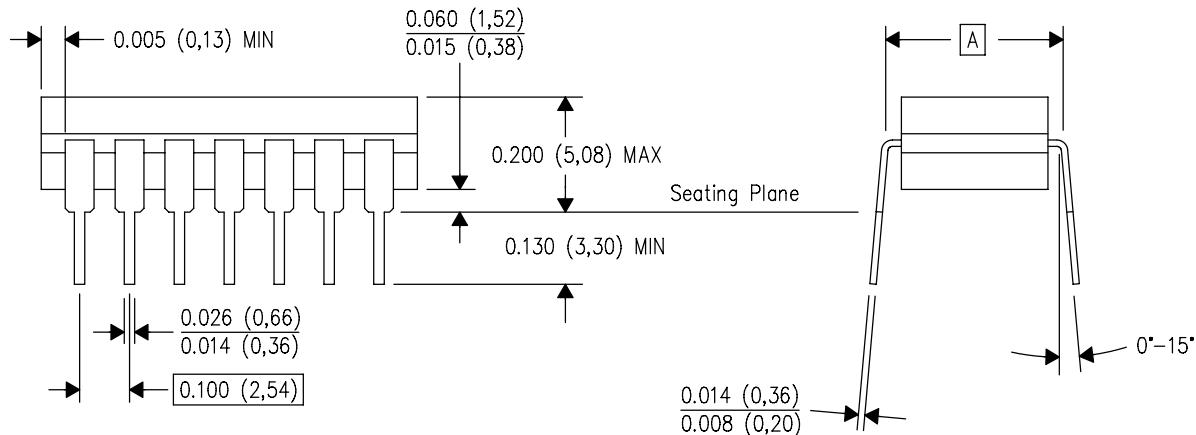
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

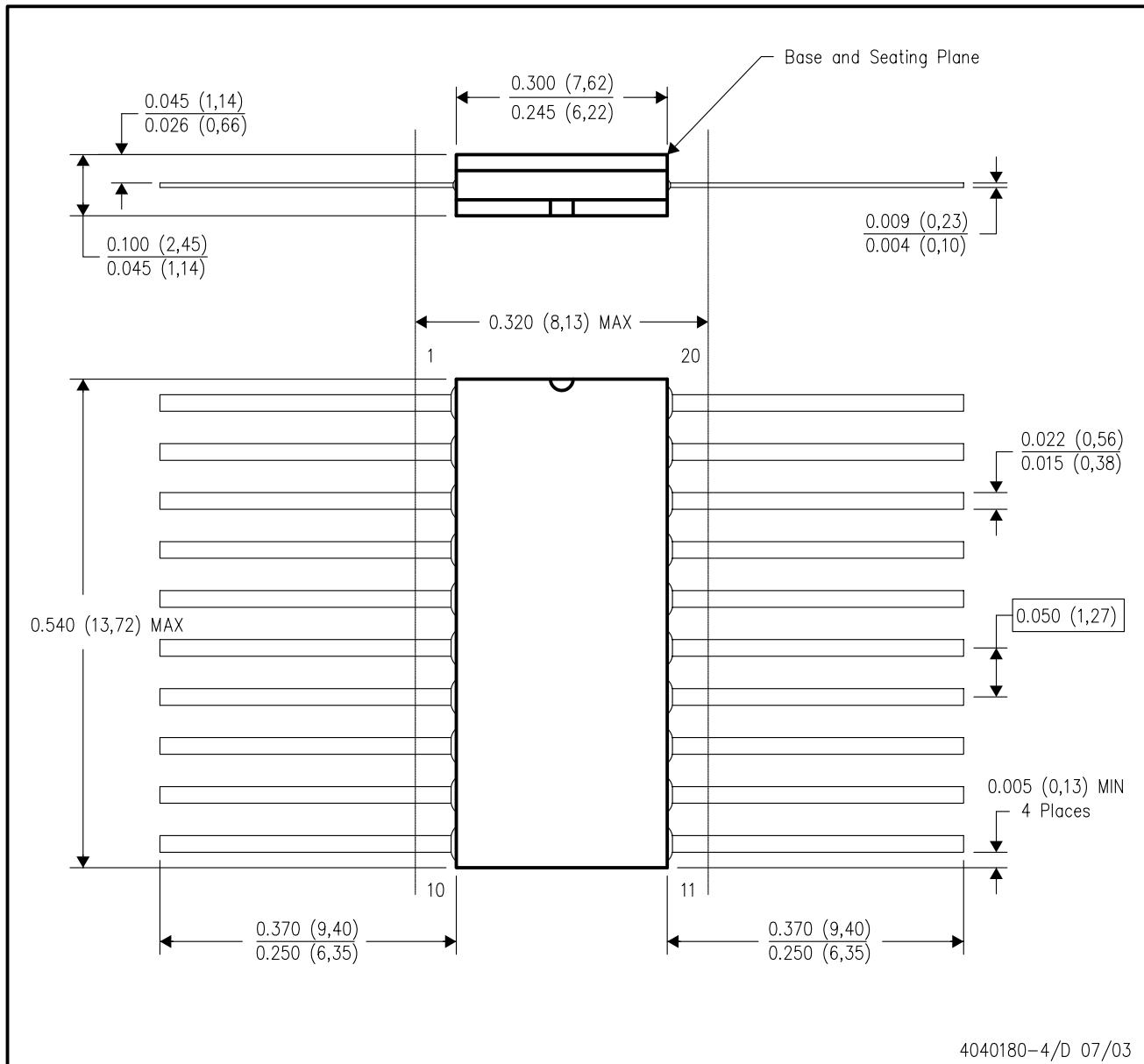


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

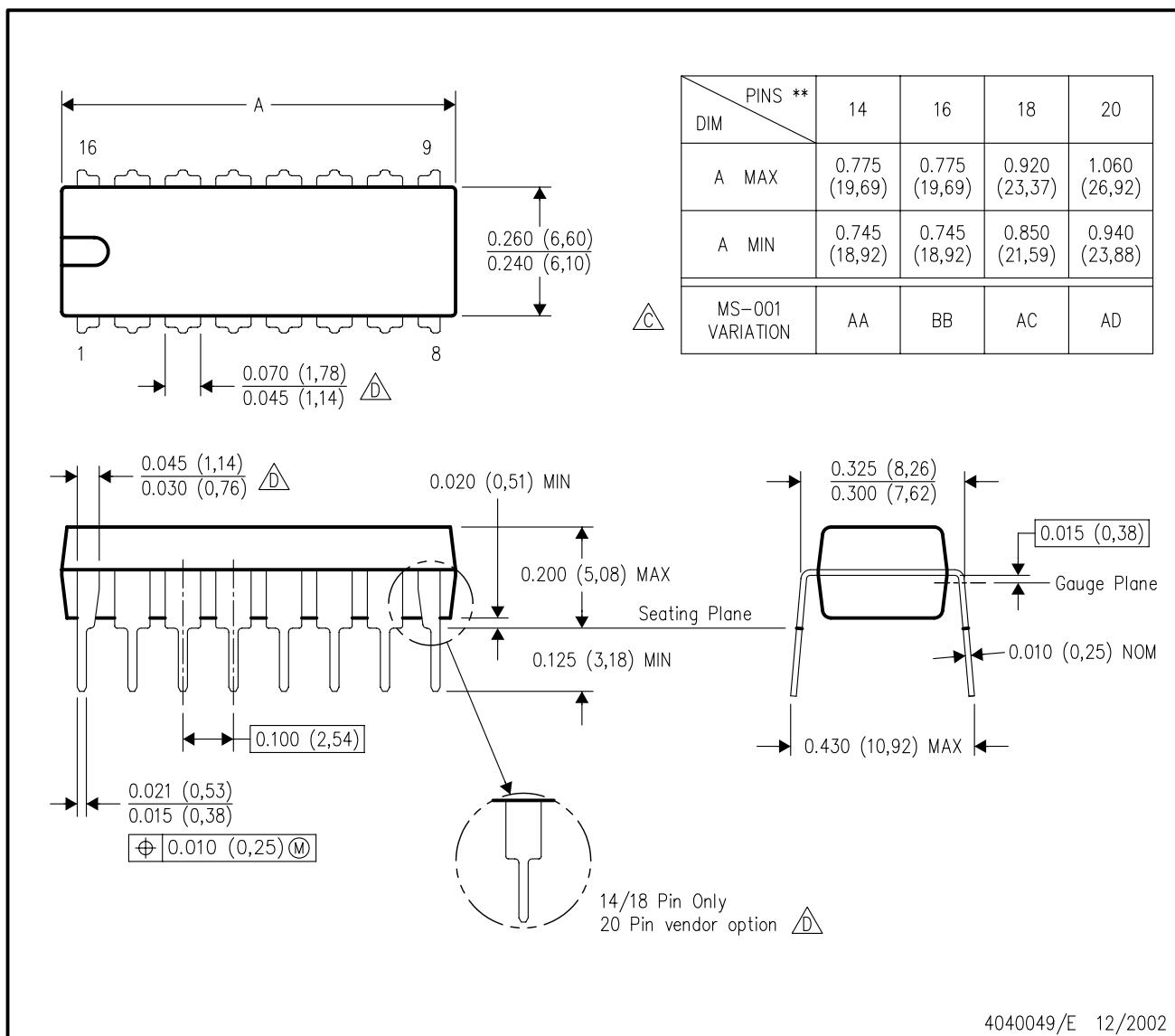
E. Falls within JEDEC MS-004

4040140/D 10/96

## N (R-PDIP-T\*\*)

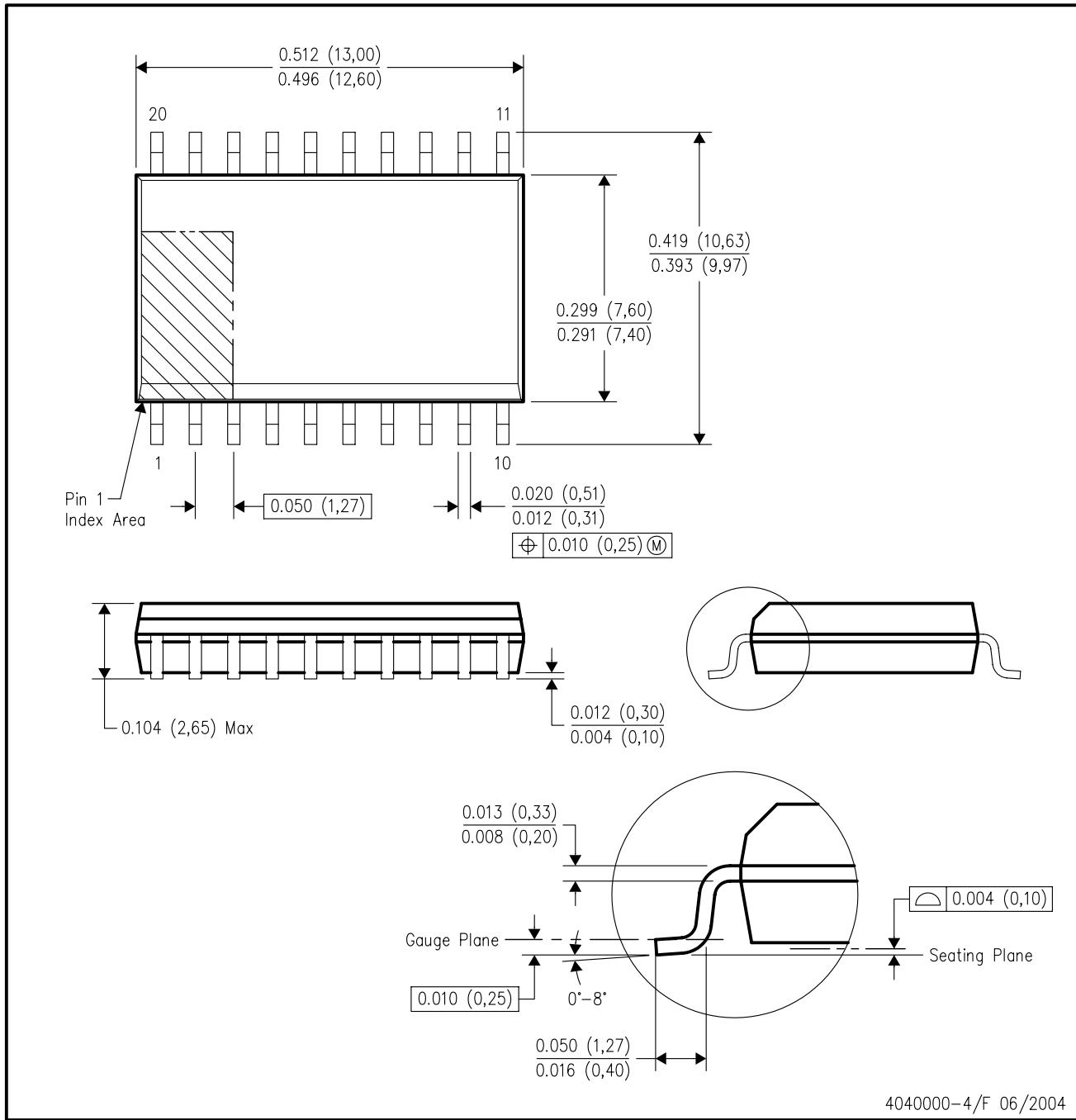
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



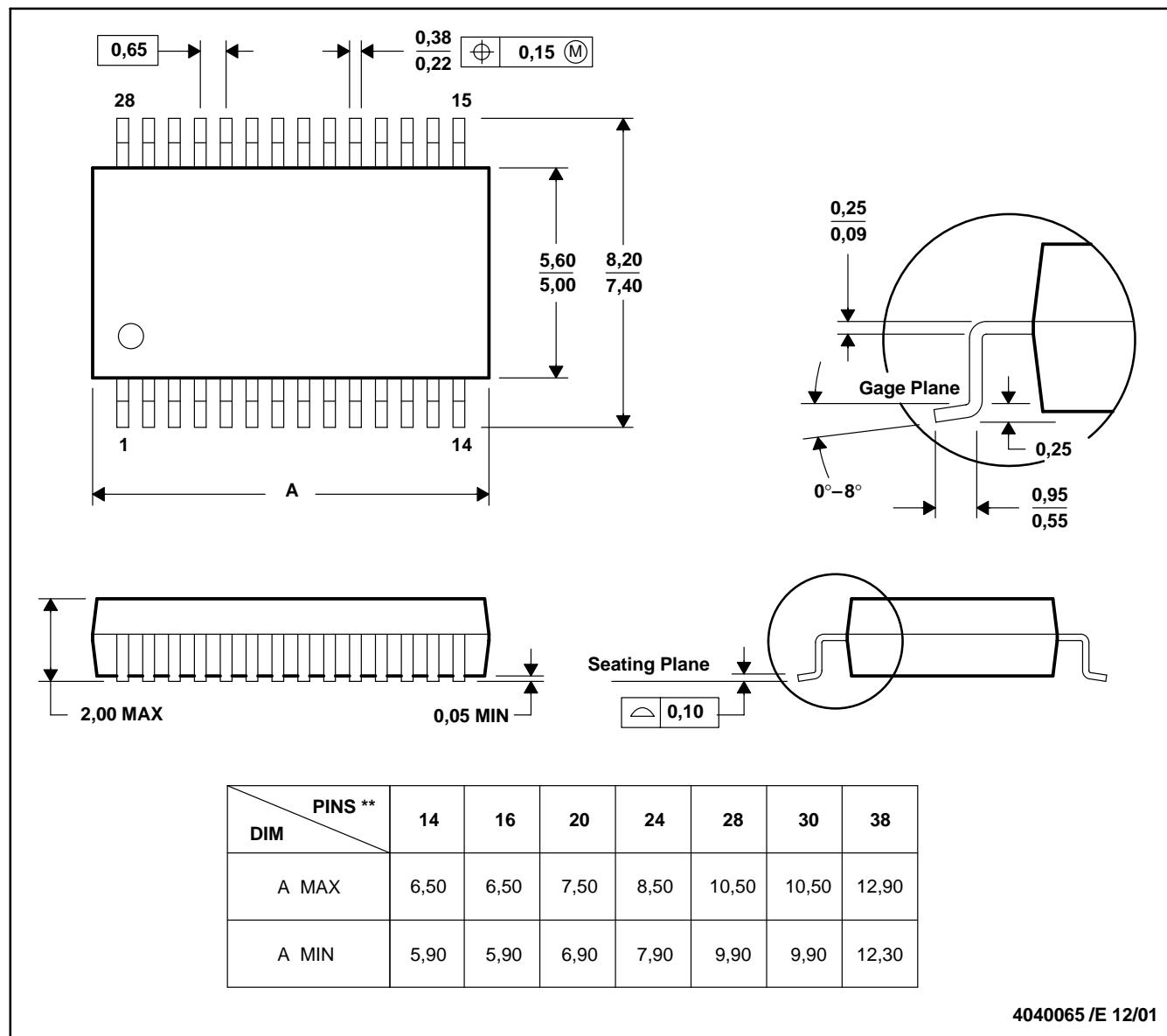
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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