

IRG4BC20UD-S

INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE

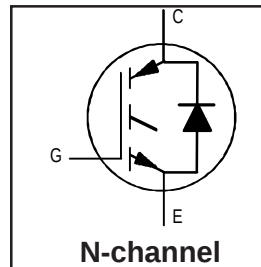
UltraFast CoPack IGBT

Features

- UltraFast: Optimized for high operating frequencies 8-40 kHz in hard switching, >200kHz in resonant mode
- Generation 4 IGBT design provides tighter parameter distribution and higher efficiency than Generation 3
- IGBT co-packaged with HEXFRED™ ultrafast, ultra-soft-recovery anti-parallel diodes for use in bridge configurations
- Industry standard D²Pak package

Benefits

- Generation 4 IGBTs offers highest efficiencies available
- Optimized for specific application conditions
- HEXFRED diodes optimized for performance with IGBTs . Minimized recovery characteristics require less/no snubbing
- Designed to be a "drop-in" replacement for equivalent industry-standard Generation 3 IR IGBTs



$V_{CES} = 600V$
 $V_{CE(on)} \text{ typ.} = 1.85V$
@ $V_{GE} = 15V, I_C = 6.5A$



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	13	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	6.5	
I_{CM}	Pulsed Collector Current ①	52	
I_{LM}	Clamped Inductive Load Current ②	52	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	7.0	
I_{FM}	Diode Maximum Forward Current	52	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	60	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	24	
T_J	Operating Junction and	-55 to +150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	1.44	—	g (oz)

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ^③	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/ $^\circ\text{C}$	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.85	2.1	V	$I_C = 6.5A, V_{GE} = 15V$
		—	2.27	—		$I_C = 13A$
		—	1.87	—		$I_C = 6.5A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/ $^\circ\text{C}$	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ^④	1.4	4.3	—	S	$V_{CE} = 100V, I_C = 6.5A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$
		—	—	1700		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	1.4	1.7	V	$I_C = 8.0A$
		—	1.3	1.6		$I_C = 8.0A, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	27	41	nC	$I_C = 6.5A$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.5	6.8		$V_{CC} = 400V$
Q_{gc}	Gate - Collector Charge (turn-on)	—	10	16		$V_{GE} = 15V$
$t_{d(on)}$	Turn-On Delay Time	—	39	—	ns	$T_J = 25^\circ\text{C}$
t_r	Rise Time	—	15	—		$I_C = 6.5A, V_{CC} = 480V$
$t_{d(off)}$	Turn-Off Delay Time	—	93	140		$V_{GE} = 15V, R_G = 50\Omega$
t_f	Fall Time	—	110	170		Energy losses include "tail" and diode reverse recovery.
E_{on}	Turn-On Switching Loss	—	0.16	—	mJ	See Fig. 9, 10, 11, 18
E_{off}	Turn-Off Switching Loss	—	0.13	—		
E_{ts}	Total Switching Loss	—	0.29	0.3		
$t_{d(on)}$	Turn-On Delay Time	—	38	—	ns	$T_J = 150^\circ\text{C}$, See Fig. 9, 10, 11, 18
t_r	Rise Time	—	17	—		$I_C = 6.5A, V_{CC} = 480V$
$t_{d(off)}$	Turn-Off Delay Time	—	100	—		$V_{GE} = 15V, R_G = 50\Omega$
t_f	Fall Time	—	220	—		Energy losses include "tail" and diode reverse recovery.
E_{ts}	Total Switching Loss	—	0.49	—	mJ	
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	530	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	39	—		$V_{CC} = 30V$
C_{res}	Reverse Transfer Capacitance	—	7.4	—		$f = 1.0MHz$
t_{rr}	Diode Reverse Recovery Time	—	37	55	ns	$T_J = 25^\circ\text{C}$ See Fig. 14
		—	55	90		$T_J = 125^\circ\text{C}$
I_{rr}	Diode Peak Reverse Recovery Current	—	3.5	5.0	A	$T_J = 25^\circ\text{C}$ See Fig. 15
		—	4.5	8.0		$T_J = 125^\circ\text{C}$
Q_{rr}	Diode Reverse Recovery Charge	—	65	138	nC	$T_J = 25^\circ\text{C}$ See Fig. 16
		—	124	360		$T_J = 125^\circ\text{C}$
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	240	—	A/ μs	$T_J = 25^\circ\text{C}$ See Fig. 17
		—	210	—		$T_J = 125^\circ\text{C}$

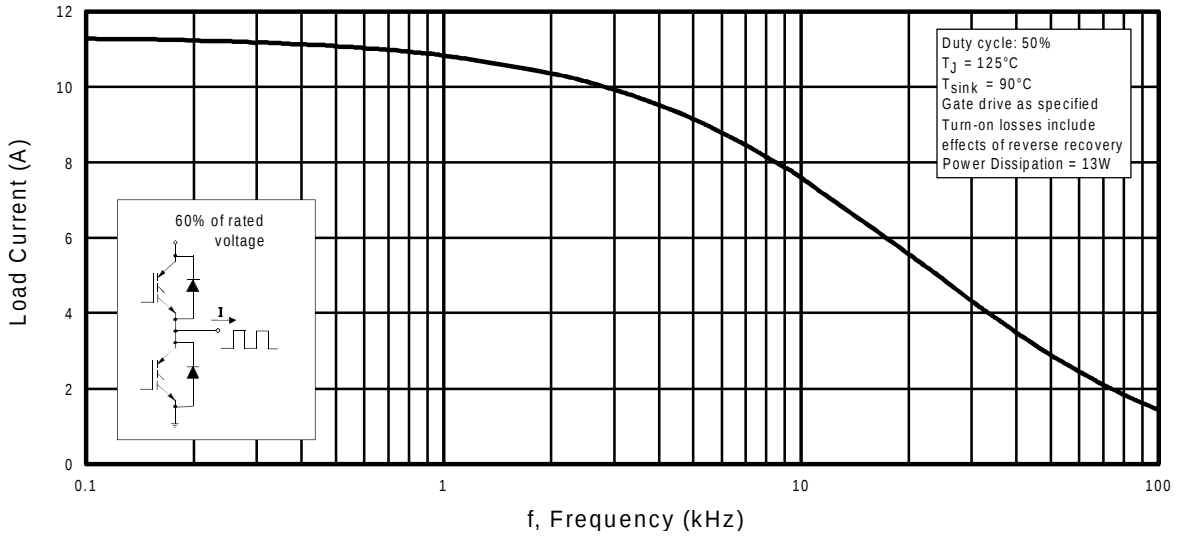


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

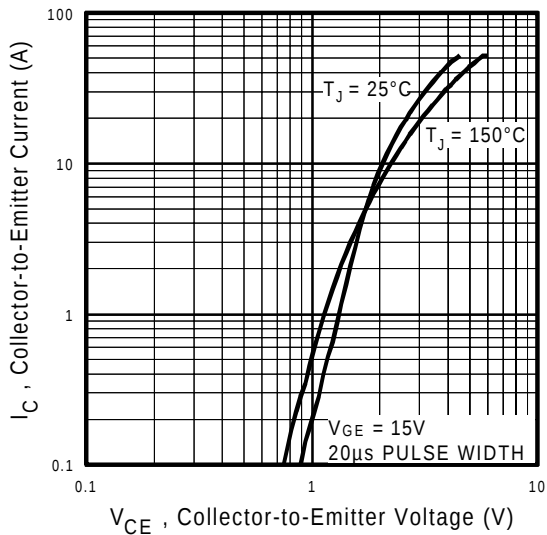


Fig. 2 - Typical Output Characteristics

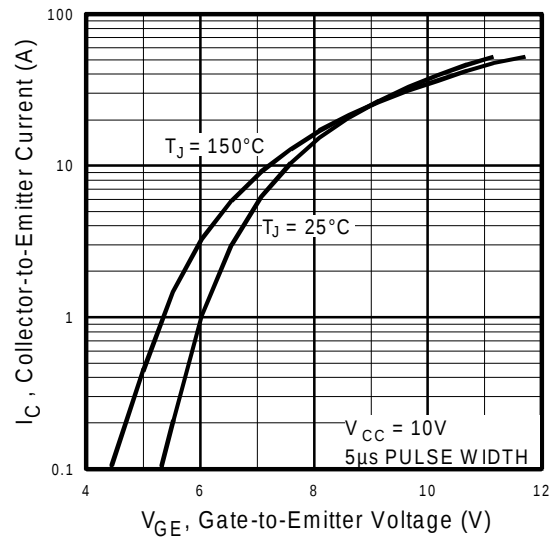


Fig. 3 - Typical Transfer Characteristics

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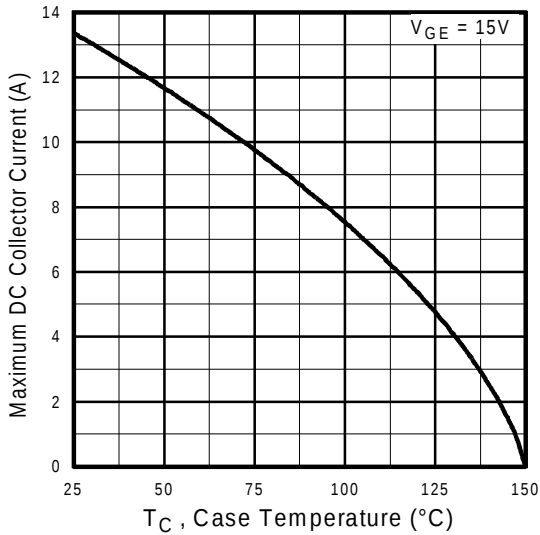


Fig. 4 - Maximum Collector Current vs. Case Temperature

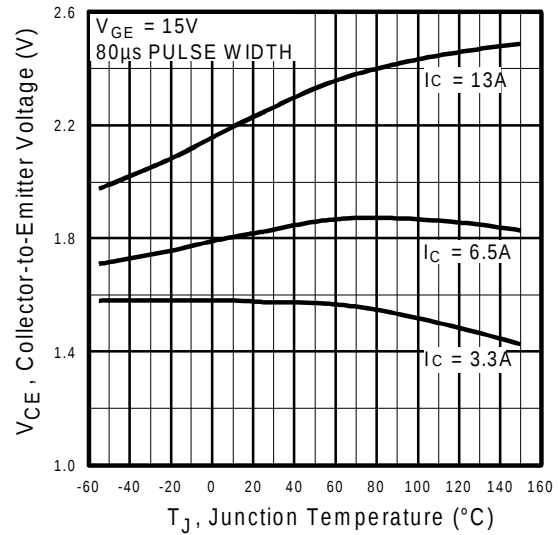


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

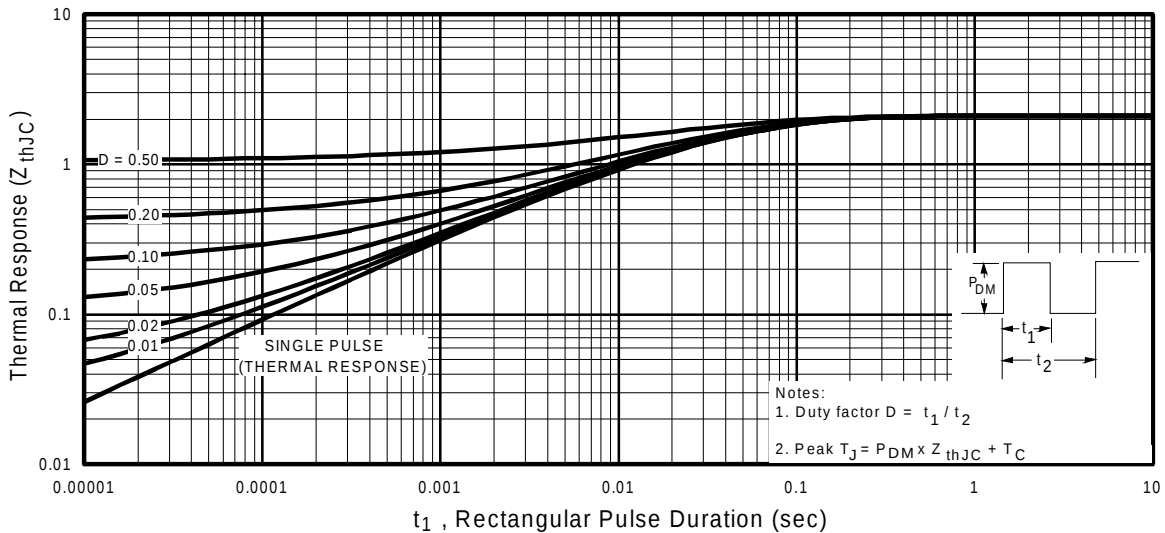


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction-to-Case

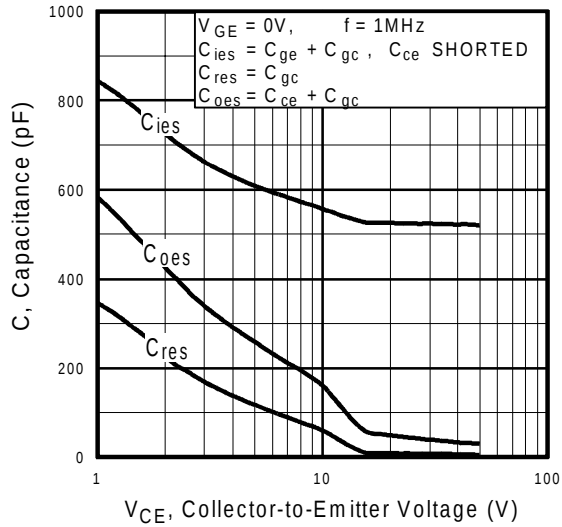


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

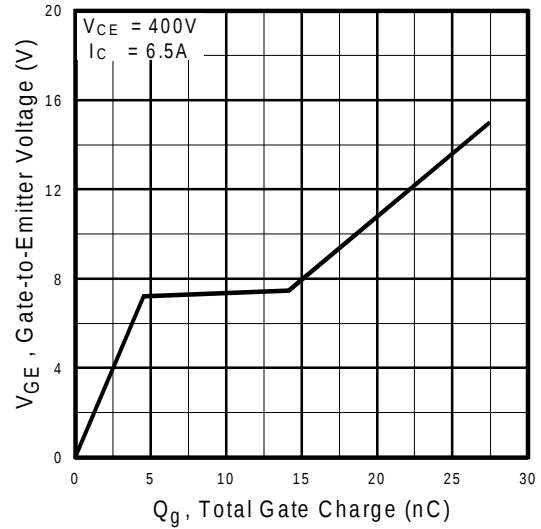


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

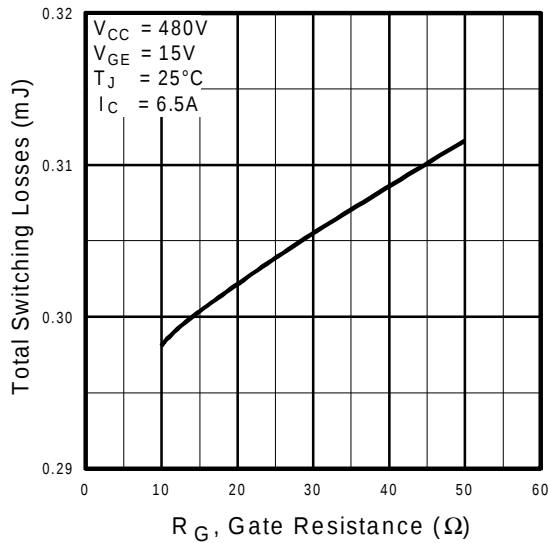


Fig. 9 - Typical Switching Losses vs. Gate Resistance

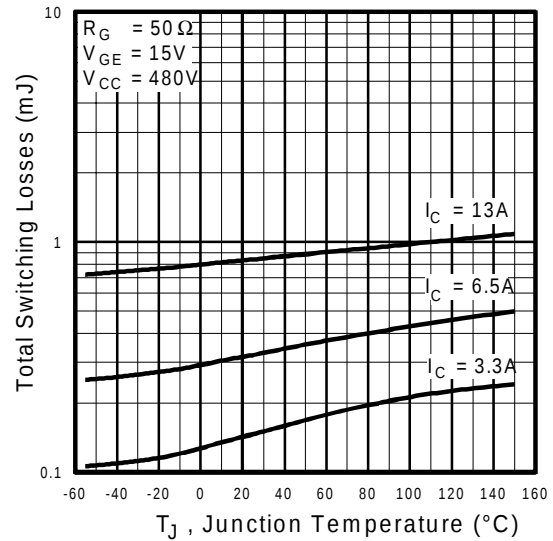
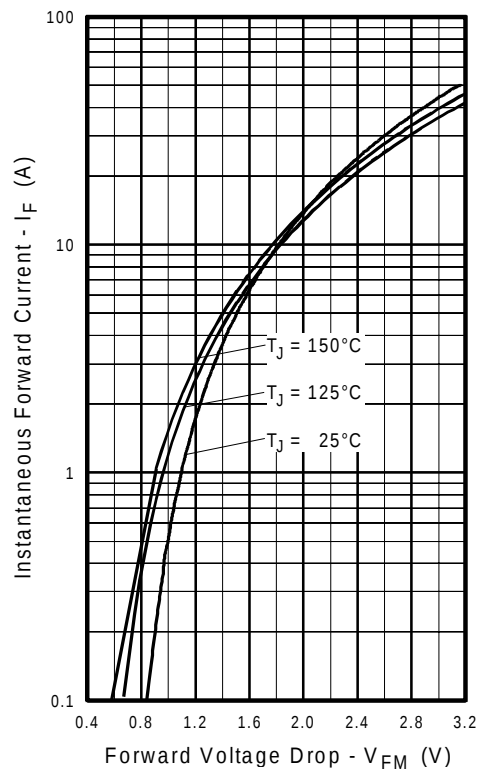
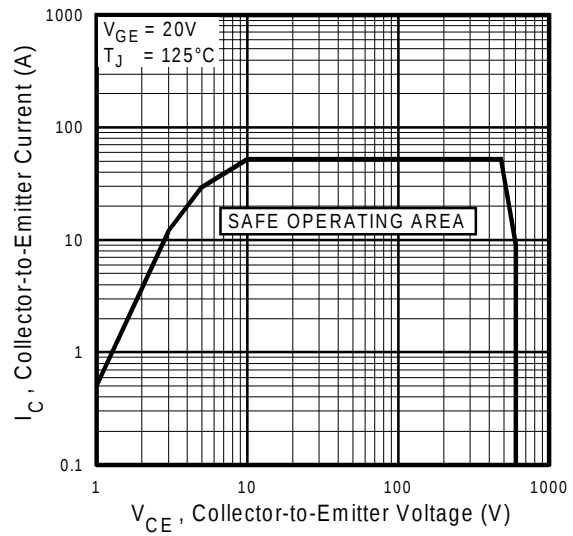
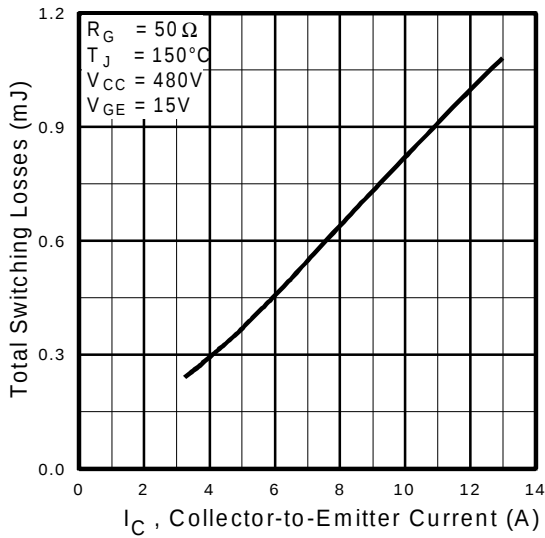


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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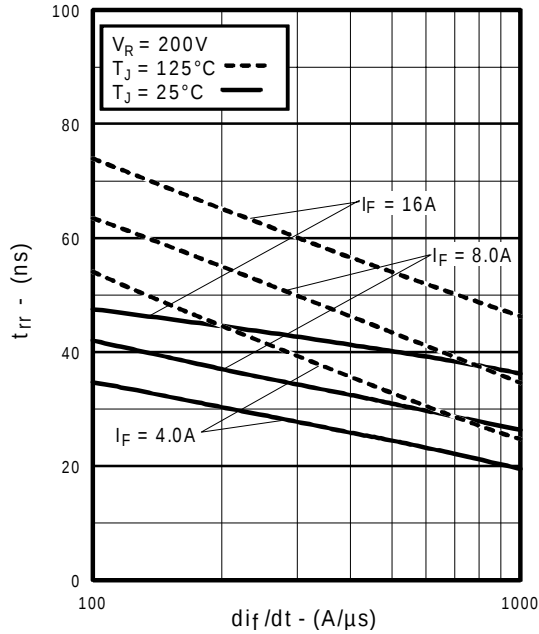


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

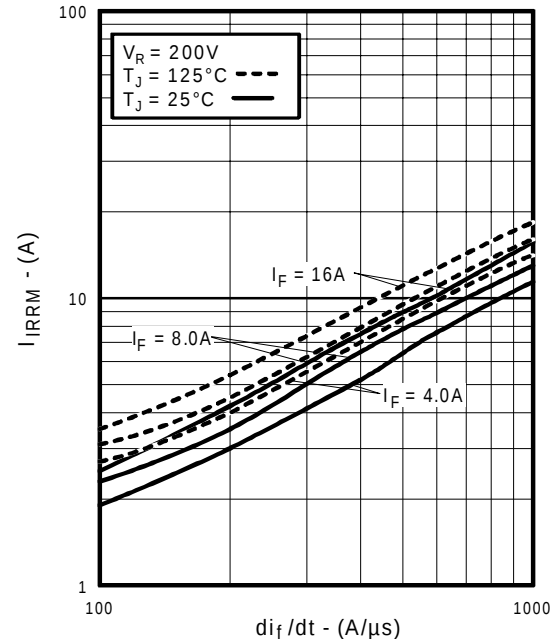


Fig. 15 - Typical Recovery Current vs. di_f/dt

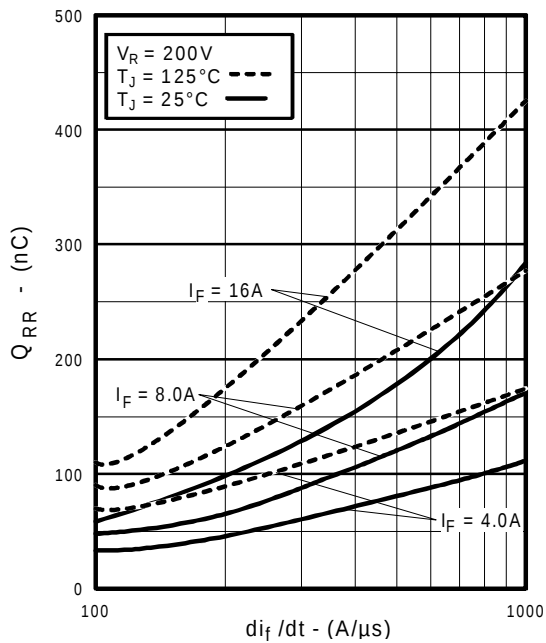


Fig. 16 - Typical Stored Charge vs. di_f/dt

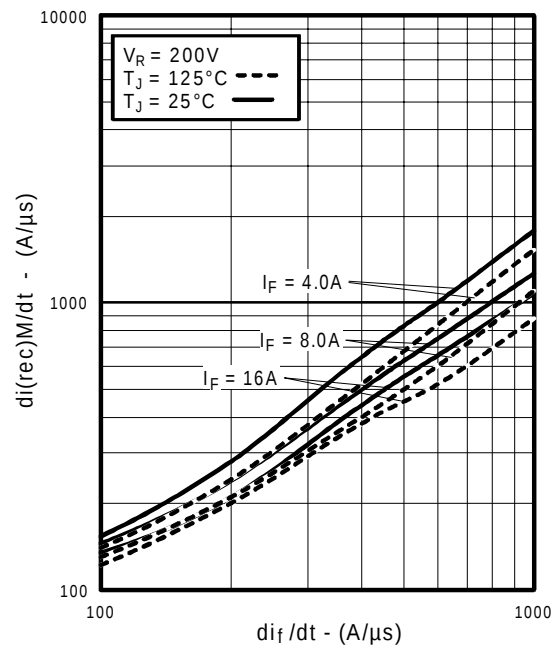


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt

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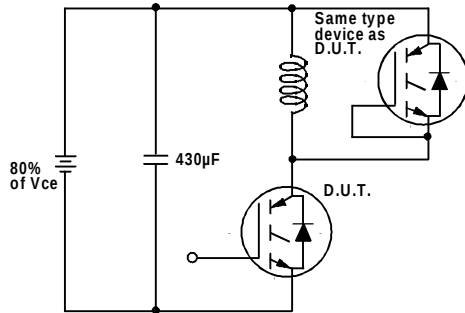


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

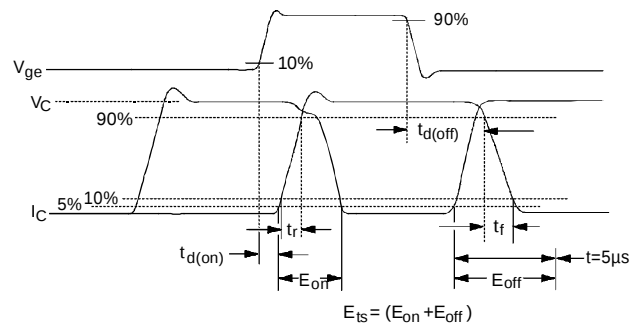


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

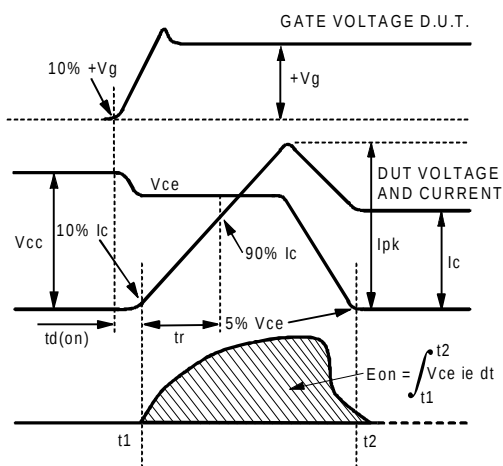


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

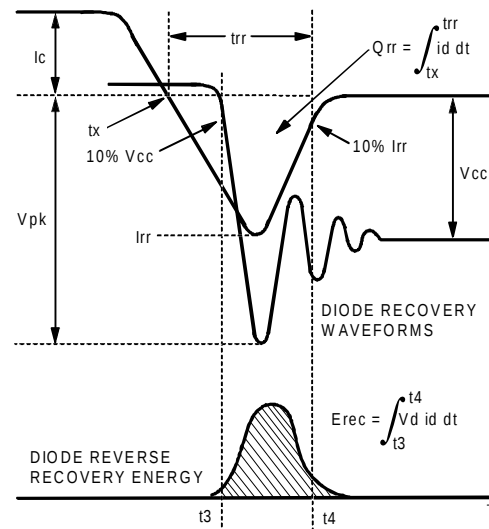


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

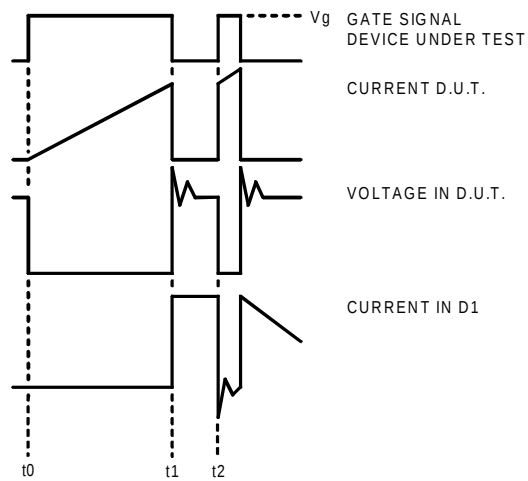


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

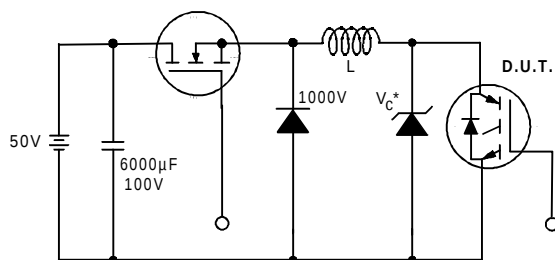


Figure 19. Clamped Inductive Load Test Circuit

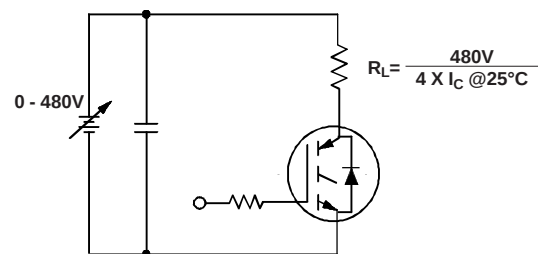
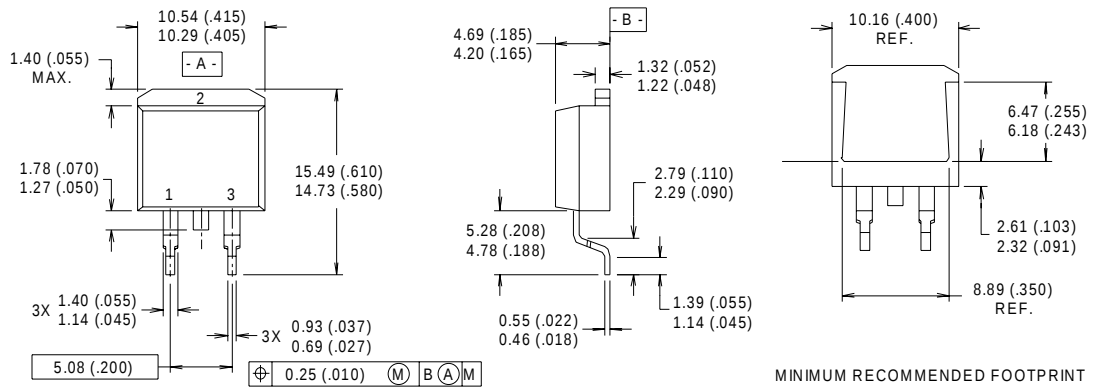


Figure 20. Pulsed Collector Current Test Circuit

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D²Pak Package Outline



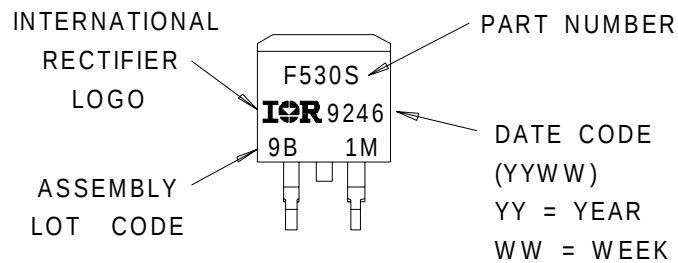
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

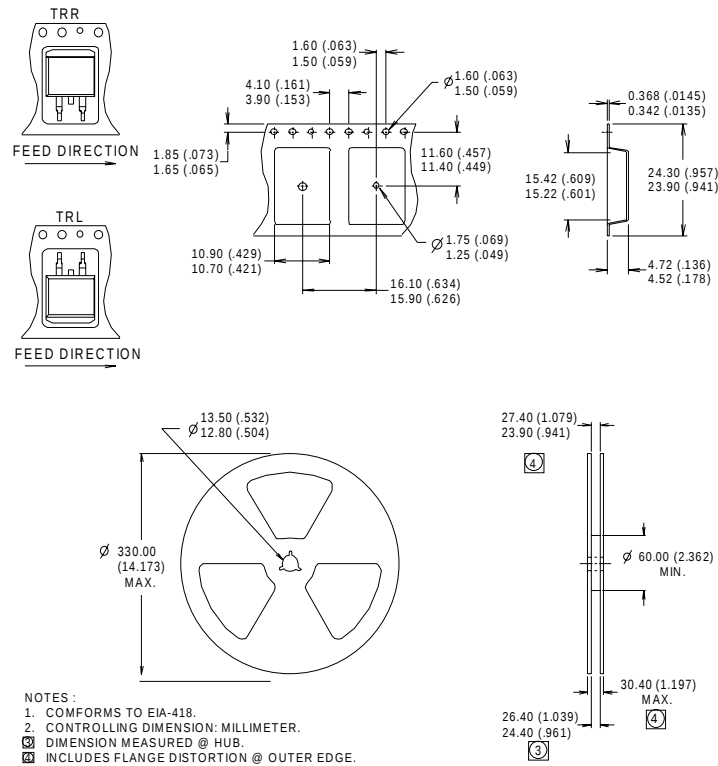
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

D²Pak Part Marking Information



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating: $V_{GE}=20V$; pulse width limited by maximum junction temperature (Figure 20)
- ② $V_{CC}=80\%(V_{CES})$, $V_{GE}=20V$, $L=10\mu H$, $R_G = 50\Omega$ (Figure 19)
- ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ④ Pulse width $5.0\mu s$, single shot.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Visit us at www.irf.com for sales contact information.1/01

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>