

To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors.

Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.

Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

Switching Regulator for Chopper Type DC/DC Converter



ADE-204-020A (Z)

Rev.1
Dec. 2000

Description

The HA16114P/FP/FPJ and HA16120FP/FPJ are single-channel PWM switching regulator controller ICs suitable for chopper-type DC/DC converters. Integrated totem-pole output circuits enable these ICs to drive the gate of a power MOSFET directly. The output logic of the HA16120 is designed to control a DC/DC step-up (boost) converter using an N-channel power MOS FET. The output logic of the HA16114 is designed to control a DC/DC step-down (buck) converter or inverting converter using a P-channel power MOS FET.

These ICs can operate synchronously with external pulse, a feature that makes them ideal for power supplies that use a primary-control AC/DC converter to convert commercial AC power to DC, then use one or more DC/DC converters on the secondary side to obtain multiple DC outputs. Synchronization is with the falling edge of the 'sync' pulse, which can be the secondary output pulse from a flyback transformer. Synchronization eliminates the beat interference that can arise from different operating frequencies of the AC/DC and DC/DC converters, and reduces harmonic noise. Synchronization with an AC/DC converter using a forward transformer is also possible, by inverting the 'sync' pulse.

Overcurrent protection features include a pulse-by-pulse current limiter that can reduce the width of individual PWM pulses, and an intermittent operating mode controlled by an on-off timer. Unlike the conventional latched shutdown function, the intermittent operating function turns the IC on and off at controlled intervals when pulse-by-pulse current limiting continues for a programmable time. This results in sharp vertical settling characteristics. Output recovers automatically when the overcurrent condition subsides.

Using these ICs, a compact, highly efficient DC/DC converter can be designed easily, with a reduced number of external components.

Functions

- 2.5 V voltage reference
- Sawtooth oscillator (Triangle wave)
- Overcurrent detection
- External synchronous input
- Totem-pole output

HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

- Undervoltage lockout (UVL)
- Error amplifier
- Vref overvoltage protection (OVP)

Features

- Wide supply voltage range: 3.9 V to 40 V*
- Maximum operating frequency: 600 kHz
- Able to drive a power MOS FET (± 1 A maximum peak current) by the built-in totem-pole gate pre-driver circuit
- Can operate in synchronization with an external pulse signal, or with another controller IC
- Pulse-by-pulse overcurrent limiting (OCL)
- Intermittent operation under continuous overcurrent
- Low quiescent current drain when shut off by grounding the ON/OFF pin
HA16114: $I_{OFF} = 10 \mu A$ (max)
HA16120: $I_{OFF} = 150 \mu A$ (max)
- Externally trimmable reference voltage (Vref): ± 0.2 V
- Externally adjustable undervoltage lockout points (with respect to V_{IN})
- Stable oscillator frequency
- Soft start and quick shut function

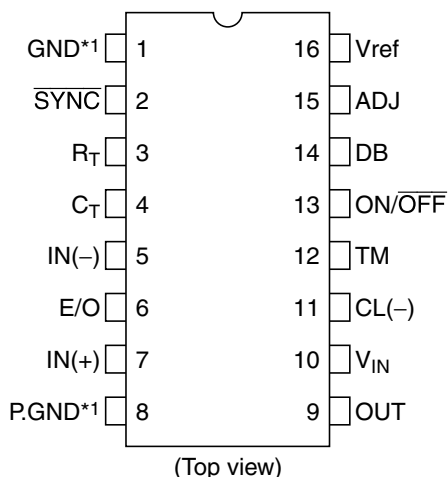
Note: The reference voltage 2.5 V is under the condition of $V_{IN} \geq 4.5$ V.

Ordering Information

Hitachi Control ICs for Chopper-Type DC/DC Converters

Channels	Product	Channel	Control Functions			Output Circuits	Overcurrent
	Number	No.	Step-Up	Step-Down	Inverting		Protection
Dual	HA17451	Ch 1				Open collector	SCP with timer (latch)
		Ch 2					
Single	HA16114	—	—			Totem pole power MOS FET driver	Pulse-by-pulse current limiter and intermittent operation by on/off timer
	HA16120	—		—	—		
Dual	HA16116	Ch 1	—				
		Ch 2	—		—		
	HA16121	Ch 1	—				
		Ch 2		—	—		

Pin Arrangement

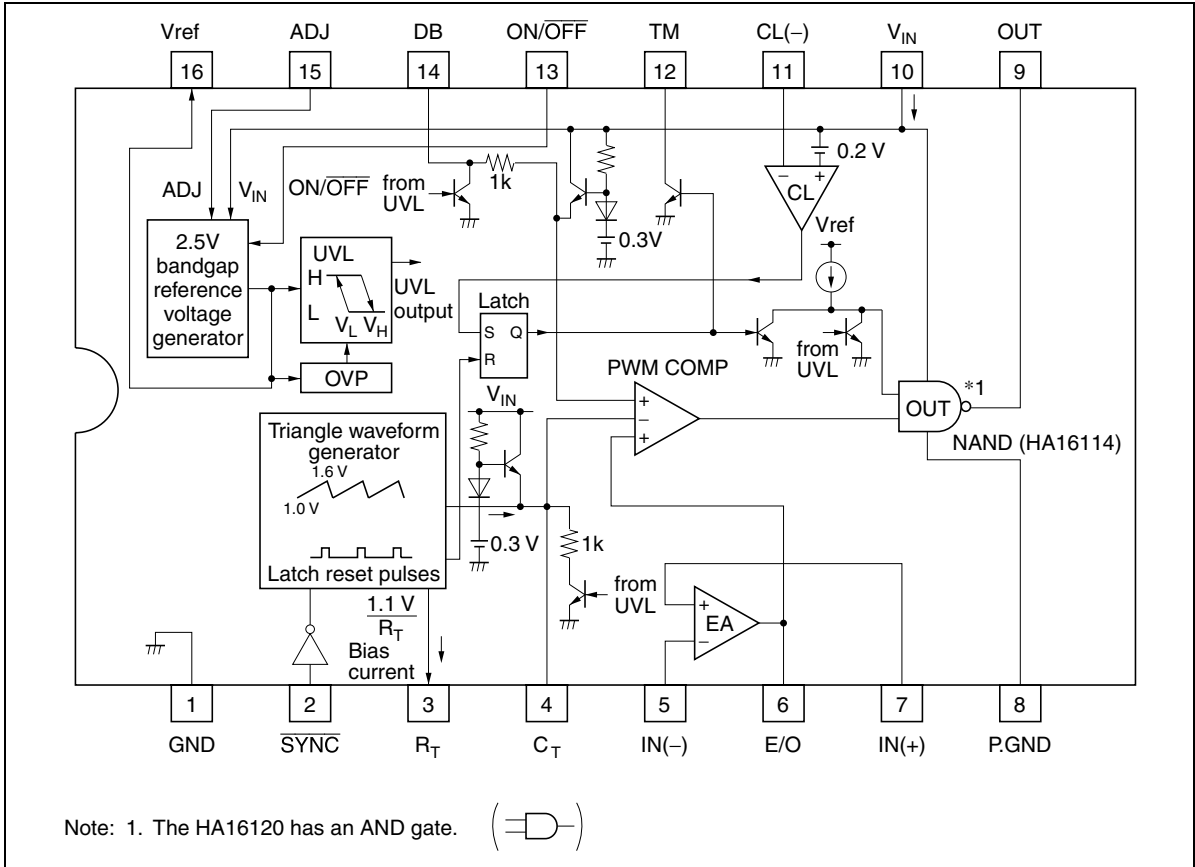


Note: 1. Pin 1 (GND) and Pin 8 (P.GND) must be connected each other with external wire.

Pin Description

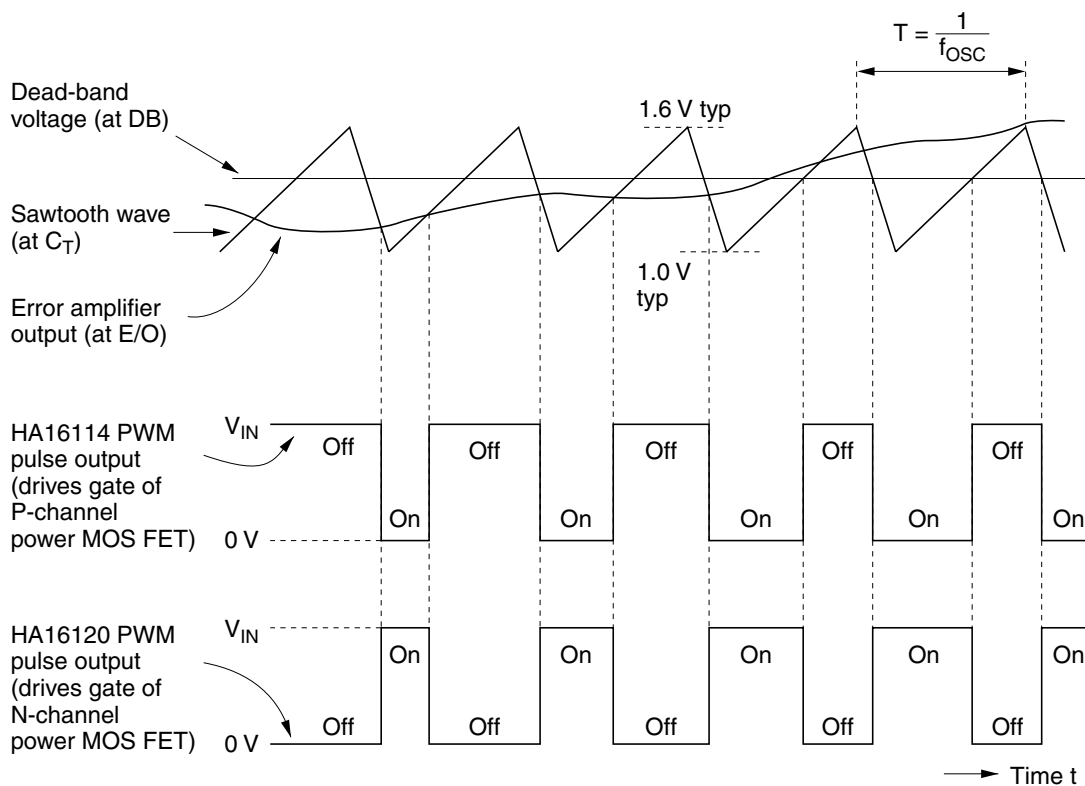
Pin No.	Symbol	Function
1	GND	Signal ground
2	$\overline{\text{SYNC}}$	External sync signal input (synchronized with falling edge)
3	R_T	Oscillator timing resistor connection (bias current control)
4	C_T	Oscillator timing capacitor connection (sawtooth voltage output)
5	IN(-)	Inverting input to error amplifier
6	E/O	Error amplifier output
7	IN(+)	Non-inverting input to error amplifier
8	P.GND	Power ground
9	OUT	Output (pulse output to gate of power MOS FET)
10	V_{IN}	Power supply input
11	CL(-)	Inverting input to current limiter
12	TM	Timer setting for intermittent shutdown when overcurrent is detected (sinks timer transistor current)
13	$\overline{\text{ON/OFF}}$	IC on/off control (off below approximately 0.7 V)
14	DB	Dead-band duty cycle control input
15	ADJ	Reference voltage (Vref) adjustment input
16	Vref	2.5 V reference voltage output

Block Diagram



Timing Waveforms

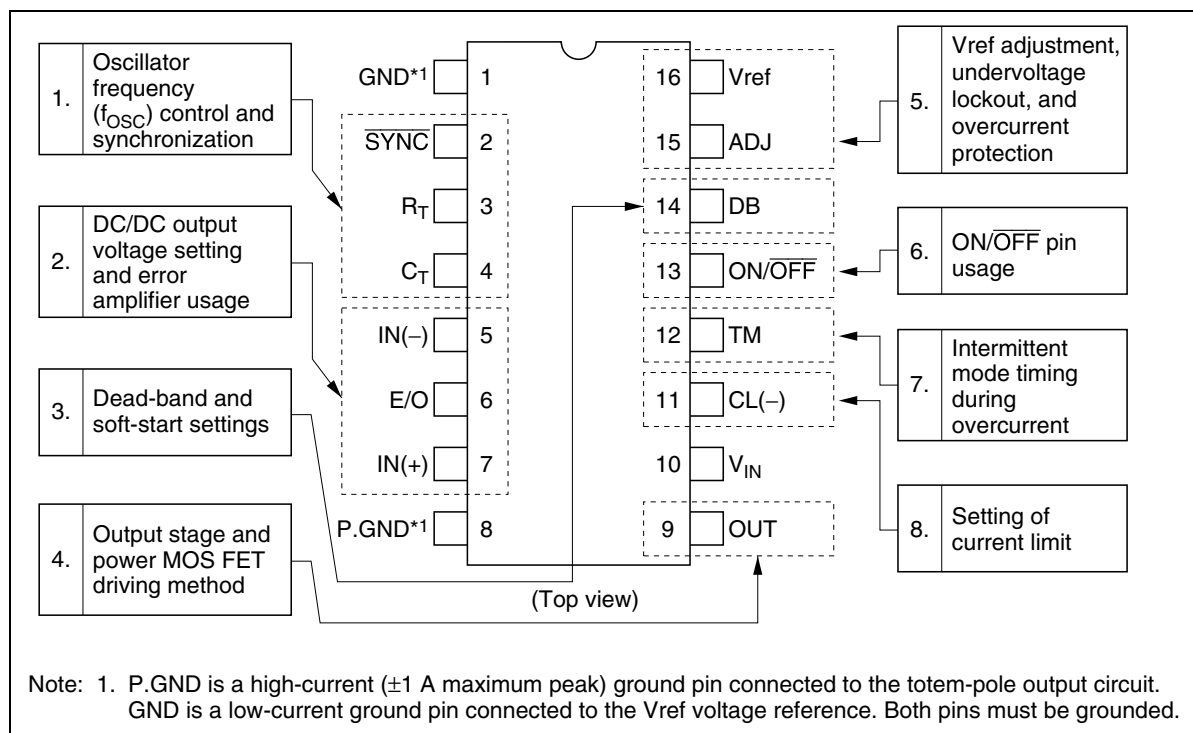
Generation of PWM pulse output from sawtooth wave (during steady-state operation)



Note: On duty = $\frac{t_{ON}}{T}$

Guide to the Functional Description

The description covers the topics indicated below.



1. Sawtooth Oscillator (Triangle Wave)

1.1 Operation and Frequency Control

The sawtooth wave is a voltage waveform from which the PWM pulses are created (See figure 1). The sawtooth oscillator operates as follows. A constant current I_o determined by an external timing resistor R_T is fed continuously to an external timing capacitor C_T . When the C_T pin voltage exceeds a comparator threshold voltage V_{TH} , the comparator output opens a switching transistor, allowing a $3I_o$ discharge current to flow from C_T . When the C_T pin voltage drops below a threshold voltage V_{TL} , the comparator output closes the switching transistor, stopping the $3I_o$ discharge. Repetition of these operations generates a sawtooth wave.

The value of I_o is $1.1 \text{ V}/R_T \text{ } \Omega$. The I_o current mirror has a limited current capacity, so R_T should be at least $5 \text{ k}\Omega$ ($I_o \leq 220 \text{ } \mu\text{A}$).

Internal resistances R_A , R_B , and R_C set the peak and valley voltages V_{TH} and V_{TL} of the sawtooth waveform at approximately 1.6 V and 1.0 V .

The oscillator frequency f_{osc} can be calculated as follows.

$$f_{osc} = \frac{1}{t_1 + t_2 + t_3}$$

$$\text{Here, } t_1 = \frac{C_T \times (V_H - V_L)}{1.1 \text{ V}/R_T}$$

$$t_2 = \frac{C_T \times (V_H - V_L)}{3 \times 1.1 \text{ V}/R_T}$$

$$t_3 \approx 0.8 \mu\text{s} \text{ (comparator delay time)}$$

$$\text{Since } V_H - V_L = 0.6 \text{ V}$$

$$f_{osc} \approx \frac{1}{0.73 \times C_T \times R_T + 0.8 (\mu\text{s})} \text{ (Hz)}$$

At high frequencies the comparator delay causes the sawtooth wave to overshoot the 1.6 V threshold and undershoot the 1.0 V threshold, and changes the dead-band thresholds accordingly. Select constants by testing under implementation conditions.

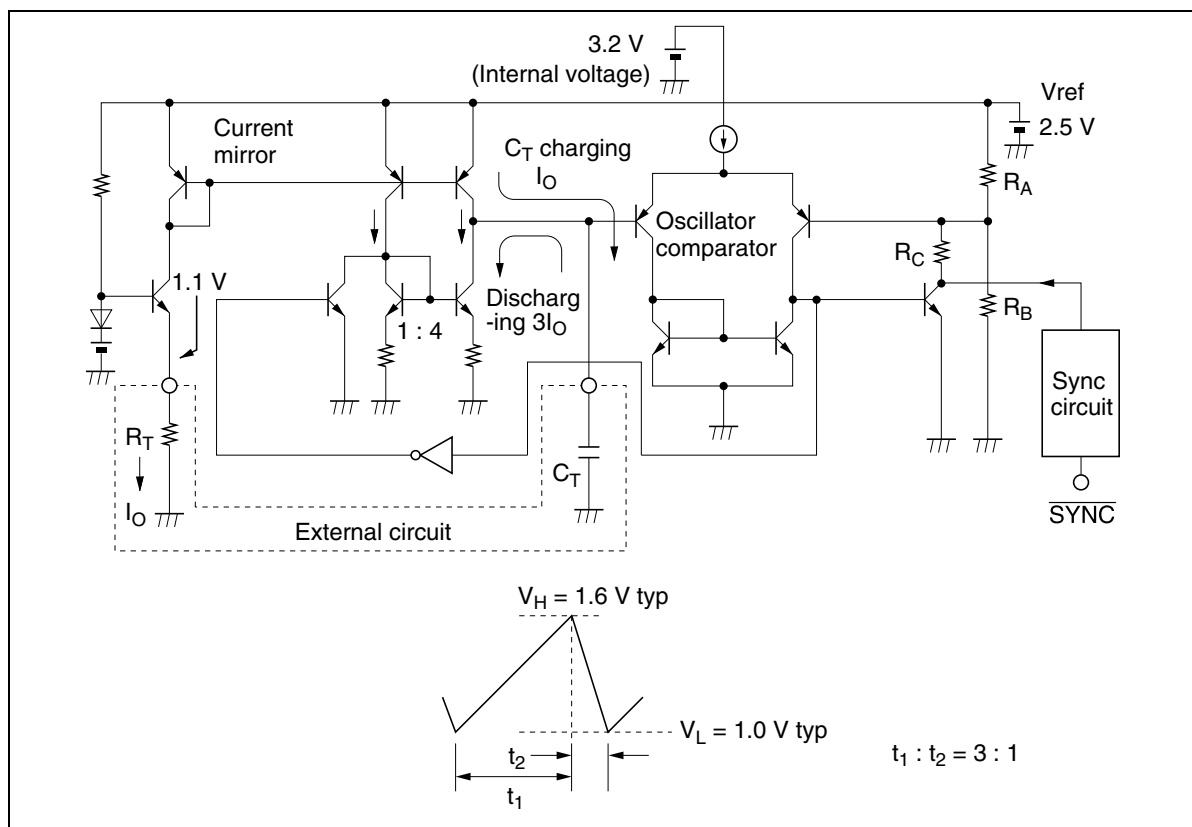


Figure 1.1 Equivalent Circuit of Oscillator

1.2 External Synchronization

These ICs have a sync input pin so that they can be synchronized to a primary-control AC/DC converter. Pulses from the secondary winding of the switching transformer should be dropped through a resistor voltage divider to the sync input pin. Synchronization takes place at the falling edge, which is optimal for multiple-output power supplies that synchronize with a flyback AC/DC converter.

The sync input pin ($\overline{\text{SYNC}}$) is connected internally through a synchronizing circuit to the sawtooth oscillator to synchronize the sawtooth waveform (see figure 1.2).

- Synchronization is with the falling edge of the external sync signal.
- The frequency of the external sync signal must be in the range $f_{\text{osc}} < f_{\overline{\text{SYNC}}} < f_{\text{osc}} \times 2$.
- The duty cycle of the external sync signal must be in the range $5\% < t_1/t_2 < 50\%$ ($t_1 = 300 \text{ ns Min}$).
- With external synchronization, V_{TH}' can be calculated as follows.

$$V_{\text{TH}}' = (V_{\text{TH}} - V_{\text{TL}}) \times \frac{f_{\text{OSC}}}{f_{\overline{\text{SYNC}}}} + V_{\text{TL}}$$

Note: When not using external synchronization, connect the $\overline{\text{SYNC}}$ pin to the Vref pin.

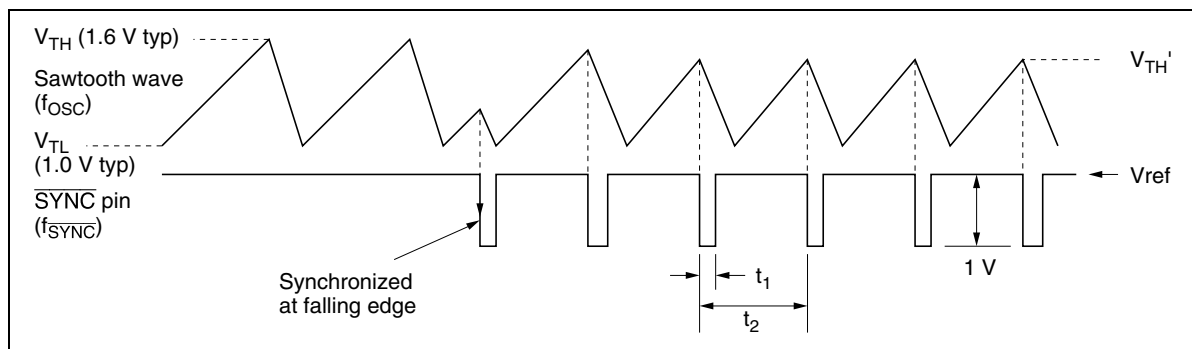


Figure 1.2 External Synchronization

2. DC/DC Output Voltage Setting and Error Amplifier Usage

2.1 DC/DC Output Voltage Setting

1. Positive Output Voltage ($V_o > V_{ref}$)

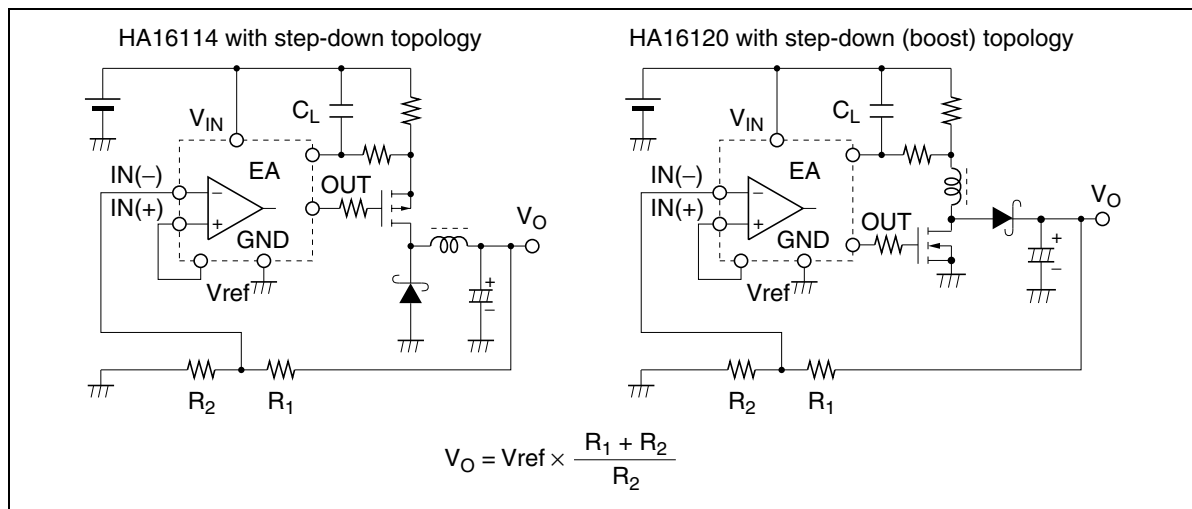


Figure 2.1 Output Voltage Setting (1)

2. Negative Output Voltage ($V_o < 0$ V)

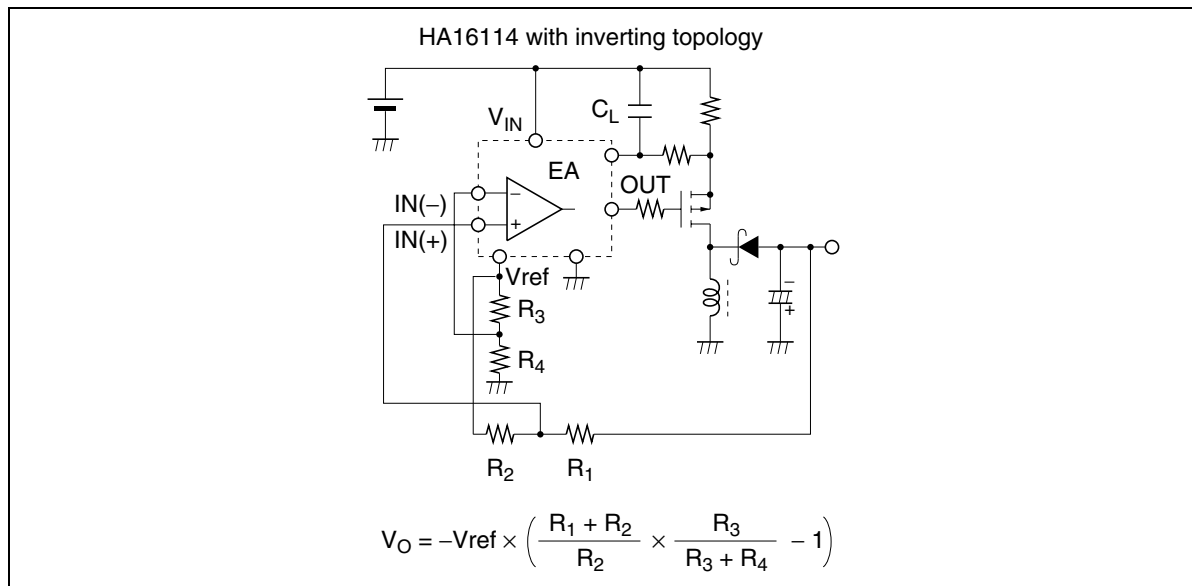


Figure 2.2 Output Voltage Setting (2)

2.2 Error Amplifier Usage

Figure 2.3 shows an equivalent circuit of the error amplifier. The error amplifier in these ICs is a simple NPN-transistor differential amplifier with a constant-current-driven output circuit.

The amplifier combines a wide bandwidth ($f_T = 4$ MHz) with a low open-loop gain (50 dB Typ), allowing stable feedback to be applied when the power supply is designed. Phase compensation is also easy.

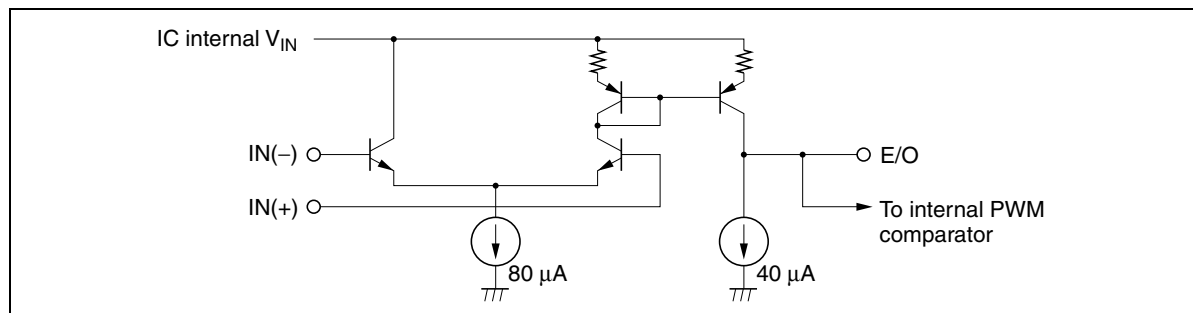


Figure 2.3 Error Amplifier Equivalent Circuit

3. Dead-Band Duty Cycle and Soft-Start Settings

3.1 Dead-Band Duty Cycle Setting

The dead-band duty cycle (the maximum duty cycle of the PWM pulse output) can be programmed by the voltage V_{DB} at the DB pin. A convenient way to obtain V_{DB} is to divide the IC's Vref output by two external resistors. The dead-band duty cycle (DB) and V_{DB} can be calculated as follows.

$$DB = \frac{V_{TH} - V_{DB}}{V_{TH} - V_{TL}} \times 100 (\%) \quad \dots \text{This applies when } V_{DB} > V_{TL}.$$

If $V_{DB} < V_{TL}$, there is no PWM output.

$$V_{DB} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

Note: V_{DB} is the voltage at the DB pin.

V_{TH} : 1.6 V (Typ)

V_{TL} : 1.0 V (Typ)

Vref is typically 2.5 V. Select R_1 and R_2 so that $1.0 \text{ V} \leq V_{DB} \leq 1.6 \text{ V}$.

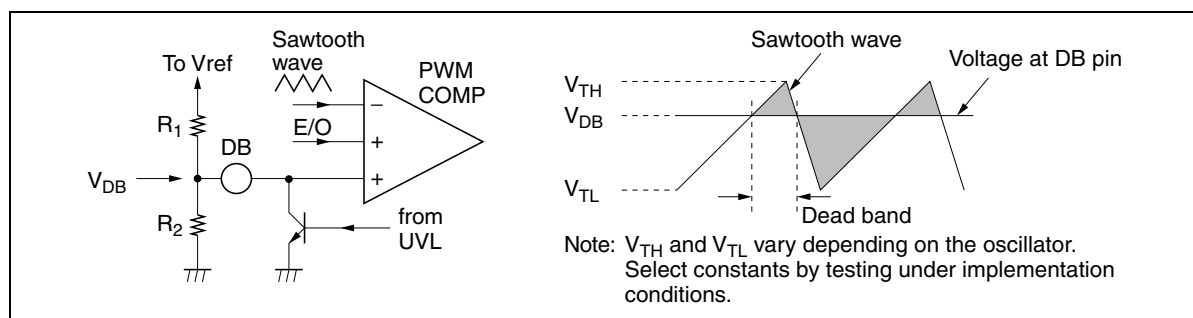


Figure 3.1 Dead-Band Duty Cycle Setting

3.2 Soft-Start Setting

Soft-start avoids overshoot at power-up by widening the PWM output pulses gradually, so that the converted DC output rises slowly. Soft-start is programmed by connecting a capacitor between the DB pin and ground. The soft-start time is determined by the time constant of this capacitor and the resistors that set the voltage at the DB pin.

$$t_{\text{soft}} = -C_1 \times R \times \ln \left(1 - \frac{V_X}{V_{\text{DB}}} \right)$$

$$R = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{\text{DB}} = V_{\text{ref}} \times \frac{R_2}{R_1 + R_2}$$

Note: V_X is the voltage at the DB pin after time t ($V_X < V_{\text{DB}}$).

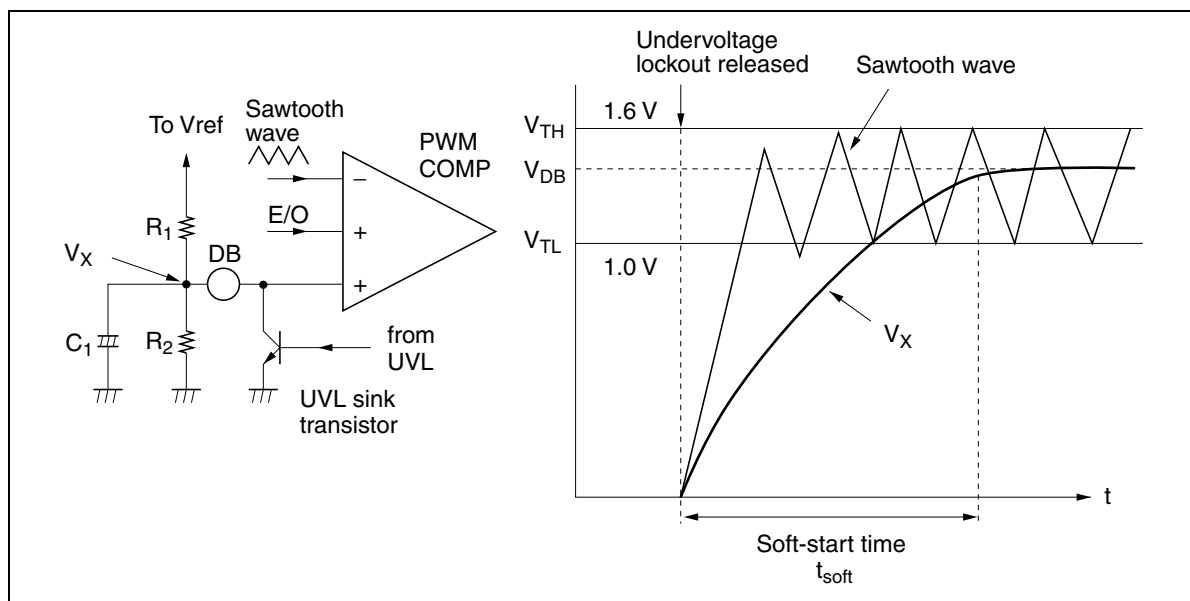


Figure 3.2 Soft-Start Setting

3.3 Quick Shutdown

The quick shutdown function resets the voltages at all pins when the IC is turned off, to assure that PWM pulse output stops quickly. Since the UVL pull-down resistor in the IC remains on even when the IC is turned off, the sawtooth wave output, error amplifier output, and DB pin are all reset to low voltage.

This feature helps in particular to discharge capacitor C_1 in figure 3.2, which has a comparatively large capacitance. In intermittent mode (explained on a separate page), this feature enables the IC to soft-start in each on-off cycle.

4. PWM Output Circuit and Power MOSFET Driving Method

These ICs have built-in totem-pole push-pull drive circuits that can drive a power MOS FET as shown in figure 4.1. The power MOS FET can be driven directly through a gate protection resistor.

If V_{IN} exceeds the gate breakdown voltage of the power MOS FET additional protective measures should be taken, e.g. by adding Zener diodes as shown in figure 4.2.

To drive a bipolar power transistor, the base should be protected by voltage and current dividing resistors as shown in figure 4.3.

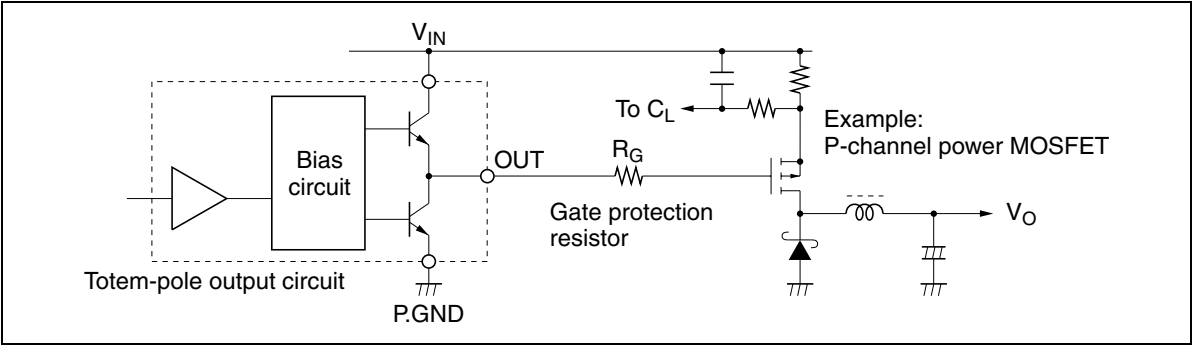


Figure 4.1 Connection of Output Stage to Power MOS FET

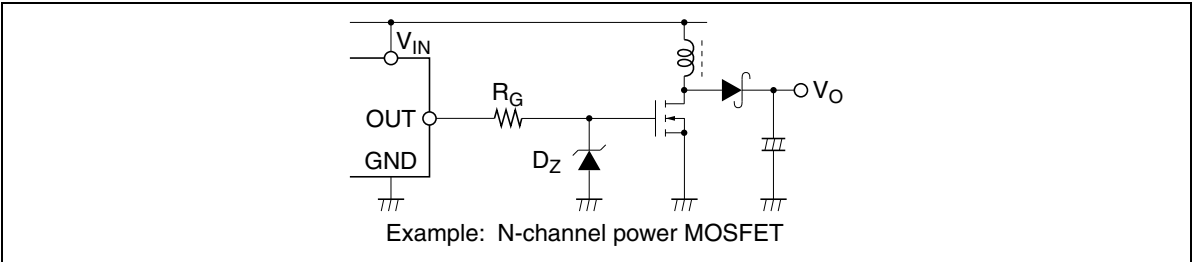


Figure 4.2 Gate Protection by Zener Diodes

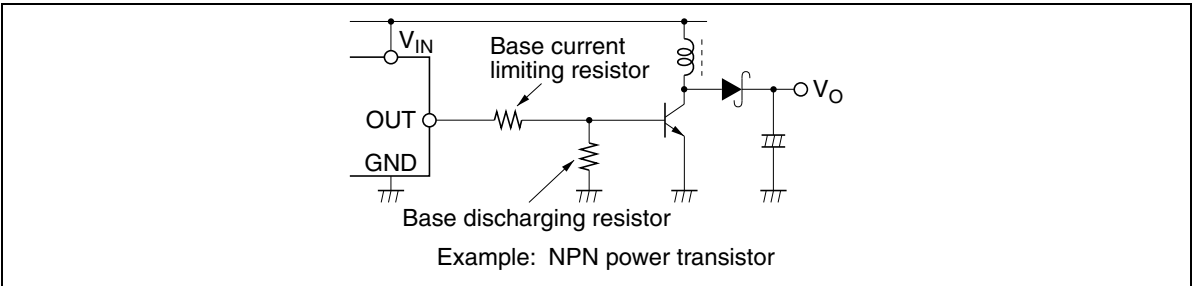


Figure 4.3 Driving a Bipolar Power Transistor

5. Voltage Reference (Vref = 2.5 V)

5.1 Voltage Reference

A bandgap reference built into the IC (see figure 5.1) outputs 2.5 V $\pm$ 50 mV. The sawtooth oscillator, PWM comparator, latch, and other internal circuits are powered by this 2.5 V and an internally-generated voltage of approximately 3.2 V.

The voltage reference section shut downs when the IC is turned off at the ON/OFF pin as described later, saving current when the IC is not used and when it operates in intermittent mode during overcurrent.

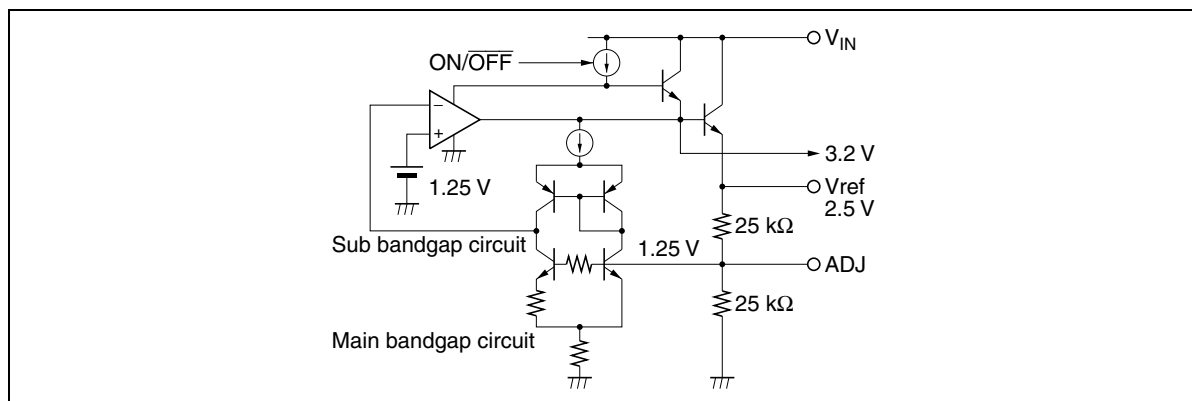


Figure 5.1 Vref Reference Circuit

5.2 Trimming the Reference Voltage (Vref and ADJ pins)

Figure 5.2 shows a simplified circuit equivalent to figure 5.1. The ADJ pin in this circuit is provided for trimming the reference voltage (Vref). The output at the ADJ pin is a voltage V_{ADJ} of 1.25 V (Typ) generated by the bandgap circuit. Vref is determined by V_{ADJ} and the ratio of internal resistors R_1 and R_2 as follows:

$$V_{ref} = V_{ADJ} \times \frac{R_1 + R_2}{R_2}$$

The design values of R_1 and R_2 are 25 k Ω with a tolerance of $\pm 25\%$.

If trimming is not performed, the ADJ pin open can be left open.

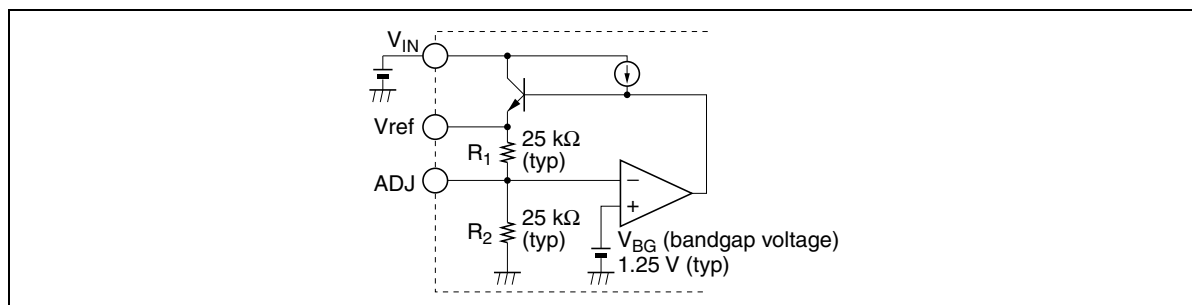


Figure 5.2 Simplified Diagram of Voltage Reference Circuit

The relation between Vref and the ADJ pin enables Vref to be trimmed by inserting one external resistor (R₃) between the Vref and ADJ pins and another (R₄) between the ADJ pin and ground, to change the resistance ratio. Vref is then determined by the combined resistance ratio of the internal R₁ and R₂ and external R₃ and R₄.

$$V_{ref} = V_{ADJ} \times \frac{R_A + R_B}{R_B}$$

Where, R_A: parallel resistance of R₁ and R₃

R_B: parallel resistance of R₂ and R₄

Although Vref can be trimmed by R₃ or R₄ alone, to decrease the temperature dependence of Vref it is better to use two resistors having identical temperature coefficients. Vref can be trimmed in the range of 2.5 V ± 0.2 V. Outside this range, the bandgap circuit will not operate and the IC may shut down.

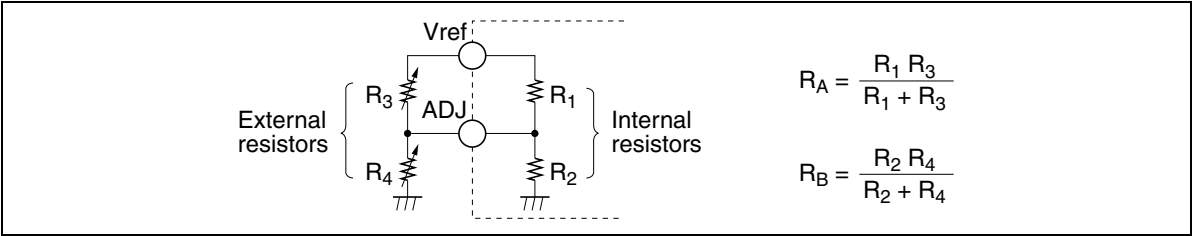


Figure 5.3 Trimming of Reference Voltage

5.3 Vref Undervoltage Lockout and Overvoltage Protection

The undervoltage lockout (UVL) function turns off PWM pulse output when the input voltage (V_{IN}) is low. In these ICs, this is done by monitoring the Vref voltage, which normally stays constant at approximately 2.5 V. The UVL circuit operates with hysteresis: it shuts PWM output off when Vref falls below 1.7 V, and turns PWM output back on when Vref rises above 2.0 V. Undervoltage lockout also provides protection in the event that Vref is shorted to ground.

The overvoltage protection circuit shuts PWM output off when Vref goes above 6.8 V. This provides protection in case the Vref pin is shorted to V_{IN} or another high-voltage source.

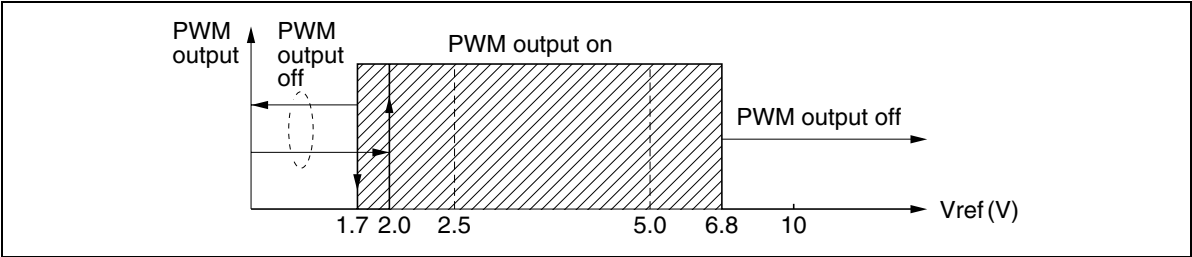


Figure 5.4 Vref Undervoltage Lockout and Overvoltage Protection

UVL Voltage	Vref (V typ)	V _{IN} (V typ)	Description
V _H	2.0 V	3.6 V	V _{IN} increasing: UVL releases; PWM output starts
V _L	1.7 V	3.3 V	V _{IN} decreasing: undervoltage lockout; PWM output stops

6. Usage of ON/OFF Pin

This pin is used for the following purposes:

- To shut down the IC while its input power remains on (power management)
- To externally alter the UVL release voltage
- With the timer (TM) pin, to operate in intermittent mode during overcurrent (see next section)

6.1 Shutdown by ON/OFF Pin Control

The IC can be shut down safely by bringing the voltage at the ON/OFF pin below about 0.7 V (the internal VBE value). This feature can be used in power supply systems to save power. When shut down, the HA16114 draws a maximum current (I_{OFF}) of 10 μ A, while the HA16120 draws a maximum 150 μ A. The ON/OFF pin sinks 290 μ A (Typ) at 5 V, so it can be driven by TTL and other logic ICs. If intermittent mode will also be employed, use a logic IC with an open-collector or open-drain output.

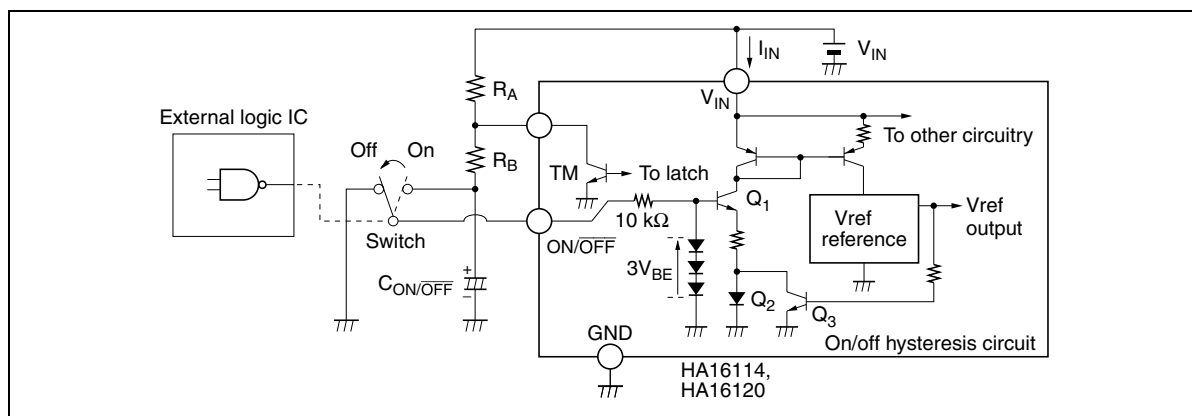


Figure 6.1 Shutdown by ON/OFF Pin Control

6.2 Adjustment of UVL Voltages (when not using intermittent mode)

These ICs permit external adjustment of the undervoltage lockout voltages. The adjustment is made by changing the undervoltage lockout thresholds V_{TH} and V_{TL} relative to V_{IN} , using the relationships shown in the accompanying diagrams.

When the IC is powered up, transistor Q_3 is off, so V_{ON} is $2V_{BE}$, or about 1.4 V. Connection of resistors R_C and R_D in the diagram makes undervoltage lockout release at:

$$V_{IN} = 1.4 \text{ V} \times \frac{R_C + R_D}{R_D}$$

This V_{IN} is the supply voltage at which undervoltage lockout is released. At the release point V_{ref} is still below 2.5 V. To obtain $V_{ref} = 2.5 \text{ V}$, V_{IN} must be at least about 4.3 V.

Since $V_{ON/OFF}$ operates in relation to the base-emitter voltage of internal transistors, V_{ON} has a temperature coefficient of approximately $-4 \text{ mV}/^\circ\text{C}$. Keep this in mind when designing the power supply unit.

When undervoltage lockout and intermittent mode are both used, the intermittent-mode time constant is shortened, so the constants of external components may have to be altered.

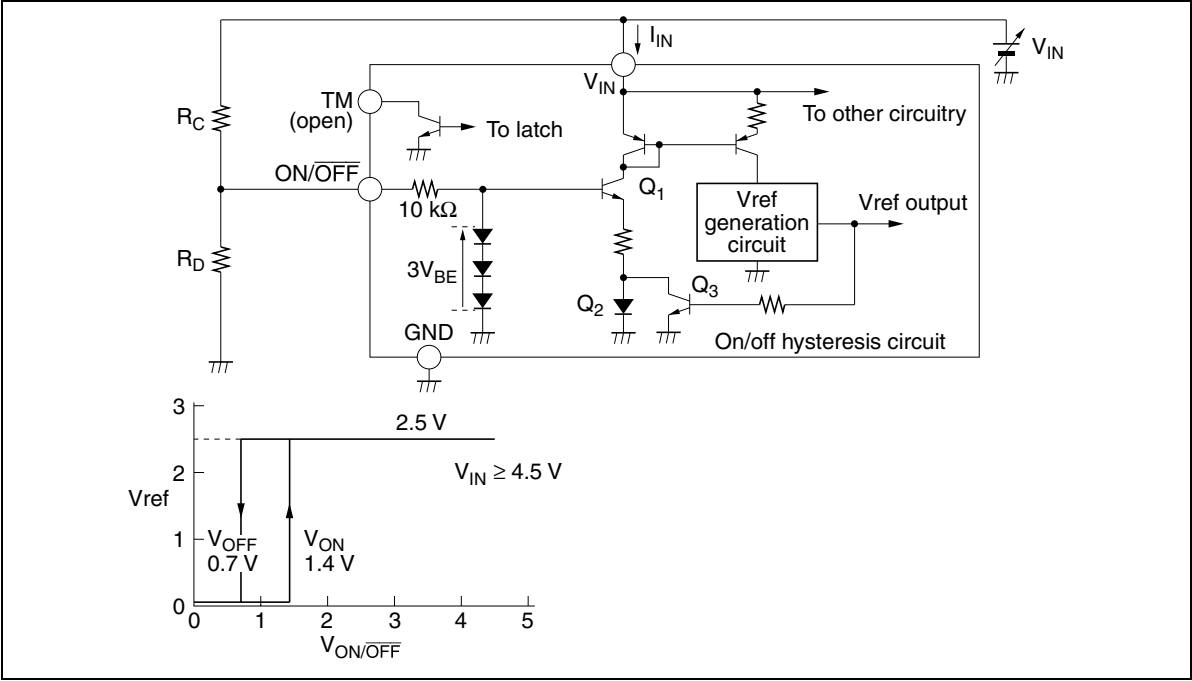


Figure 6.2 Adjustment of UVL Voltages

7. Timing of Intermittent Mode during Overcurrent

7.1 Principle of Operation

These ICs provide pulse-by-pulse overcurrent protection by sensing the current during each pulse and shutting off the pulse if overcurrent is detected. In addition, the TM and ON/OFF pins can be used to operate the IC in intermittent mode if the overcurrent state continues. A power supply with sharp settling characteristics can be designed in this way.

Intermittent mode operates by making use of the hysteresis of the ON/OFF pin threshold voltages V_{ON} and V_{OFF} (V_{ON} - V_{OFF} = V_{BE}). The timing can be programmed as explained below.

When not using intermittent mode, leave the TM pin open, and pull the ON/OFF pin up to V_{ON} or higher. The V_{BE} is base emitter voltage of internal transistors.

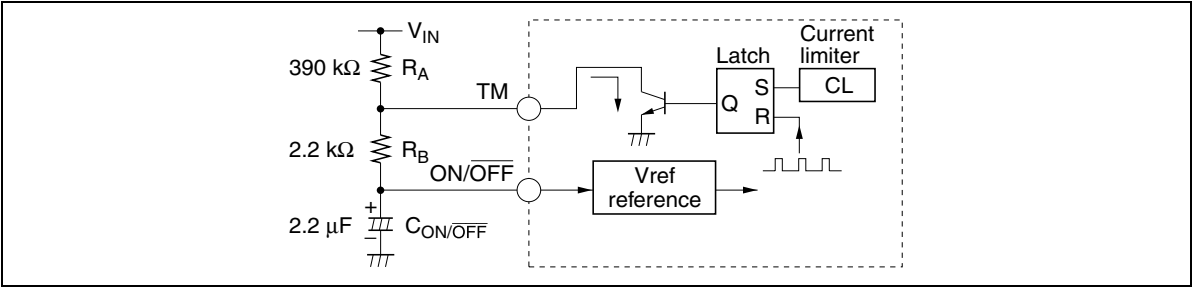
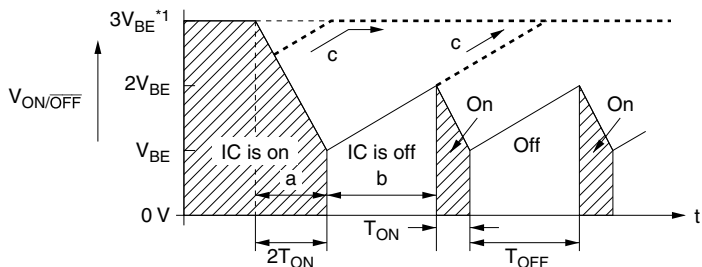


Figure 7.1 Connection Diagram (example)

7.2 Intermittent Mode Timing Diagram ($V_{ON/OFF}$ only)



- Continuous overcurrent is detected
- Intermittent operation starts (IC is off)
- Voltage if overcurrent ends (thick dotted line)

Note: 1. V_{BE} is the base-emitter voltage of internal transistors, and is approximately 0.7 V.
(See the figure 6.1.)

For details, see the overall waveform timing diagram.

Figure 7.2 Intermittent Mode Timing Diagram ($V_{ON/OFF}$ only)

7.3 Calculation of Intermittent Mode Timing

Intermittent mode timing is calculated as follows.

(1) T_{ON} (time until the IC shuts off when continuous overcurrent occurs)

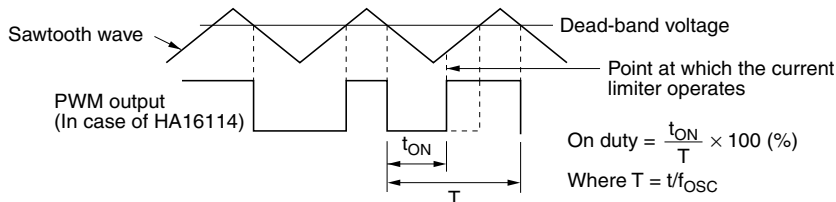
$$\begin{aligned} T_{ON} &= C_{ON/OFF} \times R_B \times \ln \left(\frac{2V_{BE}}{V_{BE}} \right) \times \left(\frac{1}{1 - \text{On duty}^*} \right) \\ &= C_{ON/OFF} \times R_B \times \ln 2 \times \left(\frac{1}{1 - \text{On duty}^*} \right) \\ &\approx 0.69 \times C_{ON/OFF} \times R_B \times \left(\frac{1}{1 - \text{On duty}^*} \right) \end{aligned}$$

(2) T_{OFF} (time from when the IC shuts off until it next turns on)

$$T_{OFF} = C_{ON/OFF} \times (R_A + R_B) \times \ln \left(\frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}} \right)$$

Where $V_{BE} \approx 0.7 \text{ V}$

The greater the overload, the sooner the pulse-by-pulse current limiter operates, the smaller t_{ON} becomes, and from the first equation (1) above, the smaller T_{ON} becomes. From the second equation (2), T_{OFF} depends on V_{IN} . Note that with the connections shown in the diagram, when V_{IN} is switched on the IC does not turn on until T_{OFF} has elapsed.



Note: On duty is the percent of time the IC output is on during one PWM cycle when the pulse-by-pulse current limiter is operating.

Figure 7.3

7.4 Examples of Intermittent Mode Timing (calculated values)

(1) T_{ON}

$$T_{ON} = T_1 \times C_{ON/OFF} \times R_B$$

Here, coefficient

$$T_1 = 0.69 \times \frac{1}{1 - \text{On duty}}$$

from section 7.3 (1) previously.

Example: If $C_{ON/OFF} = 2.2 \mu\text{F}$,
 $R_B = 2.2 \text{ k}\Omega$, and the on duty
of the current limiter is 75%,
then $T_{ON} = 13 \text{ ms}$.

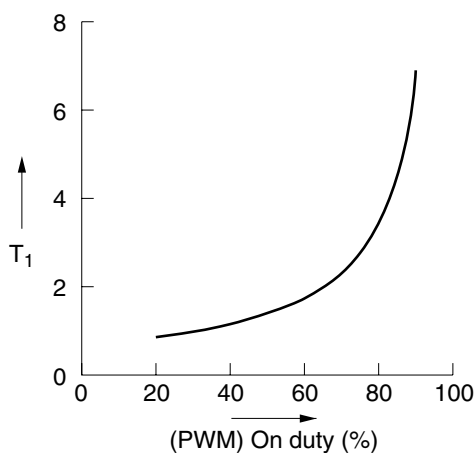


Figure 7.4 Examples of Intermittent Mode Timing (1)

(2) T_{OFF}

$$T_{OFF} = T_2 \times C_{ON/OFF} \times (R_A + R_B)$$

Here, coefficient

$$T_2 = \ln \frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}}$$

from section 7.3 (2) previously.

Example: If $C_{ON/OFF} = 2.2 \mu\text{F}$, $R_B = 2.2 \text{ k}\Omega$,
 $R_A = 390 \text{ k}\Omega$, $V_{IN} = 12 \text{ V}$,
then $T_{OFF} = 55 \text{ ms}$.

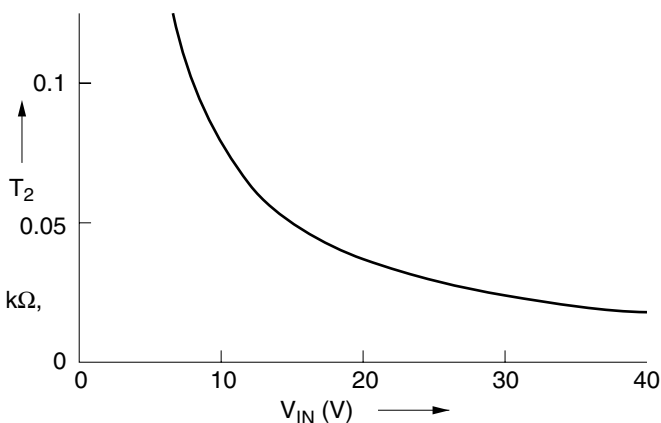


Figure 7.5 Examples of Intermittent Mode Timing (2)

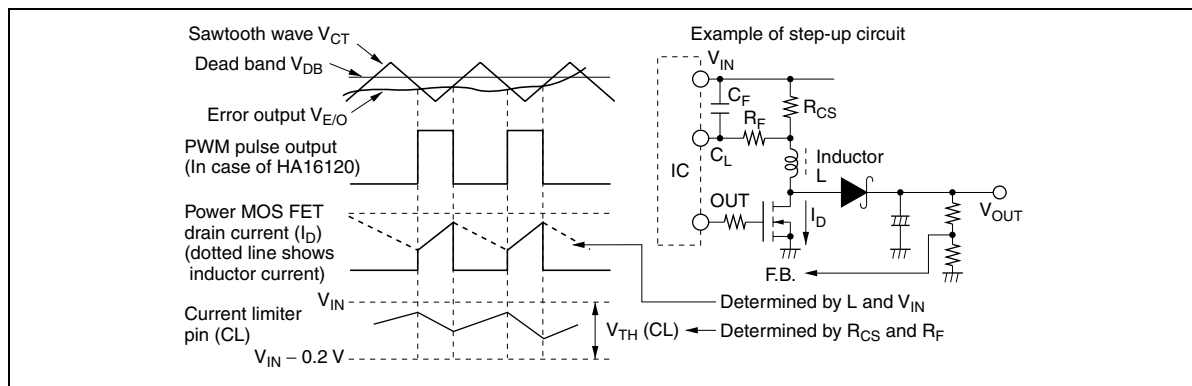


Figure 7.6

8. Setting the Overcurrent Detection Threshold

The voltage drop V_{TH} at which overcurrent is detected in these ICs is typically 0.2 V. The bias current is typically 200 μ A. The power MOS FET peak current value before the current limiter goes into operation is given as follows.

$$I_D = \frac{V_{TH} - (R_F + R_{CS}) \times I_{BCL}}{R_{CS}}$$

Where, $V_{TH} = V_{IN} - V_{CL} = 0.2$ V, V_{CL} is a voltage referred on GND.

Note that R_F and C_F form a low-pass filter with a cutoff frequency determined by their RC time constant. This filter prevents incorrect operation due to current spikes when the power MOS FET is switched on or off.

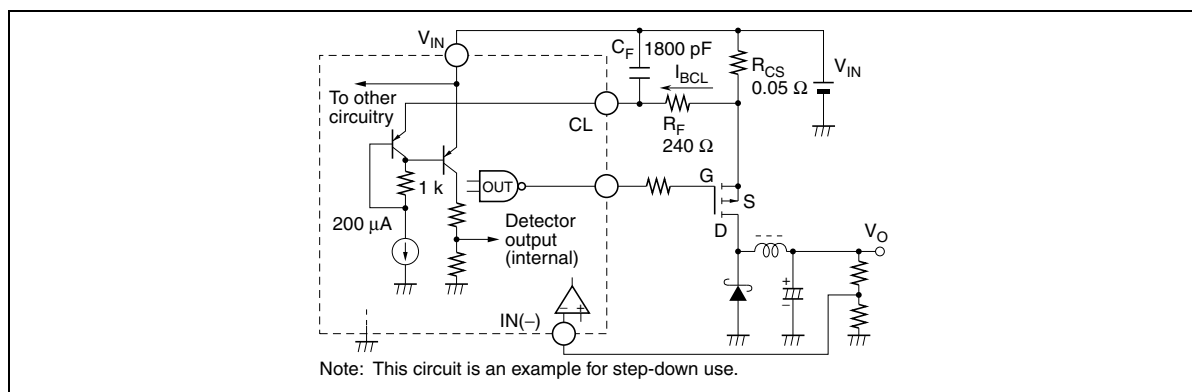


Figure 8.1 Example for Step-Down Use

With the values shown in the diagram, the peak current is:

$$I_D = \frac{0.2 \text{ V} - (240 \Omega + 0.05 \Omega) \times 200 \mu\text{A}}{0.05 \Omega} = 3.04 \text{ A}$$

The filter cutoff frequency is calculated as follows:

$$f_C = \frac{1}{2\pi C_F R_F} = \frac{1}{6.28 \times 1800 \text{ pF} \times 240 \Omega} = 370 \text{ kHz}$$

Absolute Maximum Ratings

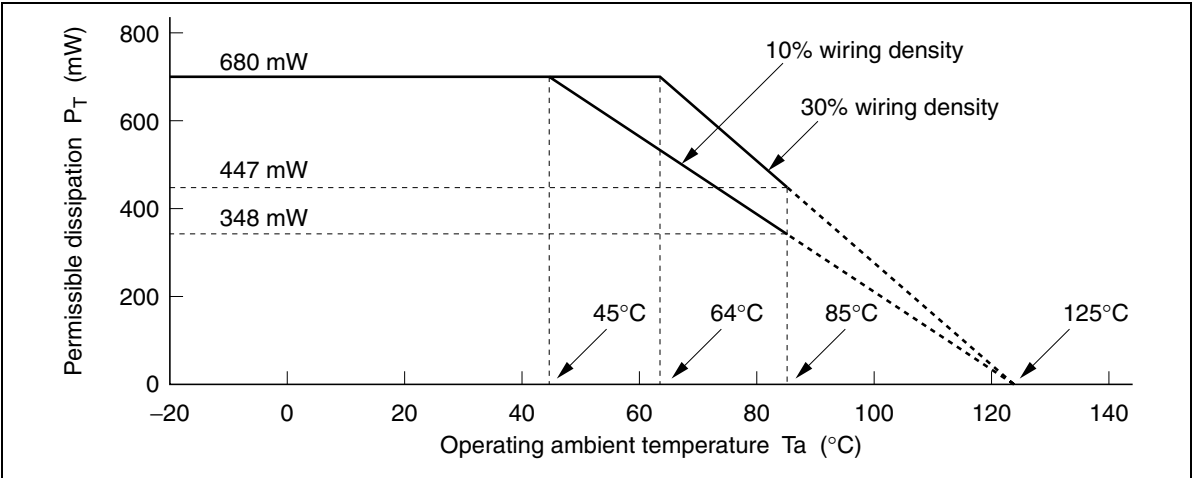
(Ta = 25°C)

Item	Symbol	Rating		Unit
		HA16114P/FP, HA16120FP	HA16114PJ/FPJ, HA16120FPJ	
Supply voltage	V _{IN}	40	40	V
Output current (DC)	I _O	±0.1	±0.1	A
Output current (peak)	I _O peak	±1.0	±1.0	A
Current limiter input voltage	V _{CL}	V _{IN}	V _{IN}	V
Error amplifier input voltage	V _{IEA}	V _{IN}	V _{IN}	V
E/O input voltage	V _{IE/O}	V _{ref}	V _{ref}	V
RT source current	I _{RT}	500	500	μA
TM sink current	I _{TM}	3	3	mA
SYNC voltage	V _{SYNC}	V _{ref}	V _{ref}	V
SYNC current	I _{SYNC}	±250	±250	μA
Power dissipation	P _T	680*1, *2	680*1, *2	mW
Operating temperature	Topr	−20 to +85	−40 to +85	°C
Junction temperature	TjMax	125	125	°C
Storage temperature	Tstg	−55 to +125	−55 to +125	°C

Notes: 1. This value is for an SOP package (FP) and is based on actual measurements on a 40 × 40 × 1.6 mm glass epoxy circuit board. With a 10% wiring density, this value is permissible up to Ta = 45°C and should be derated by 8.3 mW/°C at higher temperatures. With a 30% wiring density, this value is permissible up to Ta = 64°C and should be derated by 11.1 mW/°C at higher temperatures.

2. For the DILP package.

This value applies up to Ta = 45°C; at temperatures above this, 8.3 mW/°C derating should be applied.

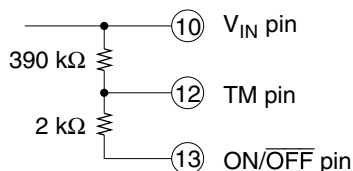


Electrical Characteristics

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Voltage reference section	Output voltage	V _{ref}	2.45	2.50	2.55	V	I _O = 1 mA	
	Line regulation	Line	—	2	60	mV	4.5 V ≤ V _{IN} ≤ 40V	1
	Load regulation	Load	—	30	60	mV	0 ≤ I _O ≤ 10 mA	
	Short-circuit output current	I _{OS}	10	24	—	mA	V _{ref} = 0 V	
	V _{ref} overvoltage protection threshold	V _{rov}	6.2	6.8	7.4	V		
	Temperature stability of output voltage	ΔV _{ref} /ΔTa	—	100	—	ppm/°C		
	V _{ref} adjustment voltage	V _{ADJ}	1.225	1.25	1.275	V		
Sawtooth oscillator section	Maximum frequency	f _{max}	600	—	—	kHz		
	Minimum frequency	f _{min}	—	—	1	Hz		
	Frequency stability with input voltage	Δf/f ₀₁	—	±1	±3	%	4.5 V ≤ V _{IN} ≤ 40 V (f ₀₁ = (f _{max} + f _{min})/2)	
	Frequency stability with temperature	Δf/f ₀₂	—	±5	—	%	−20°C ≤ Ta ≤ 85°C (f ₀₂ = (f _{max} + f _{min})/2)	
	Oscillator frequency	f _{OSC}	90	100	110	kHz	R _T = 10 kΩ C _T = 1300 pF	
Dead-band adjustment section	Low level threshold voltage	V _{TL}	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	V _{TH}	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	ΔV _{TH}	0.5	0.6	0.7	V	ΔV _{TH} = V _{TH} − V _{TL}	
	Output source current	I _{source}	170	250	330	μA	DB pin: 0 V	
PWM comparator section	Low level threshold voltage	V _{TL}	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	V _{TH}	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	ΔV _{TH}	0.5	0.6	0.7	V	ΔV _{TH} = V _{TH} − V _{TL}	

Note: 1. Resistors connected to ON/OFF pin:



Electrical Characteristics (cont.)

(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Error amplifier section	Input offset voltage	V _{IO}	—	2	10	mV		
	Input bias current	I _B	—	0.5	2.0	μA		
	Output sink current	I _{Osink}	28	40	52	μA	V _O = 2.5 V	
	Output source current	I _{Osource}	28	40	52	μA	V _O = 1.0 V	
	Common-mode input voltage range	V _{CM}	1.1	—	3.7	V		
	Voltage gain	A _V	40	50	—	dB	f = 10 kHz	
	Unity gain bandwidth	BW	—	4	—	MHz		
	High level output voltage	V _{OH}	3.5	4.0	—	V	I _O = 10 μA	
	Low level output voltage	V _{OL}	—	0.2	0.5	V	I _O = 10 μA	
Overcurrent detection section	Threshold voltage	V _{TH}	V _{IN} –0.22	V _{IN} –0.2	V _{IN} –0.18	V		
	CL(–) bias current	I _{BCL(–)}	140	200	260	μA	CL(–) = V _{IN}	
	Turn-off time	t _{OFF}	—	200	300	ns		1
			—	500	600	ns		2
UVL section	Vref high level threshold voltage	V _{TH}	1.7	2.0	2.3	V		
	Vref low level threshold voltage	V _{TL}	1.4	1.7	2.0	V		
	Threshold difference	ΔV _{TH}	0.1	0.3	0.5	V	ΔV _{TH} = V _{TH} – V _{TL}	
	VIN high level threshold voltage	V _{INH}	3.3	3.6	3.9	V		
	VIN low level threshold voltage	V _{INL}	3.0	3.3	3.6	V		

Notes: 1. HA16114 only.
2. HA16120 only.

Electrical Characteristics (cont.)

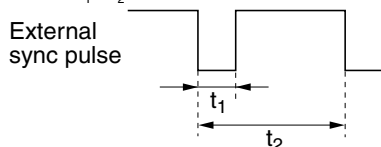
(Ta = 25°C, V_{IN} = 12 V, f_{OSC} = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Output stage	Output low voltage	V _{OL}	—	0.9	1.5	V	I _{OSink} = 10 mA	
	Output high voltage	V _{OH1}	V _{IN} –2.2	V _{IN} –1.6	—	V	I _{Osource} = 10 mA	
	High voltage when off	V _{OH2}	V _{IN} –2.2	V _{IN} –1.6	—	V	I _{Osource} = 1 mA ON/OFF pin: 0 V	1
	Low voltage when off	V _{OL2}	—	0.9	1.5	V	I _{OSink} = 1 mA ON/OFF pin: 0 V	2
	Rise time	t _r	—	50	200	ns	C _L = 1000 pF	
	Fall time	t _f	—	50	200	ns	C _L = 1000 pF	
External sync section	SYNC source current	I _{SYNC}	120	180	240	μA	SYNC pin: 0 V	
	Sync input frequency range	f _{SYNC}	f _{OSC}	—	f _{OSC} × 2	kHz		
	External sync initiation voltage	V _{SYNC}	V _{ref} –1.0	—	V _{ref} –0.5	V		
	Minimum pulse width of sync input	PW _{min}	300	—	—	ns		
	Input sync pulse duty cycle	PW	5	—	50	%		3
On/off section	ON/OFF sink current 1	I _{ON/OFF1}	60	90	120	μA	ON/OFF pin: 3 V	
	ON/OFF sink current 2	I _{ON/OFF2}	220	290	380	μA	ON/OFF pin: 5 V	
	IC on threshold	V _{ON}	1.1	1.4	1.7	V		
	IC off threshold	V _{OFF}	0.4	0.7	1.0	V		
	ON/OFF threshold difference	ΔV _{ON/OFF}	0.5	0.7	0.9	V		
Total device	Operating current	I _{IN}	6.0	8.5	11.0	mA	C _L = 1000 pF	
	Quiescent current	I _{OFF}	0	—	10	μA	ON/OFF pin: 0 V	1
			—	120	150	μA	ON/OFF pin: 0 V	2

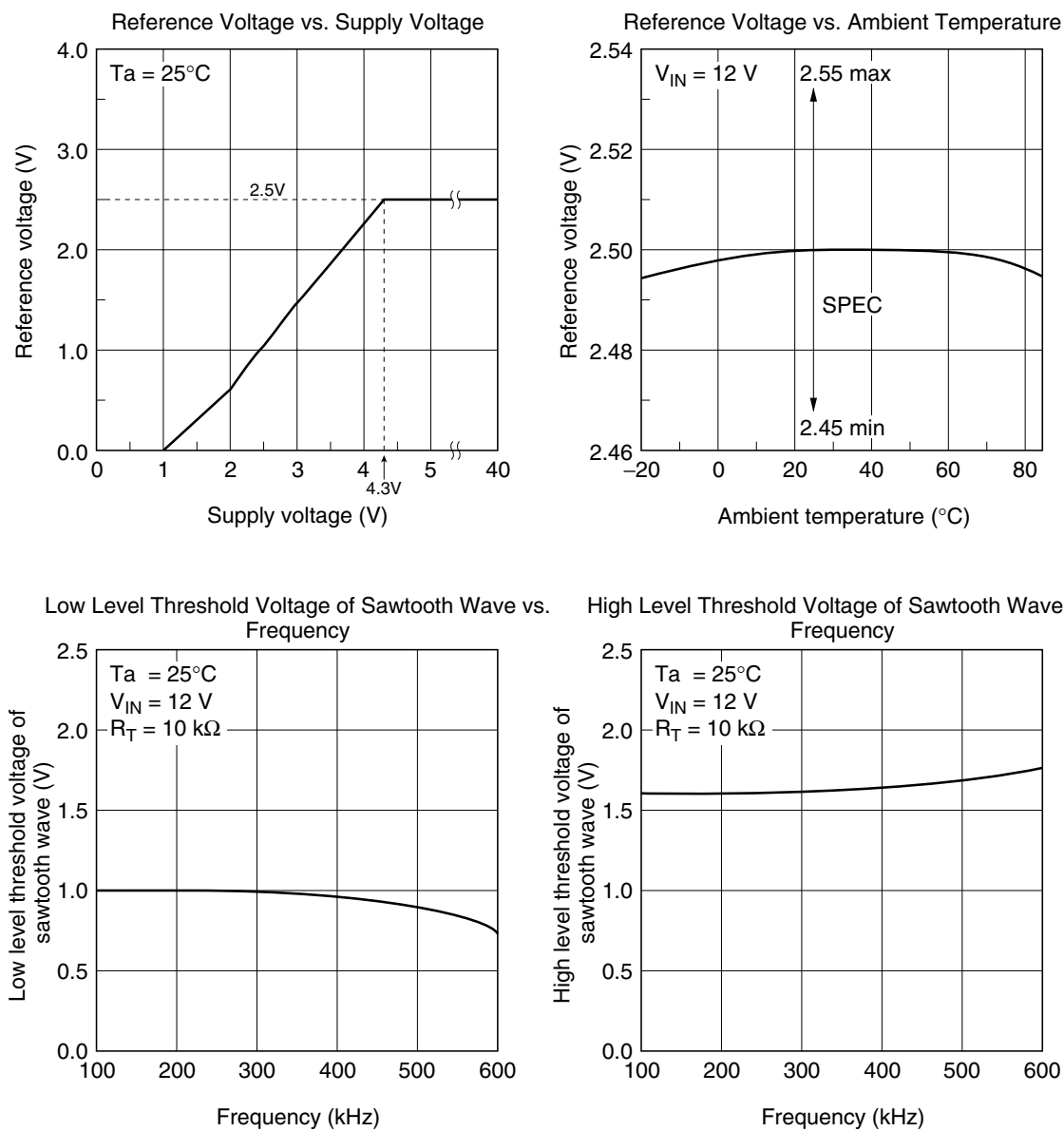
Notes: 1. HA16114 only.

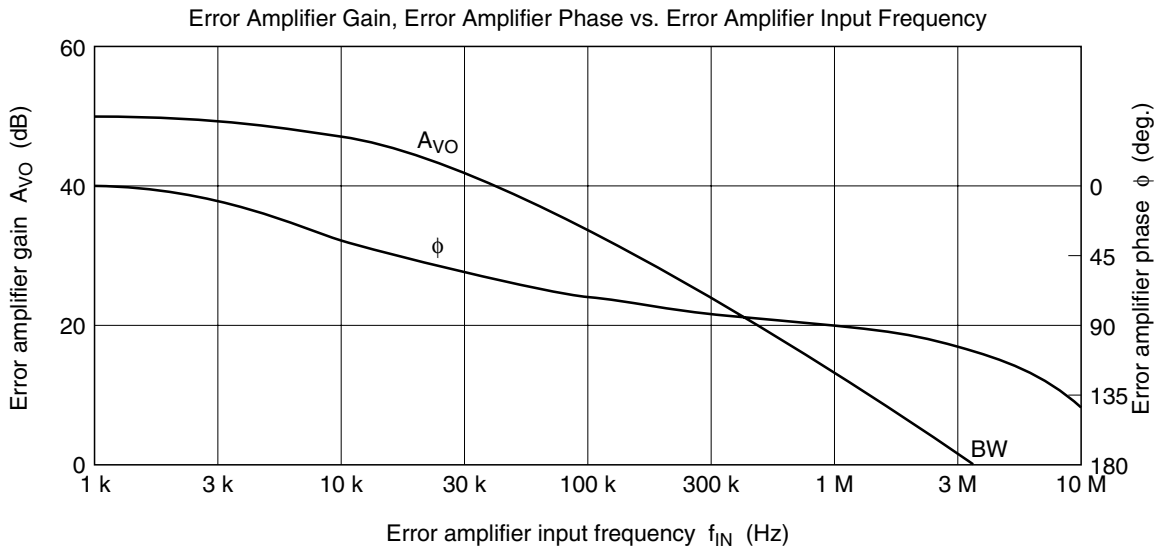
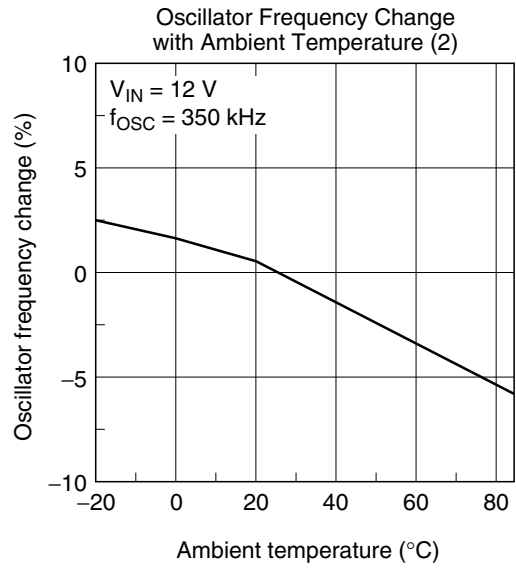
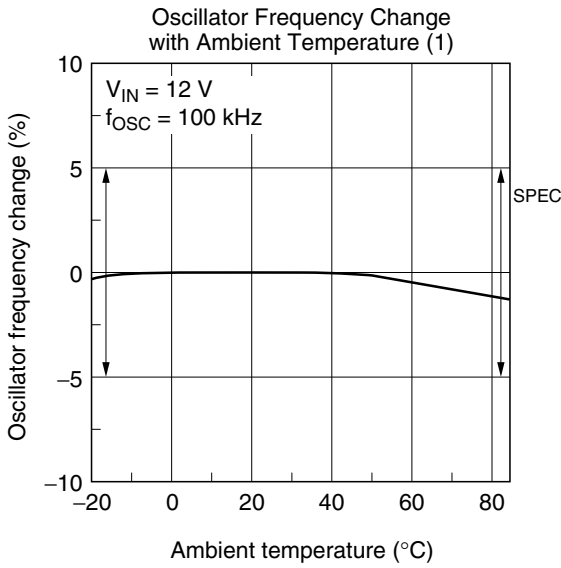
2. HA16120 only.

3. $PW = t_1 / t_2 \times 100$

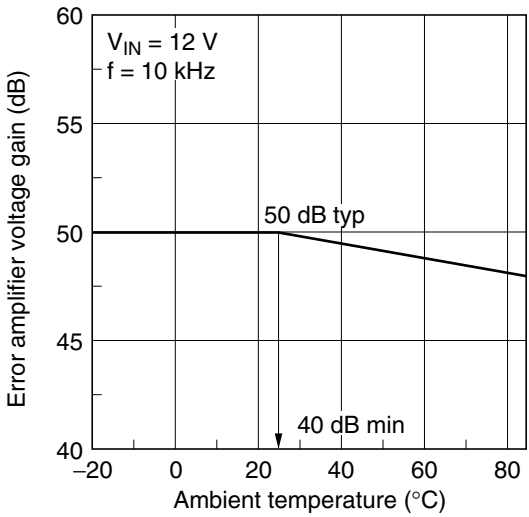


Characteristic Curves

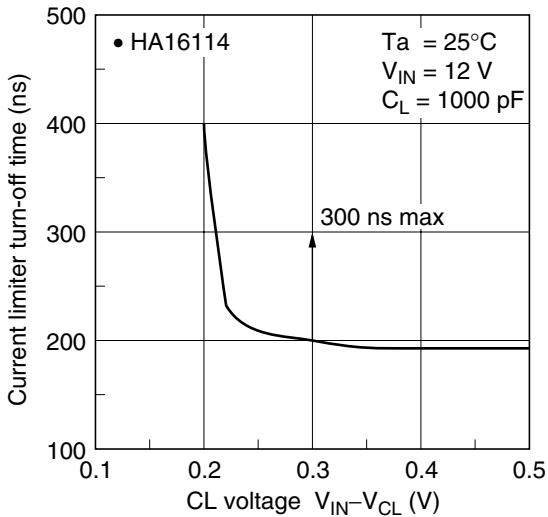




Error Amplifier Voltage Gain vs. Ambient Temperature

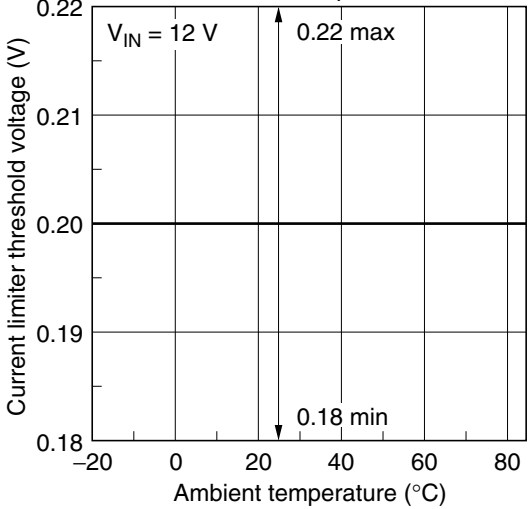


Current Limiter Turn-Off Time vs. Current Limiter Threshold Voltage ^{Note}

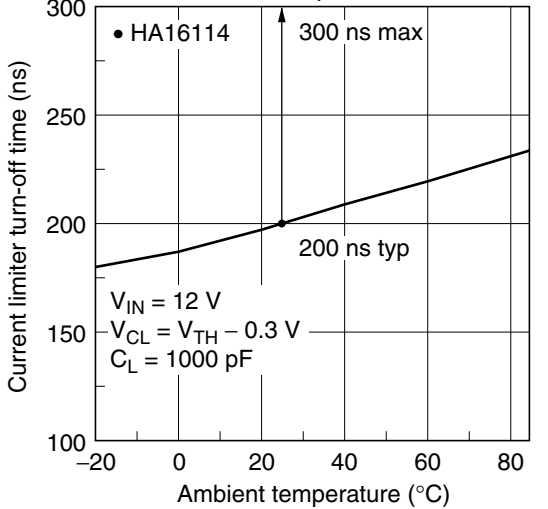


Note: Approximately 300 ns greater than this in the case of the HA16120.

Current Limiter Threshold Voltage vs. Ambient Temperature

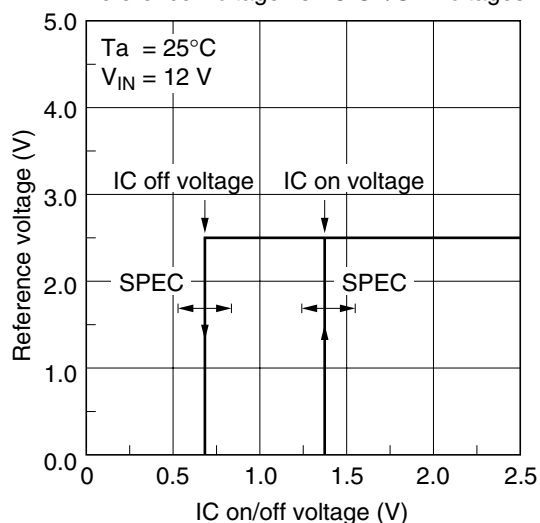


Current Limiter Turn-Off Time vs. Ambient Temperature ^{Note}

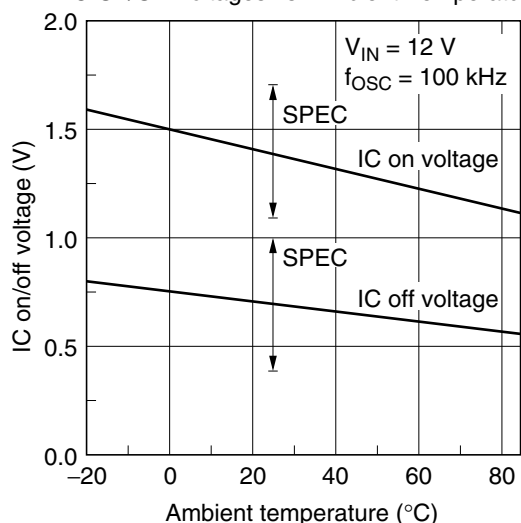


Note: Approximately 300 ns greater than this in the case of the HA16120.

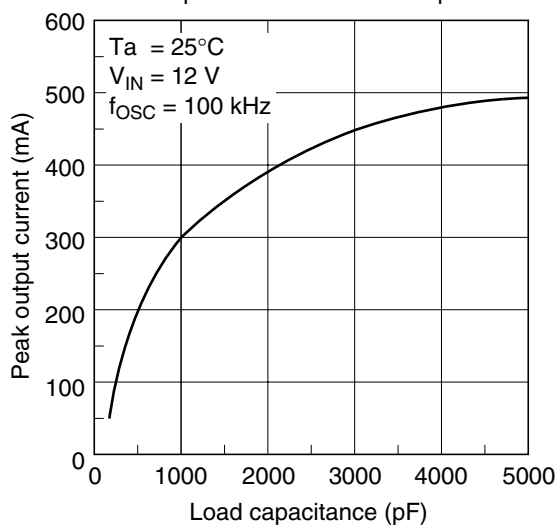
Reference Voltage vs. IC On/Off Voltages



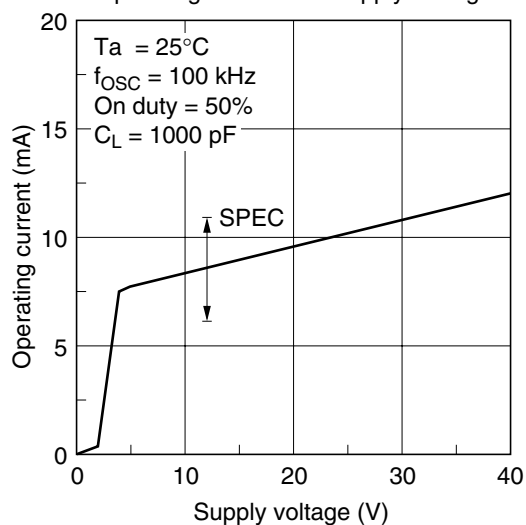
IC On/Off Voltages vs. Ambient Temperature



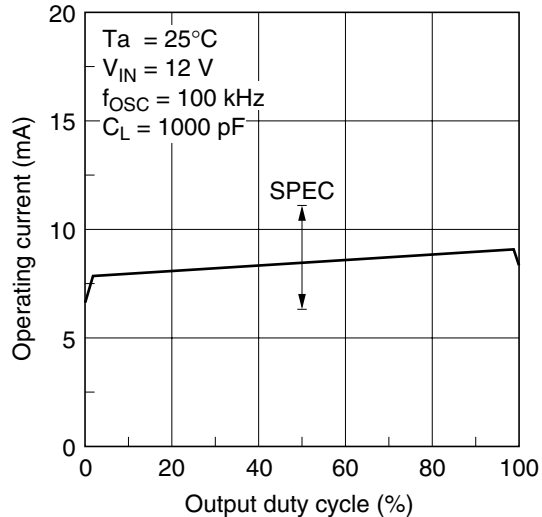
Peak Output Current vs. Load Capacitance



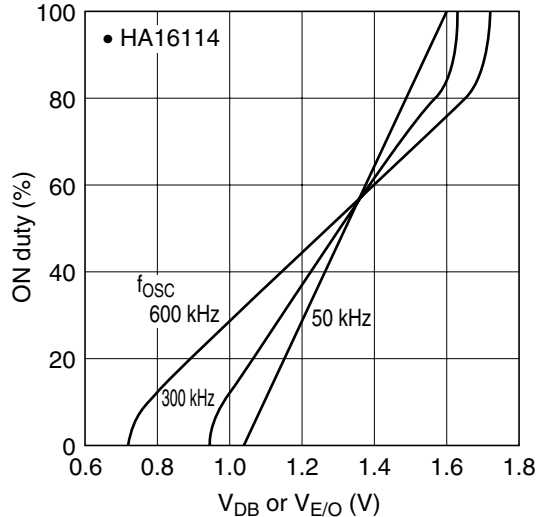
Operating Current vs. Supply Voltage



Operating Current vs. Output Duty Cycle

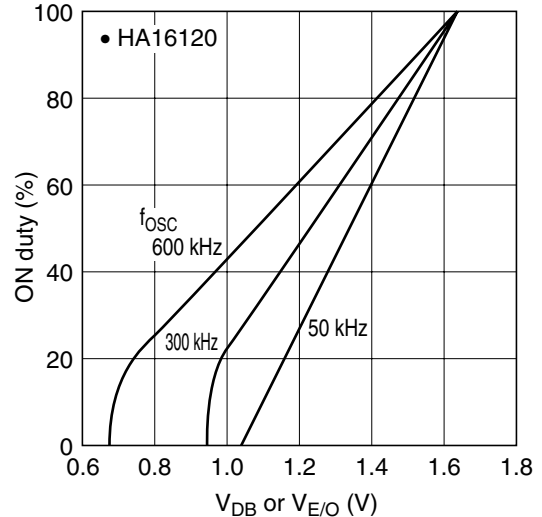


PWM Comparator Input vs. Output Duty Cycle (1)

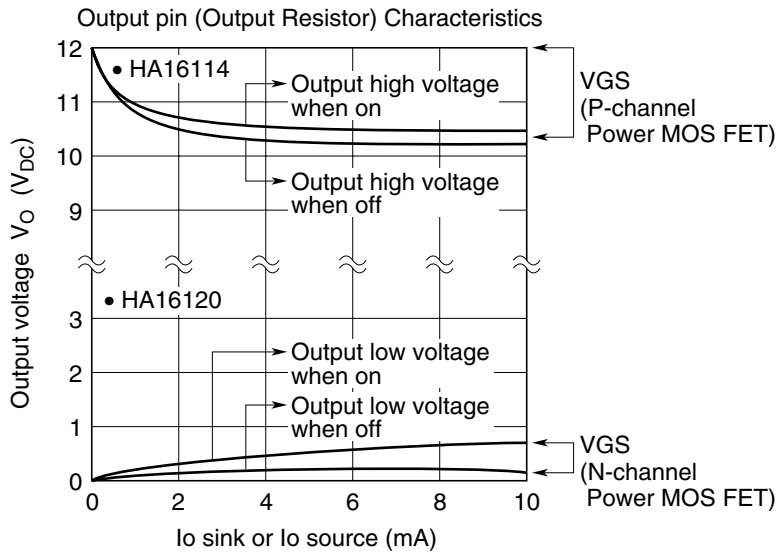


Note: The on-duty of the HA16114 is the proportion of one cycle during which output is low.

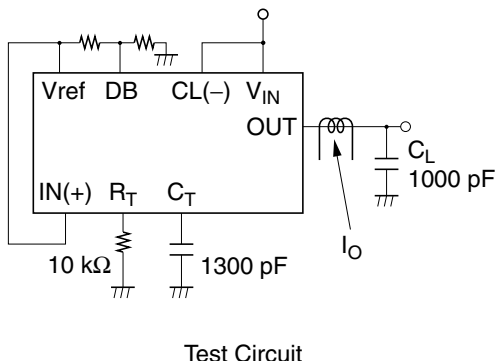
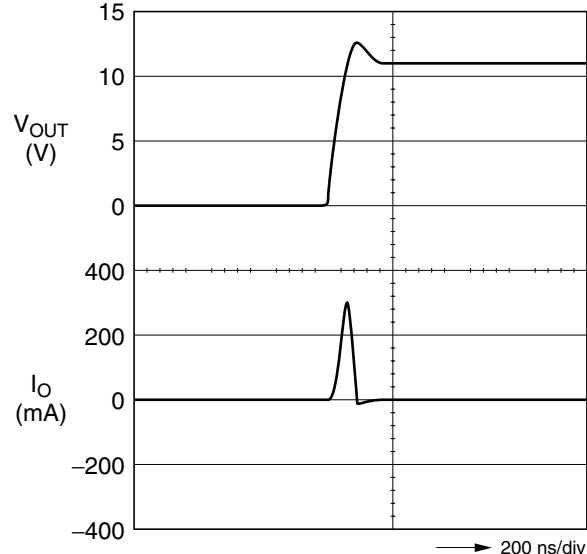
PWM Comparator Input vs. Output Duty Cycle (2)



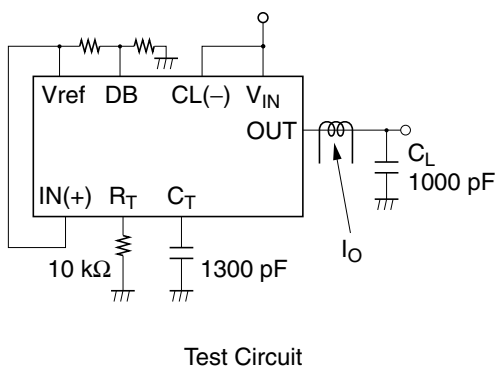
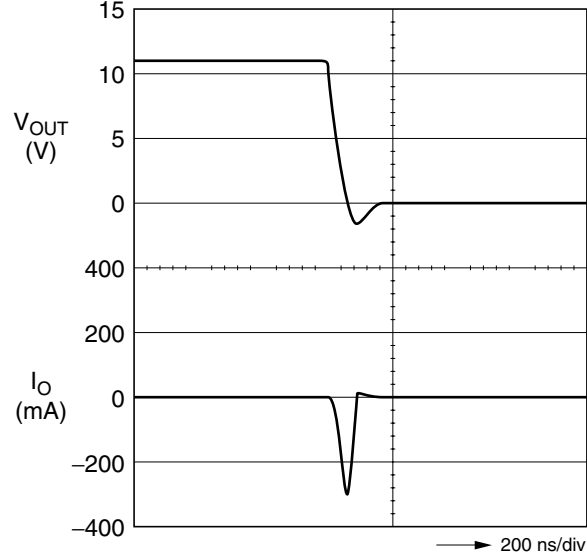
Note: The on-duty of the HA16120 is the proportion of one cycle during which output is high.

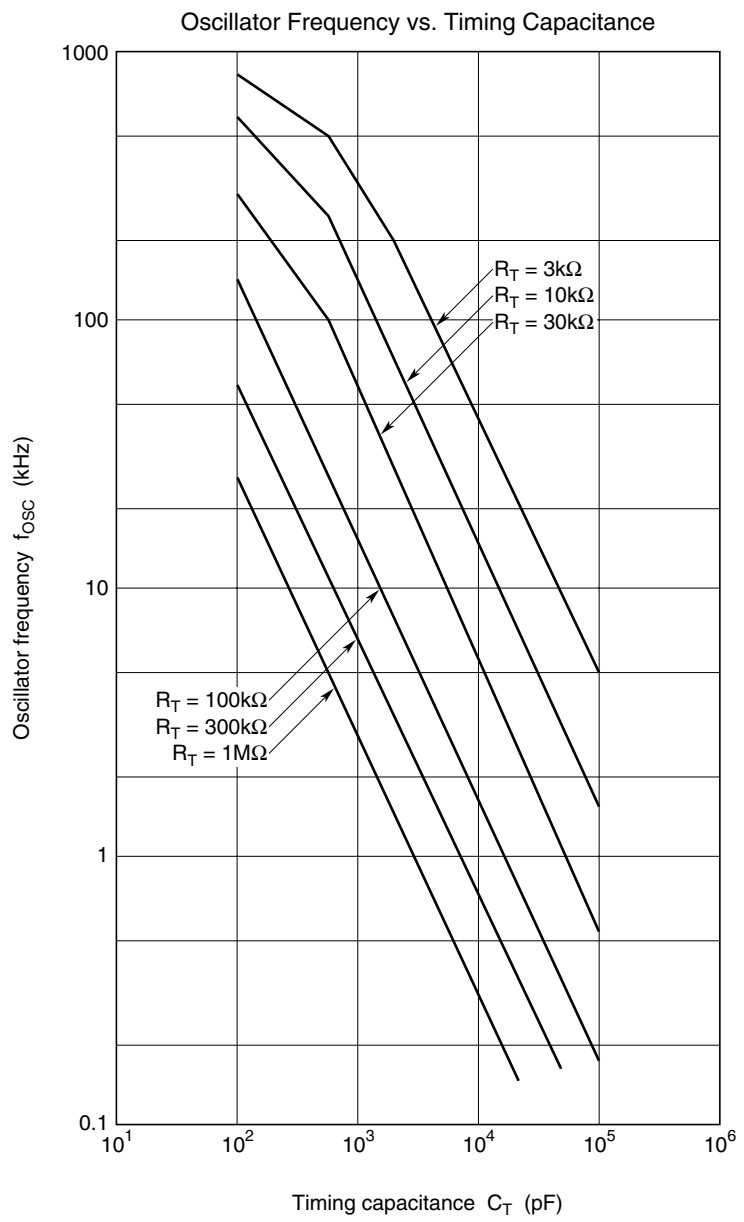


Output Waveforms: Rise of Output Voltage V_{OUT}



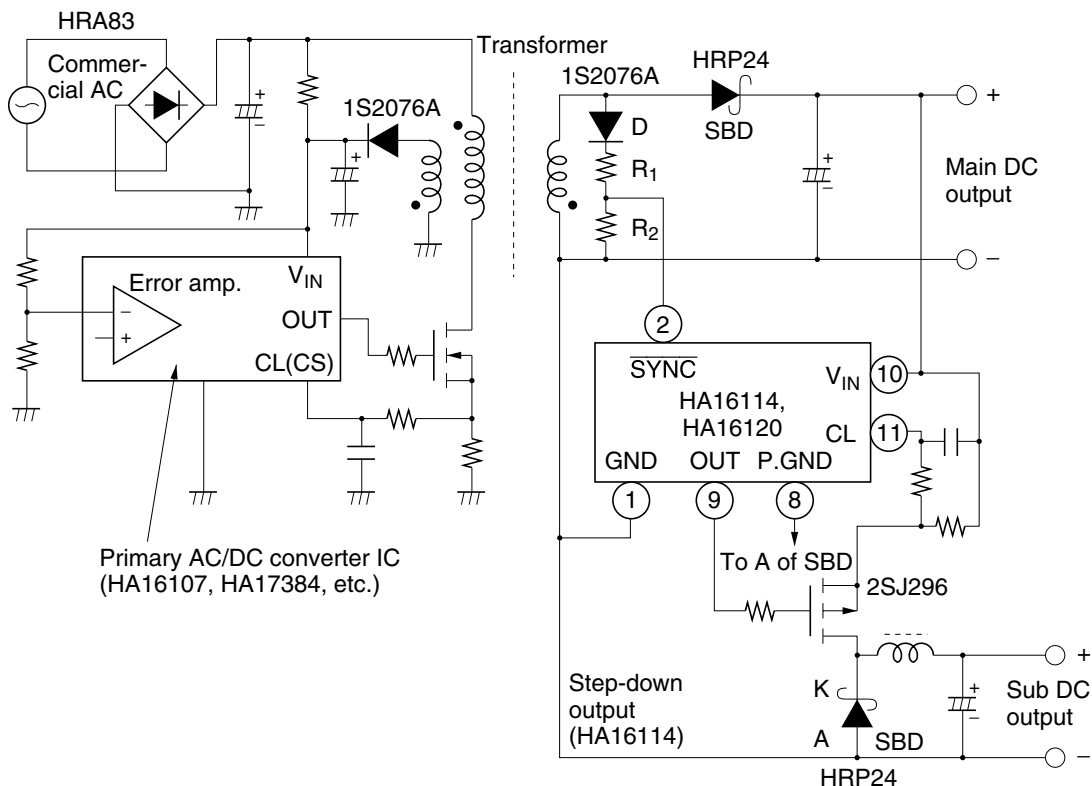
Output Waveforms: Fall of Output Voltage V_{OUT}





Application Examples (2)

- External Synchronization with Primary-Control AC/DC Converter
(1) Combination with a flyback AC/DC converter (simplified schematic)

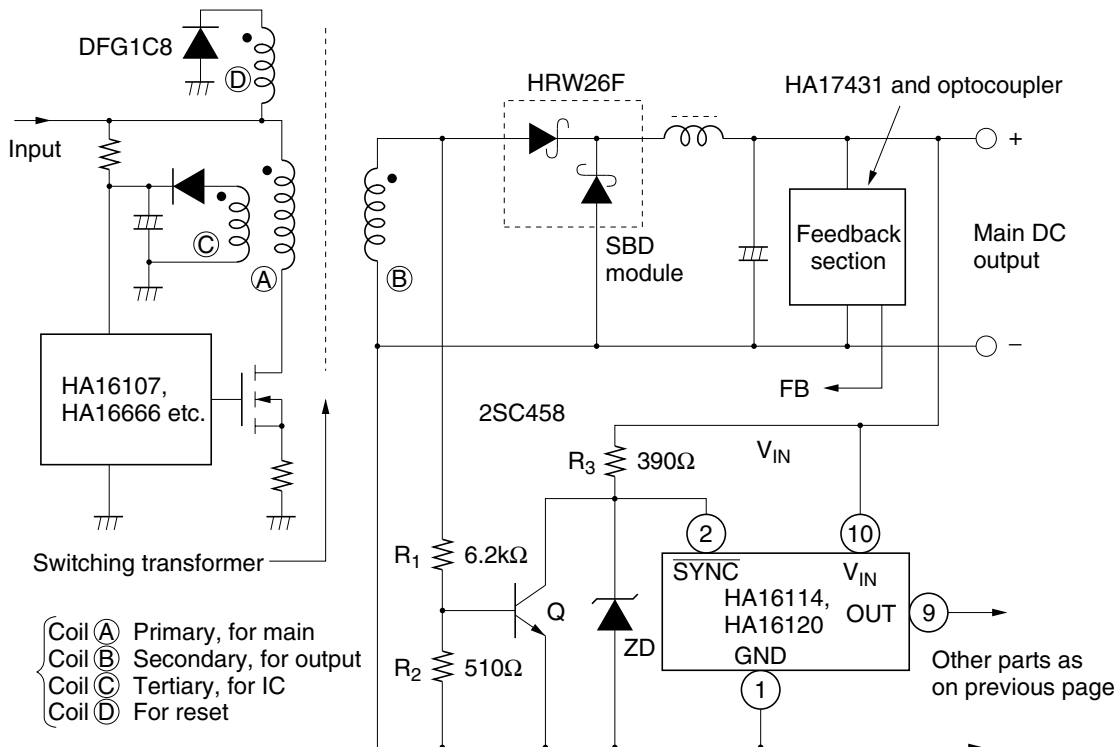


This is one example of a circuit that uses the features of the HA16114/120 by operating in synchronization with a flyback AC/DC converter. Note the following design points concerning the circuit from the secondary side of the transformer to the $\overline{\text{SYNC}}$ pin of the HA16114/120.

- Diode D prevents reverse current. Always insert a diode here. Use a general-purpose switching diode.
- Resistors R_1 and R_2 form a voltage divider to ensure that the input voltage swing at the $\overline{\text{SYNC}}$ pin does not exceed V_{ref} (2.5 V). To maintain operating speed, $R_1 + R_2$ should not exceed 10 k Ω .

Application Examples (3)

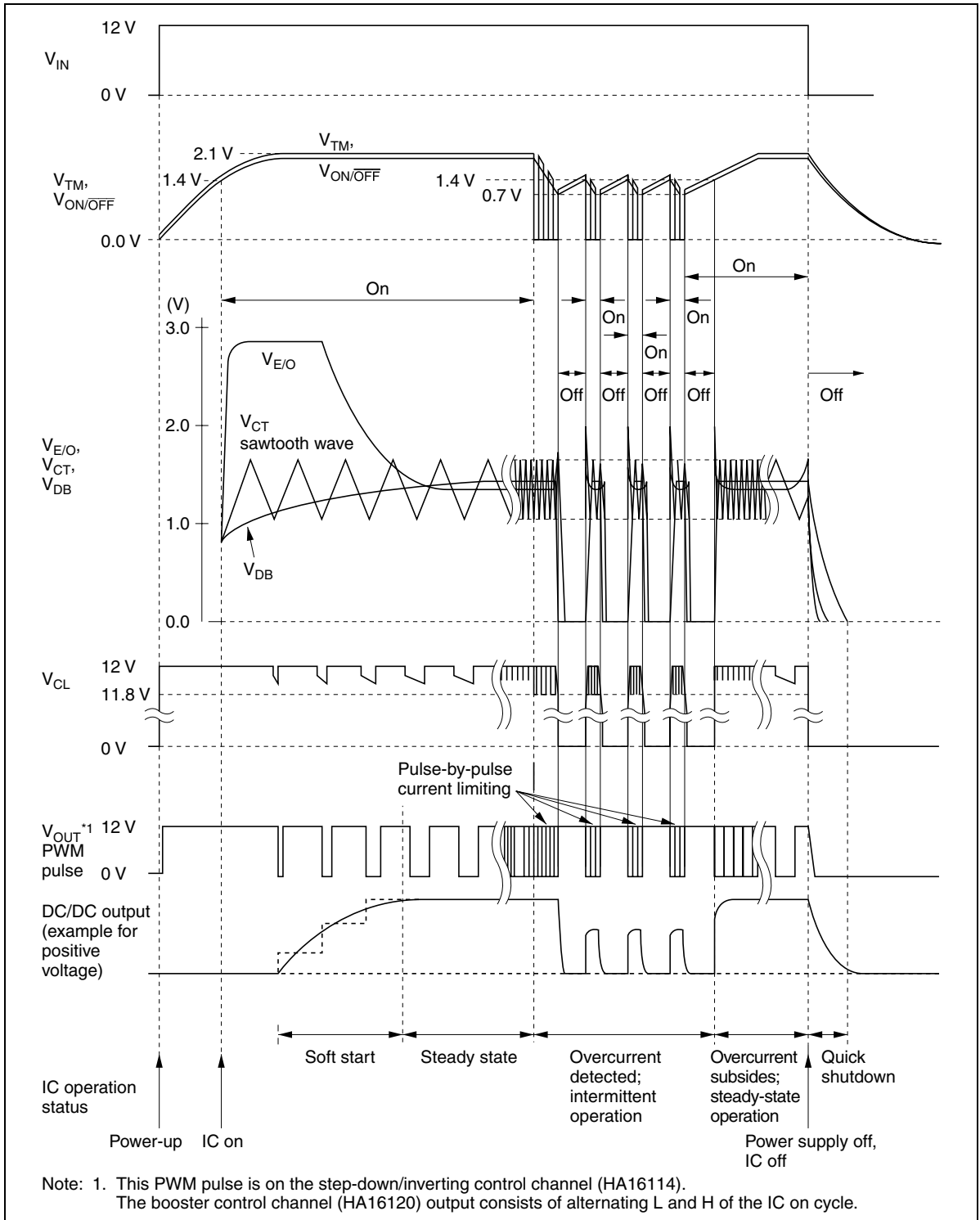
- External Synchronization with Primary-Control AC/DC Converter (cont.)
- (2) Combination with a forward AC/DC converter (simplified schematic)



This circuit illustrates the combination of the HA16114/120 with a forward AC/DC converter. The HA16114/120 synchronizes with the falling edge of the external sync signal, so with a forward transformer, the sync pulses must be inverted. In the diagram, this is done by an external circuit consisting of the following components:

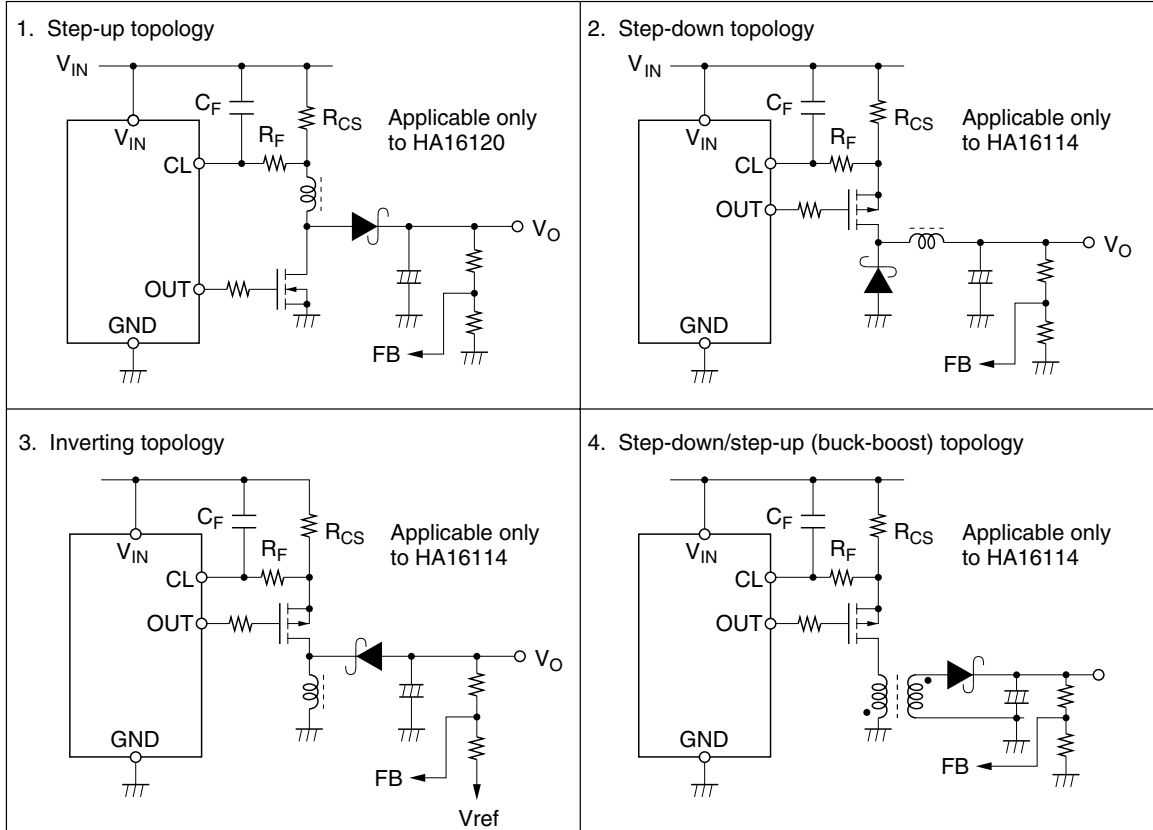
- Q: Transistor for inverting the pulses. Use a small-signal transistor.
- R₁ and R₂: These resistors form a voltage divider for driving the base of transistor Q. R₂ also provides a path for base discharge, so that the transistor can turn off quickly.
- R₃: Load resistor for transistor Q.
- ZD: Zener diode for protecting the $\overline{\text{SYNC}}$ pin.

Overall Waveform Timing Diagram (for Application Example (1))



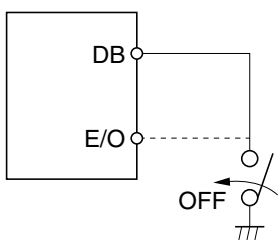
Application Examples (4) (Some Pointers on Use)

1. Inductor, Power MOS FET, and Diode Connections



2. Turning Output On and Off while the IC is On

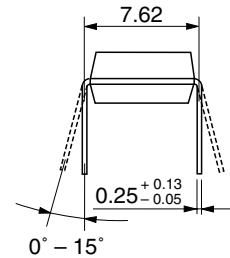
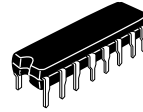
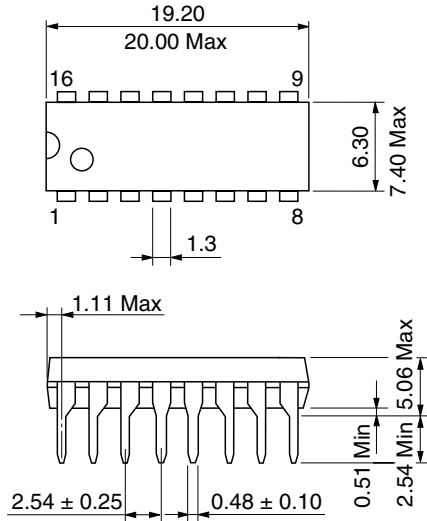
To turn only one channel off, ground the DB pin or the E/O pin.
In the case of E/O, however, there will be no soft start when the output is turned back on.



Package Dimensions

As of January, 2002

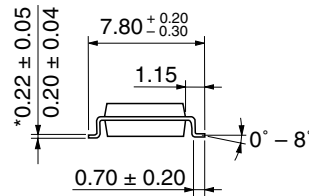
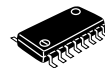
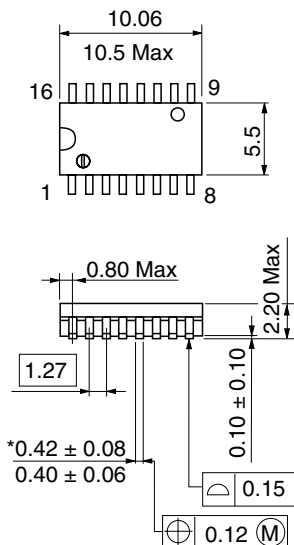
Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.07 g

As of January, 2002

Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

Sales Offices**HITACHI****Hitachi, Ltd.**

Semiconductor & Integrated Circuits
 Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
 Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor
 (America) Inc.
 179 East Tasman Drive
 San Jose, CA 95134
 Tel: <1> (408) 433-1990
 Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
 Electronic Components Group
 Whitebrook Park
 Lower Cookham Road
 Maidenhead
 Berkshire SL6 8YA, United Kingdom
 Tel: <44> (1628) 585000
 Fax: <44> (1628) 585200

Hitachi Europe GmbH
 Electronic Components Group
 Dornacher Straße 3
 D-85622 Feldkirchen
 Postfach 201, D-85619 Feldkirchen
 Germany
 Tel: <49> (89) 9 9180-0
 Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
 Hitachi Tower
 16 Collyer Quay #20-00
 Singapore 049318
 Tel: <65>-6538-6533/6538-8577
 Fax: <65>-6538-6933/6538-3877
 URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
 (Taipei Branch Office)
 4/F, No. 167, Tun Hwa North Road
 Hung-Kuo Building
 Taipei (105), Taiwan
 Tel: <886>-(2)-2718-3666
 Fax: <886>-(2)-2718-8180
 Telex: 23222 HAS-TP
 URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
 Group III (Electronic Components)
 7/F., North Tower
 World Finance Centre,
 Harbour City, Canton Road
 Tsim Sha Tsui, Kowloon Hong Kong
 Tel: <852>-2735-9218
 Fax: <852>-2730-0281
 URL: <http://semiconductor.hitachi.com.hk>

Copyright © Hitachi, Ltd., 2002. All rights reserved. Printed in Japan.
 Colophon 6.0