

# IS31FL3726

## 16-BIT COLOR LED DRIVER WITH PWM CONTROL

June 2013

### GENERAL DESCRIPTION

The IS31FL3726 is comprised of constant-current drivers designed for color LEDs. The output current value can be set using an external resistor. The output current value can be adjusted from 5mA to 60mA through the external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-bit constant t-current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

These drivers have been designed using the CMOS process.

### FEATURES

- Output current capability and number of outputs: 60mA × 16 outputs
- Constant current range: 5mA to 60mA
- Application output voltage:  $\geq 0.4V$
- For anode-common LEDs
- Power supply voltage range,  $V_{DD} = 3.3V$  to  $5.5V$
- Serial and parallel data transfer rate: 20MHz (Max. cascade connection)
- Operating temperature range,  $T_A = -40^{\circ}C \sim +85^{\circ}C$
- Package: QFN-24 and TSSOP-24
- Current accuracy (All output on)

| Output voltage | Current Accuracy |             | Output Current |
|----------------|------------------|-------------|----------------|
|                | Between Bits     | Between ICs |                |
| $\geq 0.4V$    | $\pm 4\%$        | $\pm 20\%$  | 5mA ~ 60mA     |

### APPLICATIONS

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Toys

### BLOCK DIAGRAM

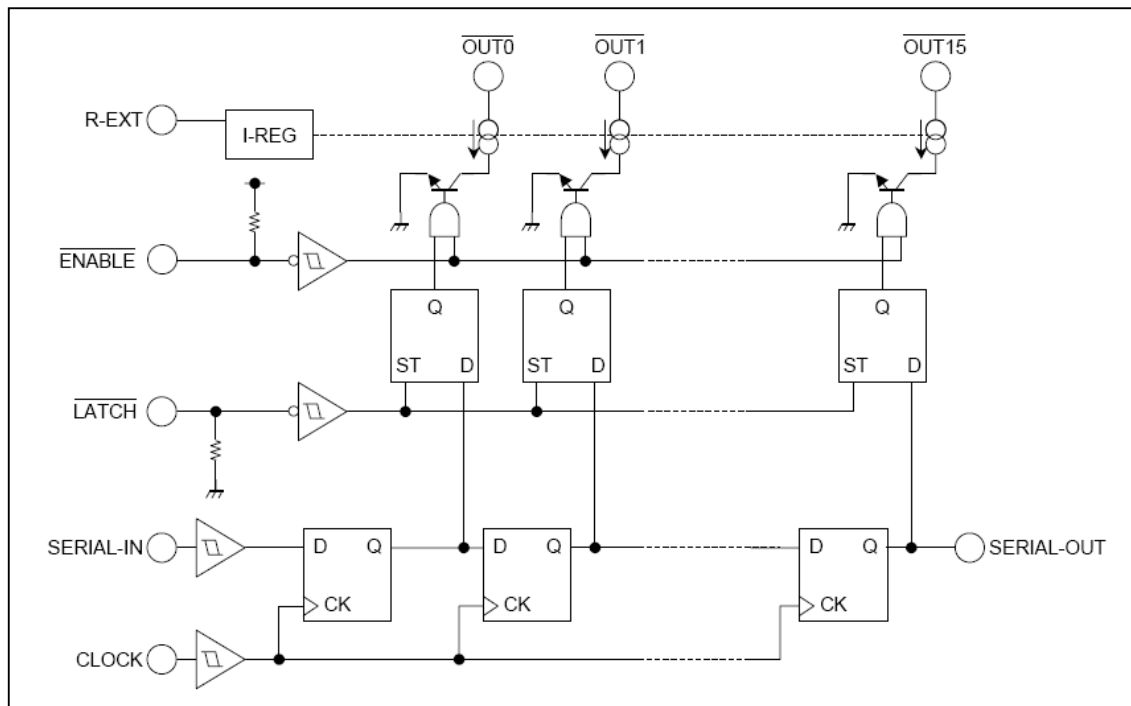


Figure 1 Block Diagram

## TYPICAL APPLICATION CIRCUIT

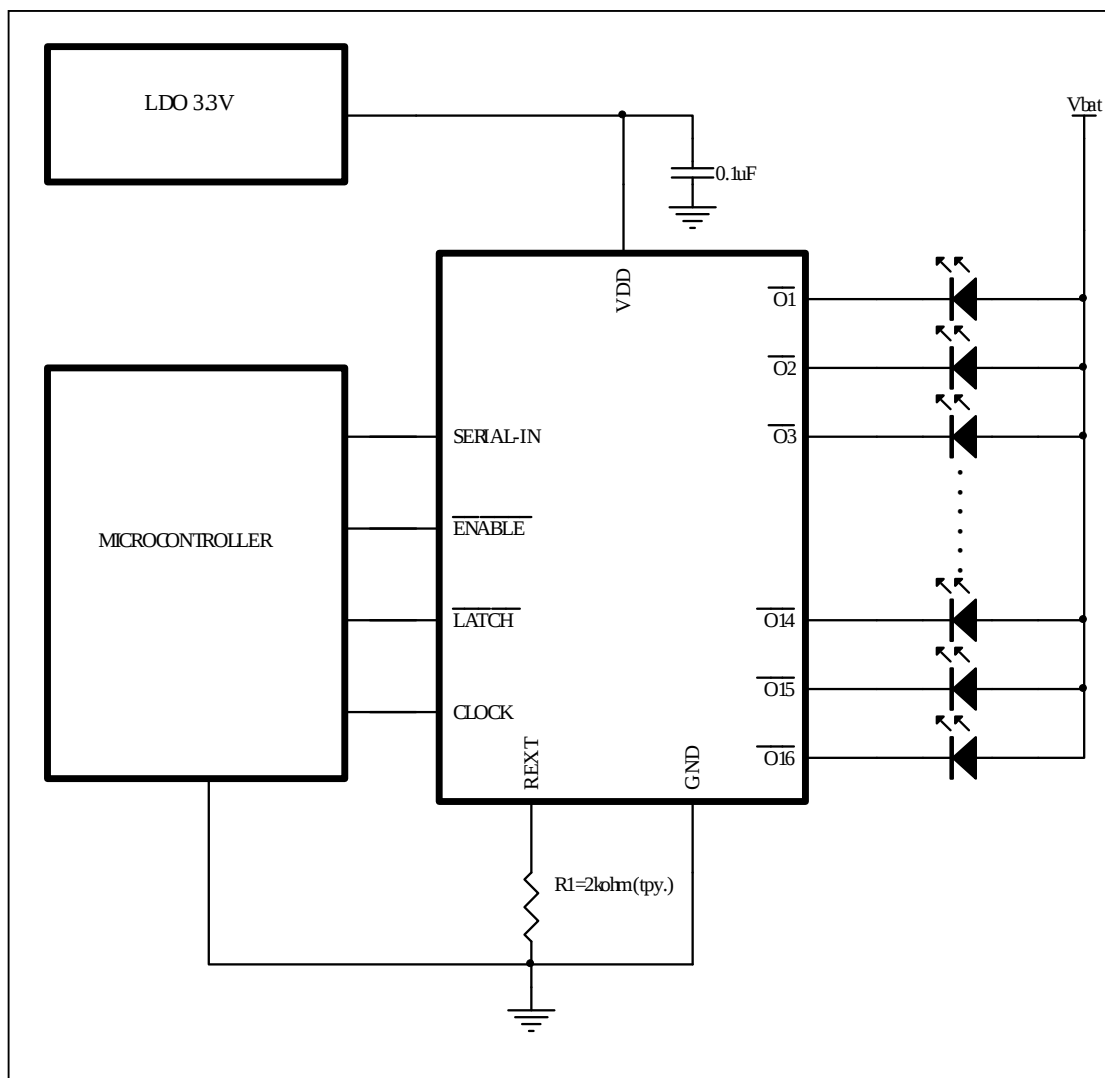
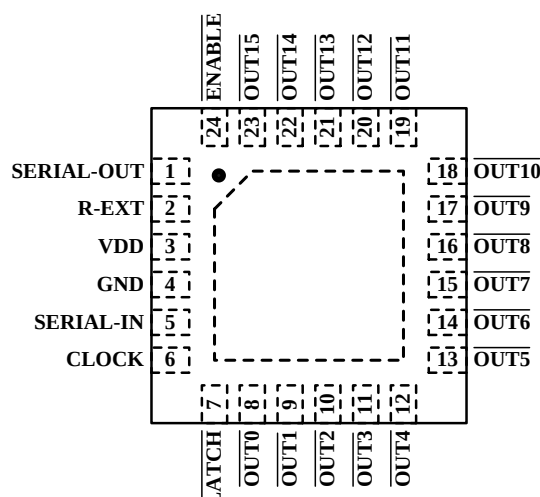
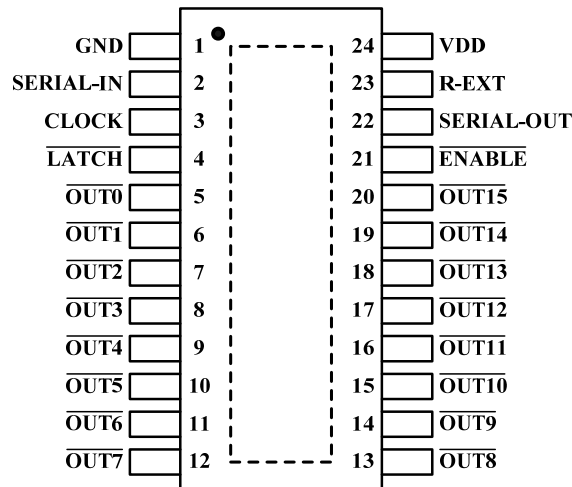


Figure 2 Typical Application Figure

# IS31FL3726

## PIN CONFIGURATION

| Package  | Pin Configuration (Top View)                                                        |
|----------|-------------------------------------------------------------------------------------|
| QFN-24   |   |
| TSSOP-24 |  |

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## PIN DESCRIPTION

| No.    |       | Pin                        | Description                                                                                                                                                                                                                                 |
|--------|-------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFN    | TSSOP |                            |                                                                                                                                                                                                                                             |
| 1      | 22    | SERIAL-OUT                 | Output terminal for serial data input on SERIAL-IN terminal.                                                                                                                                                                                |
| 2      | 23    | R-EXT                      | Input terminal used to connect an external resistor. This regulated the output current.                                                                                                                                                     |
| 3      | 24    | VDD                        | Supply voltage terminal.                                                                                                                                                                                                                    |
| 4      | 1     | GND                        | GND terminal for control logic.                                                                                                                                                                                                             |
| 5      | 2     | SERIAL-IN                  | Input terminal for serial data for data shift register.                                                                                                                                                                                     |
| 6      | 3     | CLOCK                      | Input terminal for clock for data shift on rising edge.                                                                                                                                                                                     |
| 7      | 4     | $\overline{\text{LATCH}}$  | Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low , data is latched.                                                                                       |
| 8 ~ 23 | 5~20  | OUT0~OUT15                 | Constant-current output terminals.                                                                                                                                                                                                          |
| 24     | 21    | $\overline{\text{ENABLE}}$ | Input terminal for output enable.<br>All outputs ( $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ ) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High .And are turned on, when the terminal is driven Low. |
|        |       | Thermal Pad                | Connect to GND.                                                                                                                                                                                                                             |



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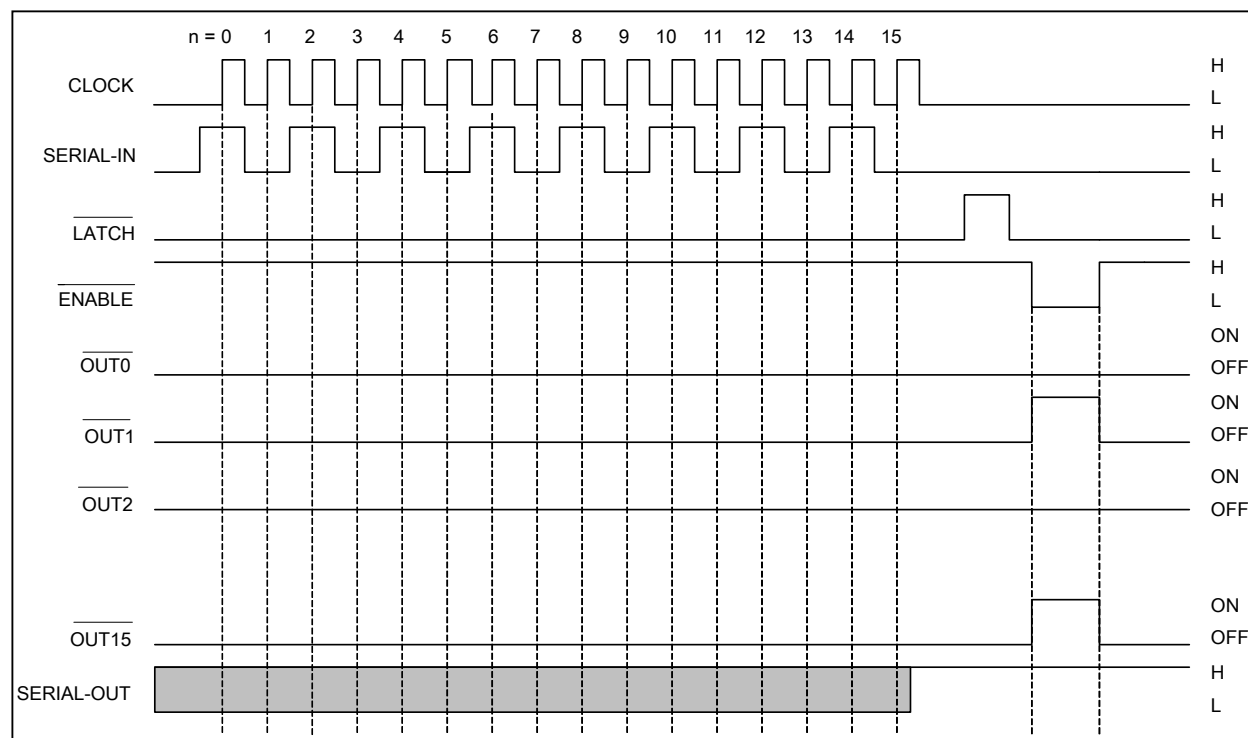
## ORDERING INFORMATION

**Industrial Range: -40°C to +85°C**

| Order Part No.      | Package             | QTY/Reel  |
|---------------------|---------------------|-----------|
| IS31FL3726-QFLS2-TR | QFN-24, Lead-free   | 2500/Reel |
| IS31FL3726-ZLS2-TR  | TSSOP-24, Lead-free | 2500/Reel |
| IS31FL3726-ZLS2     |                     | 62/Tube   |

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**Figure 3** Timing Diagram

**Warning:** Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

**Note :** The latches circuit holds data by pulling the **L A T C H** terminal Low. And, when **L A T C H** terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output. When **E N A B L E** terminal is a Low level, output terminal **O U T 0** to **O U T 1 5** respond to the data, and on and off does. And, when **E N A B L E** terminal is a High level, it offs with the output terminal regardless of the data.

## Truth Table

| CLOCK | LATCH | ENABLE | SERIAL-IN | OUT0 ...OUT7 ... OUT15 | SERIAL-OUT |
|-------|-------|--------|-----------|------------------------|------------|
|       | H     | L      | Dn        | Dn ...Dn-7 ...Dn-15    | Dn-15      |
|       | L     | L      | Dn+1      | No change              | Dn-14      |
|       | H     | L      | Dn+2      | Dn+2 ...Dn-5 ...Dn-13  | Dn-13      |
|       | X     | L      | Dn+3      | Dn+2 ...Dn-5 ...Dn-13  | Dn-13      |
|       | X     | H      | Dn+3      | OFF                    | Dn-13      |

**Note :** **OUT0** to **OUT15** =On when **Dn** = H; **OUT0** to **OUT15** =Off when **Dn** = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between **R-EXT** and **GND**.

**Warning:** The following conditions, **ENABLE=0**, **LATCH=1**, **SERIAL-IN=1**, cannot be configured at the same time when power on, or **IS31FL3726** will be abnormal.

# IS31FL3726

## ABSOLUTE MAXIMUM RATINGS

|                                          |                       |
|------------------------------------------|-----------------------|
| Supply voltage, $V_{DD}$                 | -0.3V ~ +6.0V         |
| Voltage at any input pin                 | -0.3V ~ $V_{DD}+0.2V$ |
| Maximum junction temperature, $T_{JMAX}$ | 150°C                 |
| Storage temperature range, $T_{STG}$     | -65°C ~ +150°C        |
| Operating temperature range, $T_A$       | -40°C ~ +85°C         |

### Note:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITION

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

| Symbol       | Characteristic                              | Condition                        | Min. | Typ. | Max. | Unit          |
|--------------|---------------------------------------------|----------------------------------|------|------|------|---------------|
| $V_{OUT}$    | Output voltage                              |                                  |      | 0.7  | 4    | V             |
| $f_{CLK}$    | Clock frequency (Note 1)                    | Cascade connected                |      |      | 20   | MHz           |
| $t_{WLAT}$   | $\overline{LATCH}$ pulse width              |                                  | 50   |      |      | ns            |
| $t_{WCLK}$   | CLOCK pulse width                           |                                  | 25   |      |      | ns            |
| $t_{WENA}$   | $\overline{ENABLE}$ pulse width (Note 1,2)  | Upper<br>$I_{OUT} = 20\text{mA}$ | 20   |      |      | $\mu\text{s}$ |
|              |                                             | Lower<br>$I_{OUT} = 20\text{mA}$ | 20   |      |      |               |
| $t_{SETUP1}$ | Set-up time for CLOCK terminal              |                                  | 10   |      |      | ns            |
| $t_{HOLD}$   | Hold time for CLOCK terminal                |                                  | 10   |      |      | ns            |
| $t_{SETUP2}$ | Set-up time for $\overline{LATCH}$ terminal |                                  | 50   |      |      | ns            |

**Note 1:** Guaranteed by design.

**Note 2:** When the pulse of the Low level is input to the  $\overline{ENABLE}$  terminal held in the High level.

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## ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3V ~ 5.5V, unless otherwise specified.

| Symbol                | Characteristic                           | Condition                                         |                         | Min. | Typ. | Max. | Unit |
|-----------------------|------------------------------------------|---------------------------------------------------|-------------------------|------|------|------|------|
| V <sub>DD</sub>       | Supply voltage                           | Normal operation                                  |                         | 3.3  |      | 5.5  | V    |
| I <sub>OUT1</sub>     | Output current                           | V <sub>OUT</sub> = 0.4V<br>V <sub>DD</sub> = 3.3V | R <sub>EXT</sub> = 1kΩ  | 15   | 18.7 | 22   | mA   |
| I <sub>OUT2</sub>     |                                          | V <sub>OUT</sub> = 0.4V<br>V <sub>DD</sub> = 5.5V |                         | 15   | 18.9 | 22   |      |
| ΔI <sub>OUT1</sub>    | Output current error between bits        | V <sub>OUT</sub> ≥0.4V,<br>All outputs on         | R <sub>EXT</sub> = 1kΩ  |      | ±3   | ±4   | %    |
| I <sub>OZ</sub>       | Output leakage current input voltage     | V <sub>OUT</sub> = 5.0V                           |                         |      |      | 1    | uA   |
| V <sub>IH</sub>       | Input voltage                            |                                                   |                         | 1.4  |      |      | V    |
| V <sub>IL</sub>       |                                          |                                                   |                         |      |      | 0.4  |      |
| V <sub>OL</sub>       | SOUT terminal voltage                    | I <sub>OL</sub> = 1.0mA, V <sub>DD</sub> = 3.3V   |                         |      |      | 0.3  | V    |
|                       |                                          | I <sub>OL</sub> = 1.0mA, V <sub>DD</sub> = 5V     |                         |      |      | 0.3  |      |
| V <sub>OH</sub>       |                                          | I <sub>OH</sub> = -1.0mA, V <sub>DD</sub> = 3.3V  |                         | 3    |      |      |      |
|                       |                                          | I <sub>OH</sub> = -1.0mA, V <sub>DD</sub> = 5V    |                         | 4.7  |      |      |      |
| %/V <sub>DD</sub>     | Output current supply voltage regulation | When V <sub>DD</sub> is changed 3.3V to 5.5V      |                         |      | -1   |      | %    |
| R <sub>(Up)</sub>     | Pull-up resistor                         | ENABLE terminal                                   |                         | 250  | 500  | 750  | kΩ   |
| R <sub>(Down)</sub>   | Pull-down resistor                       | LATCH terminal                                    |                         |      |      |      |      |
| I <sub>DD(OFF)1</sub> | Supply current                           | V <sub>OUT</sub> = 5V                             | R <sub>EXT</sub> = OPEN |      | 1    |      | mA   |
| I <sub>DD(OFF)2</sub> |                                          | V <sub>OUT</sub> = 5V<br>All outputs off          | R <sub>EXT</sub> = 1kΩ  |      | 4.5  |      |      |
| I <sub>DD(ON)1</sub>  |                                          | V <sub>OUT</sub> = 0.7V<br>All outputs on         | R <sub>EXT</sub> = 1kΩ  |      | 5    |      |      |

# IS31FL3726

## SWITCHING CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

| Symbol     | Characteristic          | Condition                                                                    | Min. | Typ. | Max. | Unit |
|------------|-------------------------|------------------------------------------------------------------------------|------|------|------|------|
| $t_{pLH1}$ | Propagation delay       | $\text{CLK-OUTn}, \text{LATCH} = \text{"H"}$<br>$\text{ENABLE} = \text{"L"}$ |      | 80   | 200  | ns   |
| $t_{pLH2}$ |                         | $\text{LATCH-OUTn}, \text{ENABLE} = \text{"L"}$                              |      | 80   | 200  |      |
| $t_{pLH3}$ |                         | $\text{ENABLE-OUTn}, \text{LATCH} = \text{"H"}$                              |      | 2000 |      |      |
| $t_{pLH}$  |                         | CLK-SERIAL OUT                                                               | 3    | 5    |      |      |
| $t_{pHL1}$ |                         | $\text{CLK-OUTn}, \text{LATCH} = \text{"H"}$<br>$\text{ENABLE} = \text{"L"}$ |      | 160  | 250  |      |
| $t_{pHL2}$ |                         | $\text{LATCH-OUTn}, \text{ENABLE} = \text{"L"}$                              |      | 160  | 250  |      |
| $t_{pHL3}$ |                         | $\text{ENABLE-OUTn}, \text{LATCH} = \text{"H"}$                              |      | 200  | 350  |      |
| $t_{pLH}$  |                         | CLK-SERIAL OUT                                                               | 4    | 6    |      |      |
| $t_{or}$   | Output rise time        | 10%~90% of voltage waveform                                                  | 30   | 150  | 200  | ns   |
| $t_{of}$   | Output fall time        | 90%~10% of voltage waveform                                                  | 150  | 200  | 250  | ns   |
| $t_r$      | Maximum CLOCK rise time | When not on PCB (Note)                                                       |      |      | 5    | us   |
| $t_f$      | Maximum CLOCK fall time |                                                                              |      |      | 5    | us   |

**Conditions:** (Refer to test circuit.)

$T_{opr} = 25^\circ\text{C}$ ,  $V_{DD} = V_{IH} = 3.3\text{V}$  and  $5\text{V}$ ,  $V_{OUT} = 0.7\text{V}$ ,  $V_{IL} = 0\text{V}$ ,  $R_{EXT} = 1000\Omega$ ,  $V_L = 3.0\text{V}$ ,  $R_L = 60\Omega$ ,  $C_L = 10.5\text{pF}$

### Note:

1. If the device is connected in a cascade and  $t_r/t_f$  for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.
2. Delay between outputs. The IS31FL3726 has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), OUT1 has 5ns delay, OUT2 has 10 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before  $\text{ENABLE}$  is low will still turn on and off at the determined delayed time regardless of the state of  $\text{ENABLE}$ . Therefore, every LED will be illuminated for the amount of time  $\text{ENABLE}$  is pulled high.

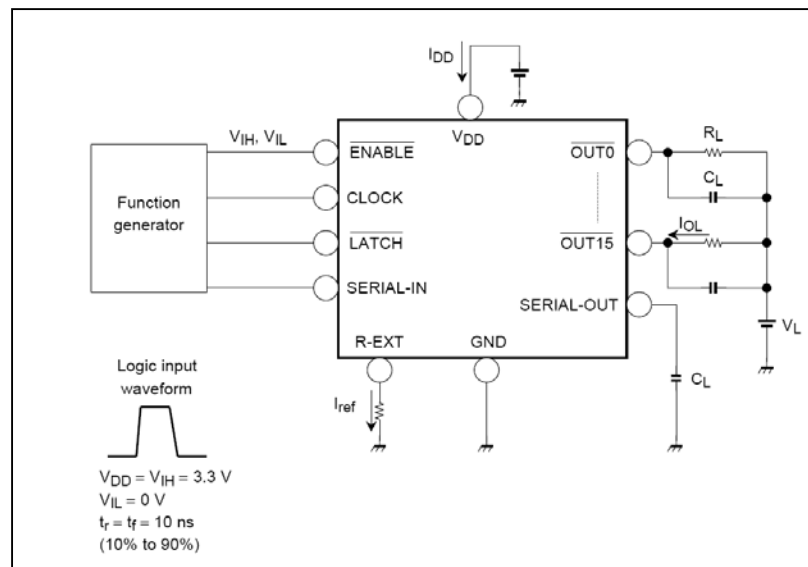
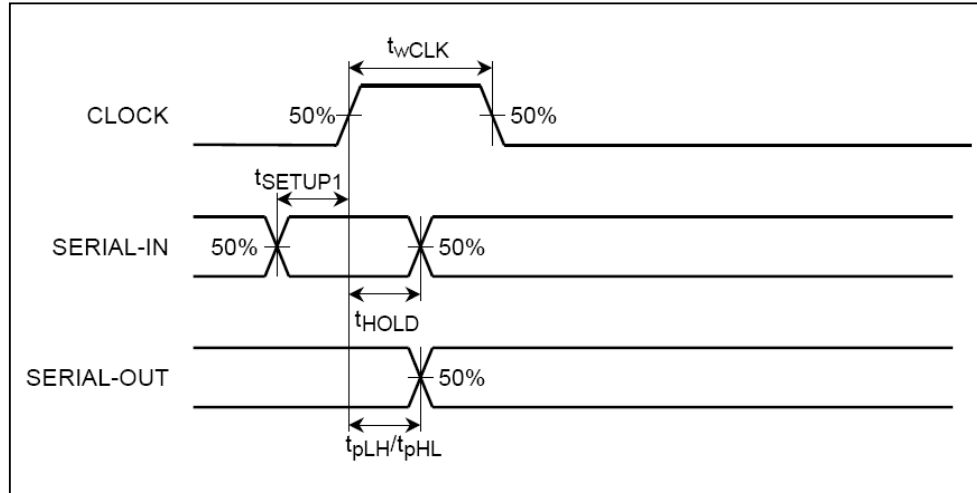


Figure 4 Test Diagram

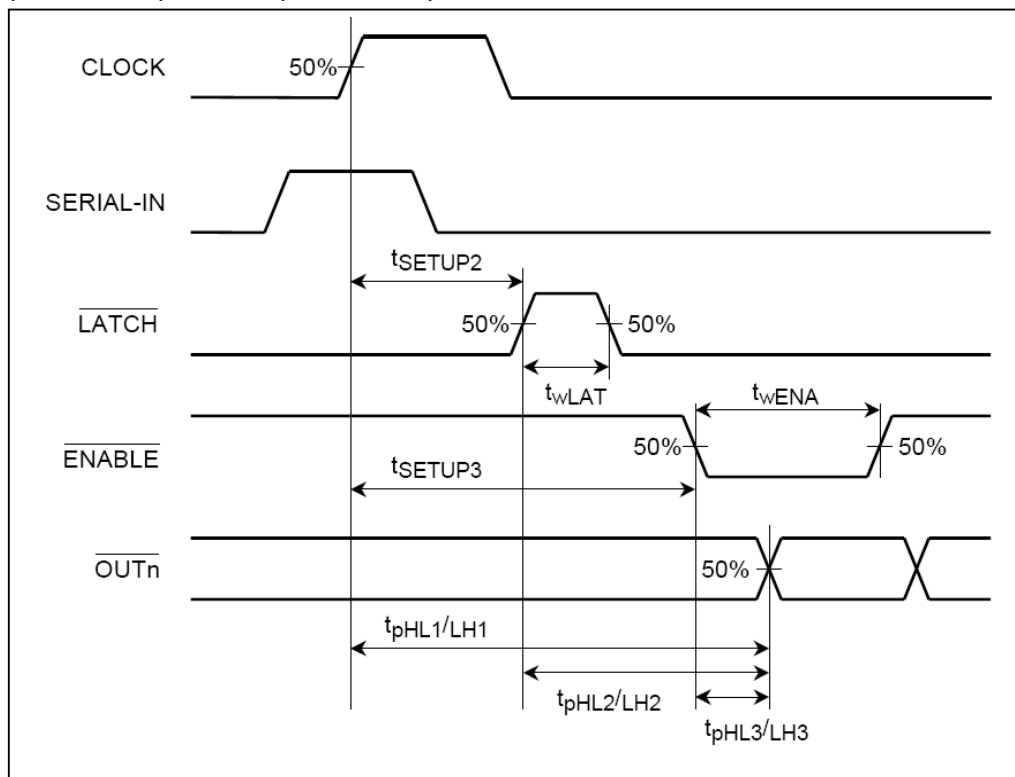
# IS31FL3726

## TIMING WAVEFORM

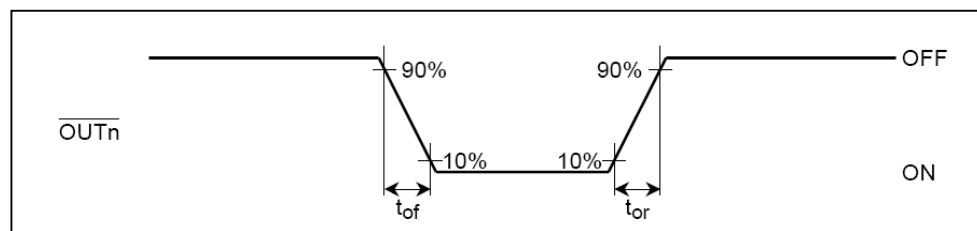
### 1. CLOCK, SERIAL-IN, SERIAL-OUT



### 2. CLOCK, SERIAL-IN, LATCH, ENABLE, OUTn



### 3. OUTn



# IS31FL3726

## TYPICAL OPERATING CHARACTERISTICS

### ADJUSTING OUTPUT CURRENT

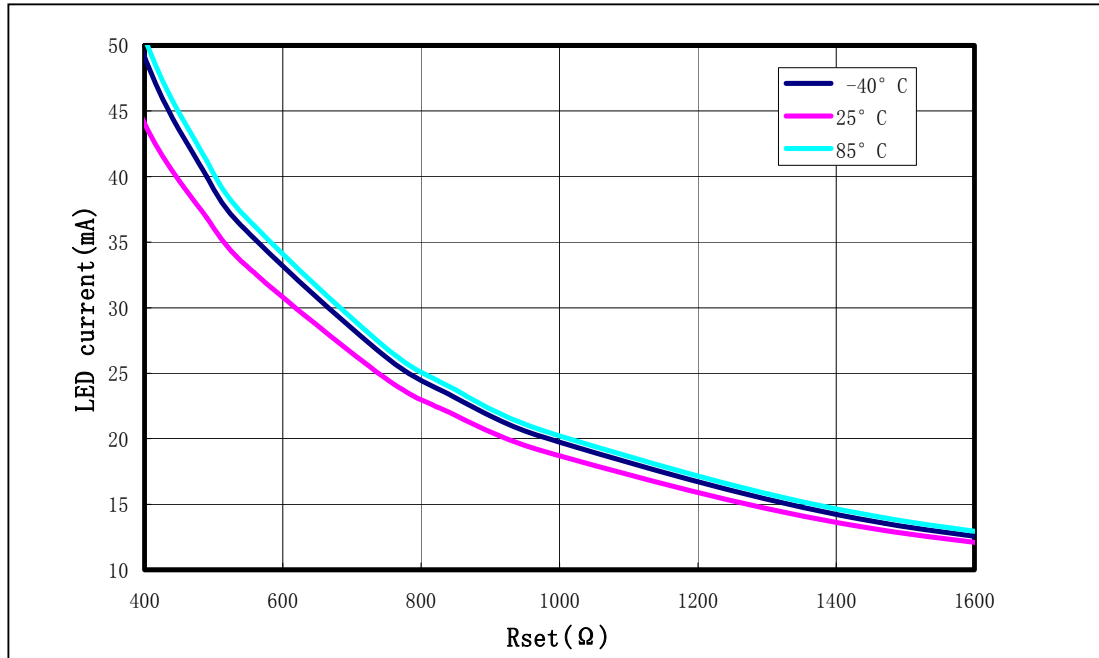
The output current of each channel is set by an external resistor  $R_{ext}$ , the relationship between  $I_{out}$  and  $R_{ext}$  is:

$$I_{out} = (V_{R-ext}/R_{ext}) \times 52$$

the  $V_{R-ext}$  is 0.36V in the IS31FL3726,so we can count the  $I_{out}$  as :

$$I_{out} = 0.36 \times 52 / R_{ext}$$

As show in the figure below:



# IS31FL3726

## CLASSIFICATION REFLOW PROFILES

| Profile Feature                                                                                                                                                    | Pb-Free Assembly                 |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Preheat & Soak<br>Temperature min (T <sub>smin</sub> )<br>Temperature max (T <sub>smax</sub> )<br>Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> ) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )                                                                                                        | 3°C/second max.                  |
| Liquidous temperature (T <sub>L</sub> )<br>Time at liquidous (t <sub>L</sub> )                                                                                     | 217°C<br>60-150 seconds          |
| Peak package body temperature (T <sub>p</sub> )*                                                                                                                   | Max 260°C                        |
| Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )                                                                  | Max 30 seconds                   |
| Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )                                                                                                      | 6°C/second max.                  |
| Time 25°C to peak temperature                                                                                                                                      | 8 minutes max.                   |

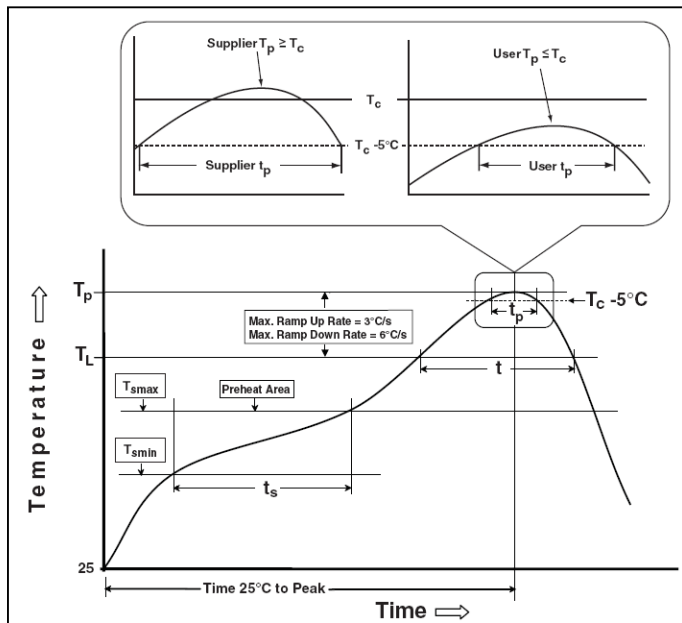
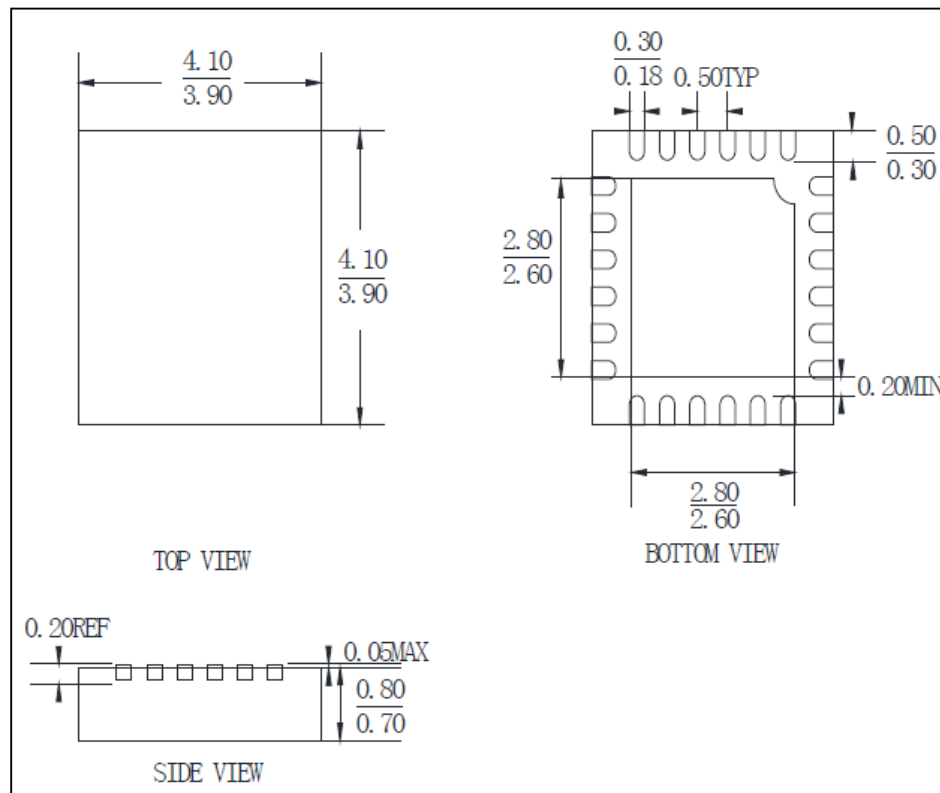


Figure 5 Classification Profile

**IS31FL3726**

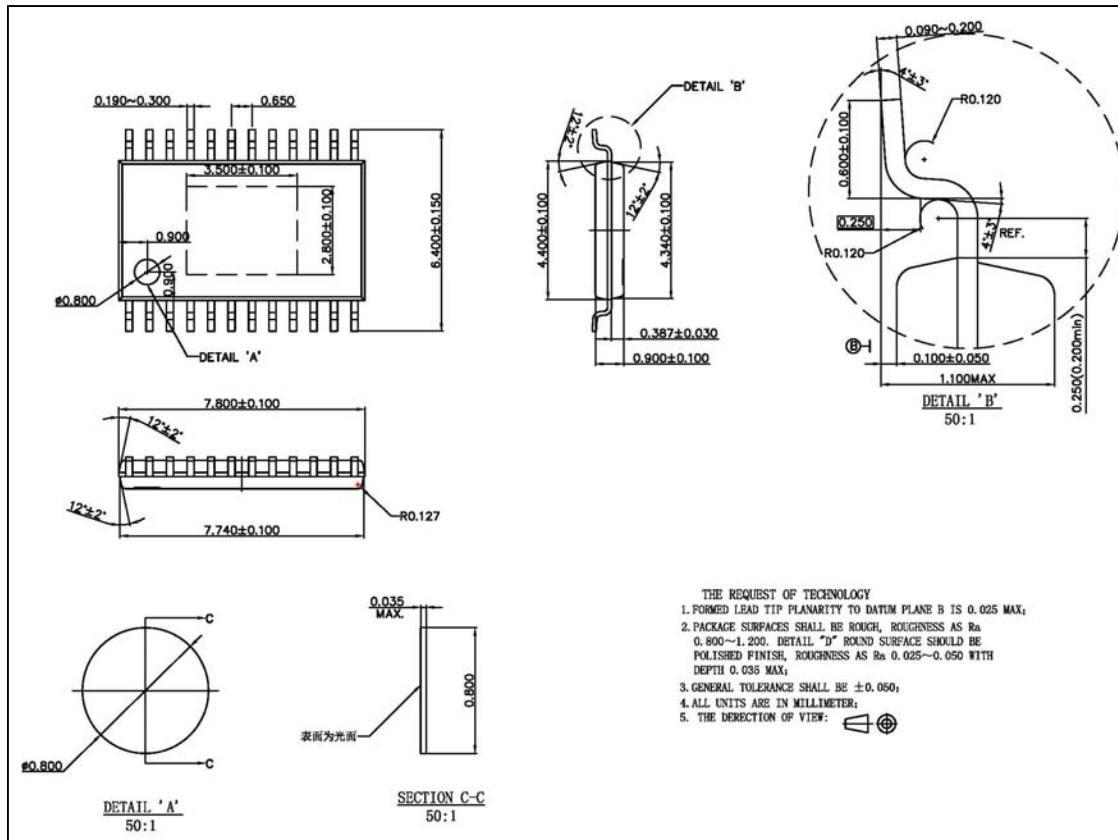
## PACKAGE INFORMATION

**QFN-24**



**Note:** All dimensions in millimeters unless otherwise stated.

## TSSOP-24



**Note:** All dimensions in millimeters unless otherwise stated.