Murata Power Solutions

S020_084-S020-00

12.0V input, 1.2 to 5.0V adjustable output, 20A or 55W

Features

- High output 20A up to 55W max
- 12V +5/-10% input
- Load Regulation ±0.5%
- Factory set to 1.2V output with output trim up to 5.0V
- High Efficiency to 93%
- Power Good and Enable
- Short Circuit protection
- MTBF 3.0 million hours
- Can sink 8A current, maintaining output regulation
- Back Bias protection

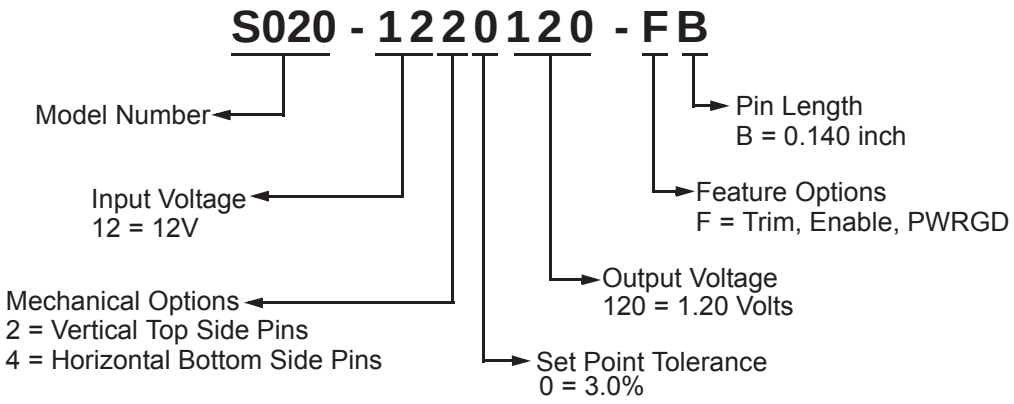
NOT RECOMMENDED FOR NEW DESIGNS

This product is not fuse protected. User is responsible for providing system protection. Consult factory for application information.

Specifications *	S020	
Input Specifications		
Input voltage range	12.0V +5/-10%	Measured at +Vin pin
External input capacitor	Input capacitor capable of ripple current	See ripple current curve on pg 6 and Input and Output Capacitance table on pg 8
Output Specifications		
Standard output voltages and output current	1.2V, 20A	Regulation range is ± 3% including output voltage set point, line regulation and load regulation over the operating temperature range. See DC Voltage Regulation table on pg 6 for trimming to different voltages
	1.25V, 20A	
	1.5V, 20A	
	1.8V, 20A	
	2.5V, 16A	
	3.3V, 13A	
	5.0V, 11A	
Load regulation	±0.5%	0 to 20A load
Line regulation	±0.4%	12.0V input voltage range
External output capacitor	820µF OSCON or equivalent with ESR < 12mΩ	See also Input and Output Capacitance table on pg 8
Short circuit protection	200% of maximum rated current	Autorecovery
General Specifications		
Enable **	ON-high / OFF-low	
Efficiency @ Full Load	93.6% @ 5V	See chart on pg 4.
Isolation	Non-isolated	
Switching frequency	300kHz	Fixed
Approvals and Standards	UL 94V-0	
Protection	Fusing	Unit is not fused.
Operating Temperature ***	0°C to 50°C	
Storage Temperature	-40°C to 70°C	Non-condensing
Weight	0.25 oz	
MTBF	1.9 million hours	Per RAC PRISM at 50°C ambient and 300 LFM

* All specifications are typical at nominal input, full load at 25°C unless otherwise stated.
** Pull below 0.35V to disable the SIP; pull above 2.4V (do not exceed 5.5V) to enable the SIP.
*** The output capacitors must meet the max ESR <12 mΩ requirement over the operating temperature range.

Ordering Information



Pin Assignments

CONNECTOR	PIN	FUNCTION	CONNECTOR	PIN	FUNCTION
J1	1	V_{OUT}	J1	6	PWRGD
	2	V_{OUT}		7	Ground
	3	V_{OUT}		8	Ground
	4	Trim		9	PWRGD_SET
	5	Enable		10	V_{IN}
				11	V_{IN}

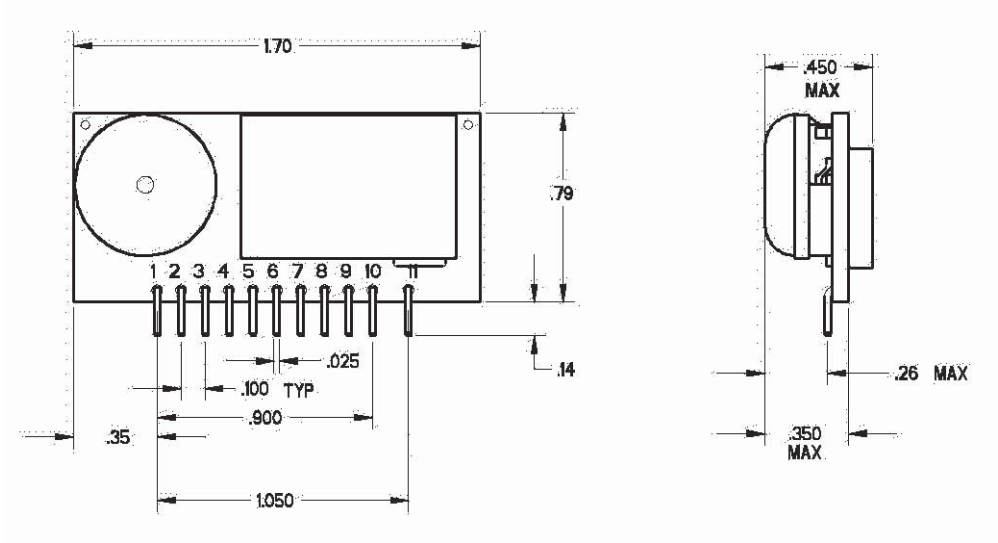
Set Point Resistor Table

Ambient conditions: 400 LFM and 50°C			
Output Set Resistor	**Output Current Rating (Amps)**	**Output Voltage**	**PWRGD Set Resistor**
Open	20	1.20	Open
23.7 kΩ	20	1.25	169 kΩ
3.92 kΩ	20	1.50	26.1 kΩ
1.96 kΩ	20	1.80	11.8 kΩ
909 Ω	16	2.50	4.22 kΩ
562 Ω	13	3.30	1.78 kΩ
309 Ω	11	5.00	0.00 Ω (short)

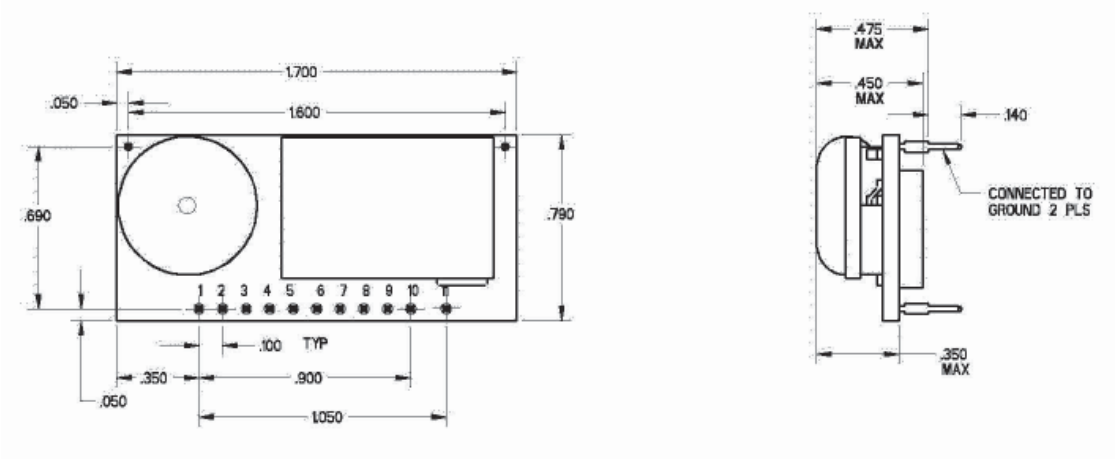
The output voltage is set by applying the correct output set resistor per above table between the Trim Pin & Ground.

Outline Drawings

Vertical Mount Option (S020-1220120-FB)



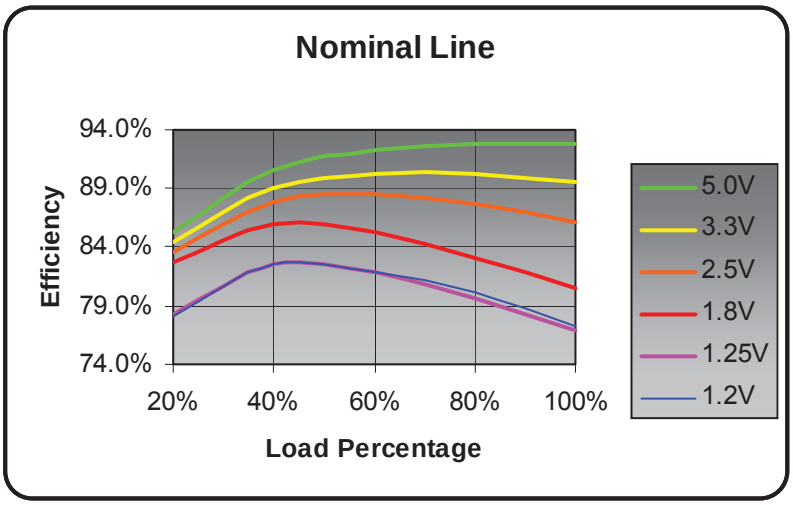
Horizontal Mount Option (S020-1240120-FB)



1. Dimensions are in inches and (millimeters).
2. Tolerances: (unless otherwise noted)

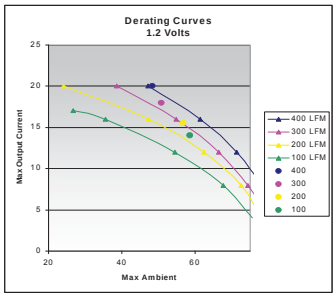
	Inches	Millimeters
	.XX ± .020	.X ± 0.5
	.XXX ± .010	.XX ± 0.25
Pin:	± .002	± 0.05

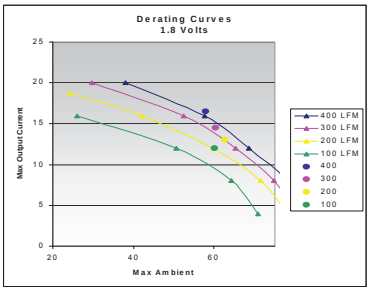
Efficiency Curves at 25°C

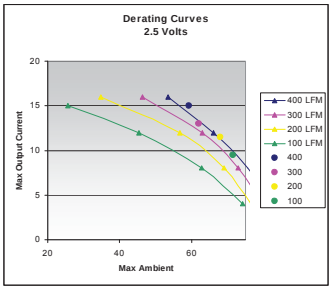


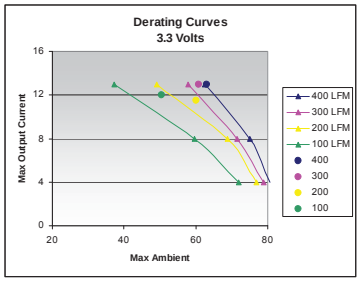
LOAD (%)	1.2 Vout	1.25 Vout	1.8 Vout	2.5 Vout	3.3 Vout	5.0 Vout
20%	78.1%	78.2%	82.7%	83.6%	84.3%	85.2%
40%	82.6%	82.5%	86.0%	87.9%	89.0%	90.6%
60%	81.9%	81.8%	85.2%	88.5%	90.3%	92.3%
80%	80.1%	79.7%	83.1%	87.8%	90.2%	92.9%
100%	77.2%	76.9%	80.6%	86.1%	89.6%	92.9%

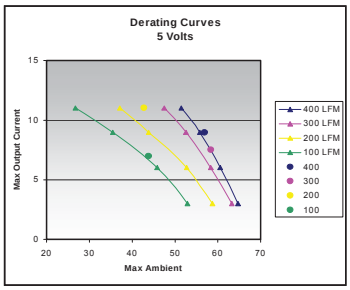
Derating Curves











PWRGD - Power Good Signal

The power good signal will be asserted, driven high, by the converter to indicate that the output is valid. If the output fails the specified DC voltage regulation limits or the output is below 90% of the nominal voltage, then the PWRGD signal will be driven low.

The output is an open collector/drain. It is capable of driving the output below 0.4V with a load of 4mA.

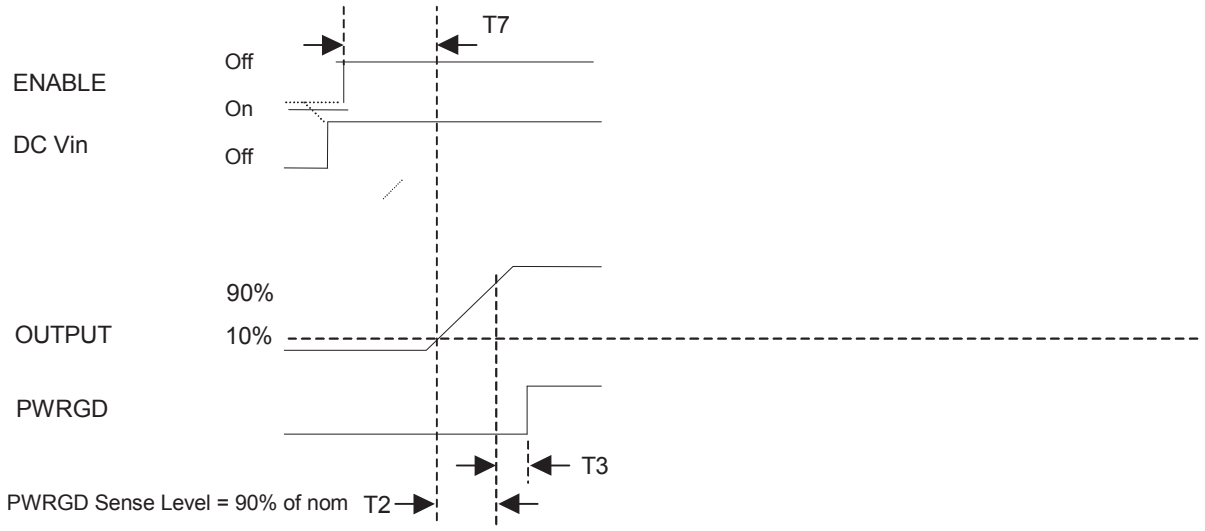
PWRGD_SET - Power Good Signal Levelset

The section sets the Power Good signal levels with a single resistor connected between the PWRGD_SET (Pin9) and Ground (Pin7). Note fault condition is Low signal on PWRGD_SET.

OUTPUT VOLTAGE	PWRGD_SET RESISTOR (1%tol)
5V	SHORT (Zero Ohm)
3.3V	1.78K
2.5V	4.22K
1.8V	11.8K
1.5V	30.1K
1.25V	169K
1.2V	Open

$$PWRGD\_Threshold := 6.19k \cdot \left(\frac{1.24}{2.21k + Rset} \quad 18.86\,10^{-6} \right) + 1.24$$

Logic Timings



Output Rise Time 0ms < T2 < 5ms
PWRGD Delay 0ms < T3 < 10ms
ENABLE-TO-OUTPUT DELAY0ms < T7 < 100ms

DC Voltage Regulation

The DC output voltages will remain within the regulation ranges shown in the following table when measured at the load end of the connector. Connect Set Resistor per table below from Trim (Pin4) to Ground (Pin7). Regulation range includes output voltage Set Point, Line Regulation & Load Regulation over the temperature range.

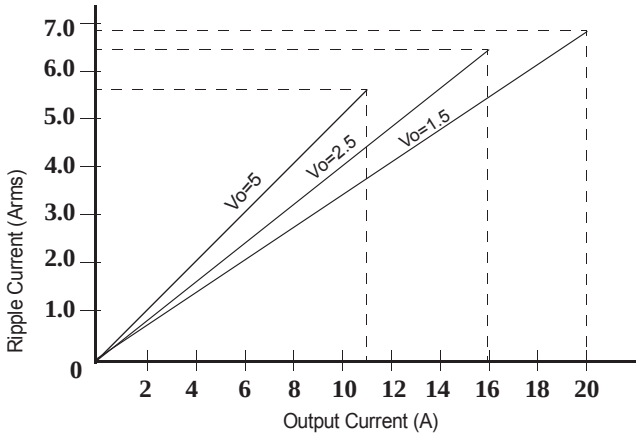
Output Level	Minimum	Maximum	Set Resistor (1%tol)
+5V	-3%	+3%	309Ω
+3.3V	-3%	+3%	562 Ω
+2.5V	-3%	+3%	909 Ω
+1.8V	-3%	+3%	1.96kΩ
1.5V	-3%	+3%	3.92kΩ
1.25V	-3%	+3%	23.7kΩ
1.2V	-3%	+3%	Open (no resistor)

The above regulations should be for all operating conditions.

$$V_o := \left(\frac{0.992}{5.62k} + \frac{0.992}{Rset} \right) 1.18k + 0.992$$

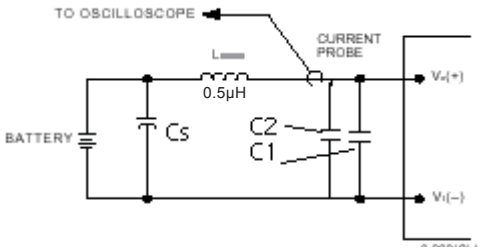
Input Ripple Current

Approximate ripple current ratings required for input bulk capacitor.



DC Input Reflected Ripple

Maximum reflected current ripple will not exceed 150mA (pk-pk) 5Hz to 20MHz per test setup indicated below.



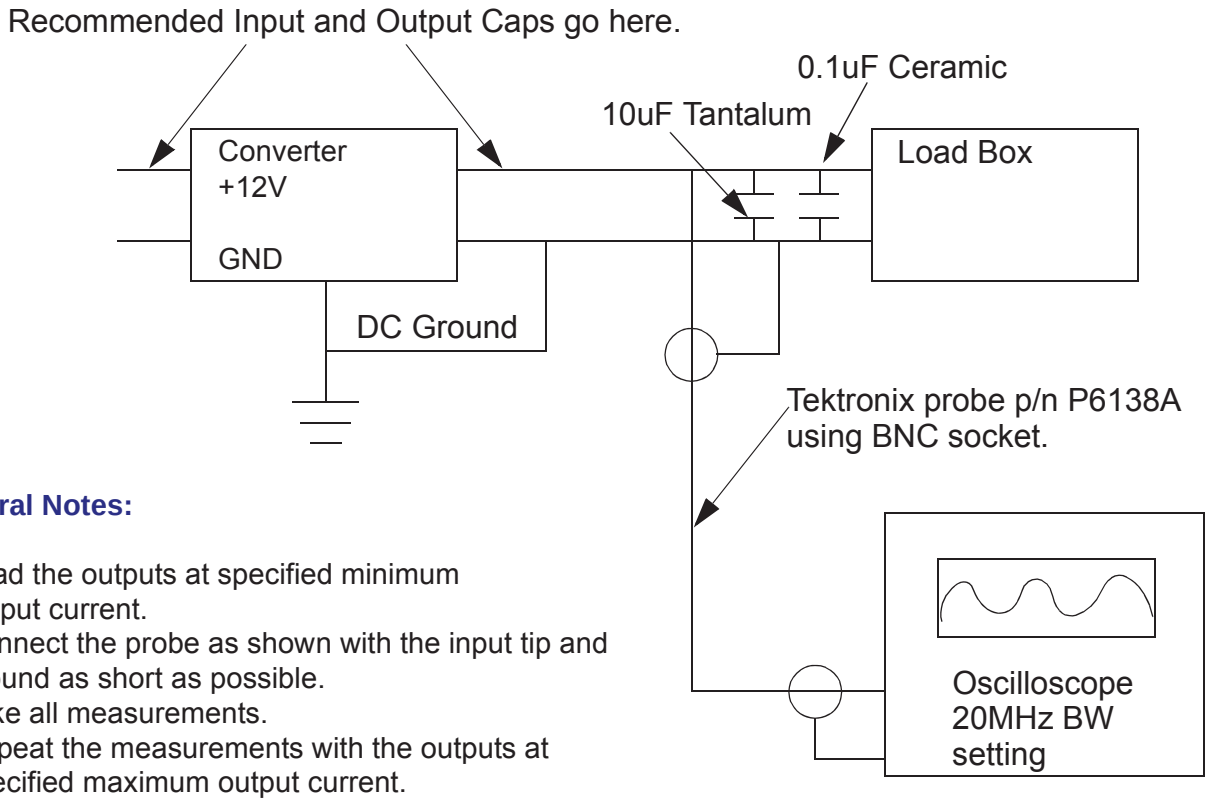
Ltest = 500nH Cs = 270µF Esr < 0.1 ohm at 100kHz 20°C
C1 = 270µF Esr < 0.02 ohm at 100kHz 20°C , C2 = 2µF ceramic
Tektronix current Probe P/N TCP202
Filter components should be mounted close to the module.

Output Ripple and Noise

The following output ripple/noise requirements will be met throughout the load ranges specified and under all input voltage conditions specified.

Output Level	Maximum	Unit
+5V	75mV	mV_{pp}
+3.3V	50mV	mV_{pp}
+2.5V	40mV	mV_{pp}
+1.8V	40mV	mV_{pp}
+1.5V	40mV	mV_{pp}
+1.25V	40mV	mV_{pp}
+1.2V	40mV	mV_{pp}

Ripple and noise are defined as periodic or random signals over the frequency band of 10Hz to 20MHz. Measurements will be made with an oscilloscope set to 20MHz bandwidth limit. Outputs will be tested per the following setup.



General Notes:

1. Load the outputs at specified minimum output current.
2. Connect the probe as shown with the input tip and ground as short as possible.
3. Take all measurements.
4. Repeat the measurements with the outputs at specified maximum output current.
5. The specification for maximum output ripple is not valid when the module is in a sinking mode. During sink the maximum peak-to-peak voltage limit is 2x the sourcing limit.

Input and Output Capacitance

The power supply requires the following capacitance (or equivalent) on the PWB.

Output Level	Output Capacitance *
+5V	One 680uF, 6.3V SP OSCON
+3.3V	One 820uF, 4V SP OSCON
+2.5V	One 820uF, 4V SP OSCON
+1.8V	One 820uF, 4V SP OSCON
+1.5	One 820uF, 4V SP OSCON
1.25V	One 820uF, 4V SP OSCON
1.2V	One 820uF, 4V SP OSCON
	Or equivalent. MBZ type AL-E caps or POSCAPs may be used instead.

* Output Ceramic Capacitance ≥ 60µF located close to the module

INPUT CAPACITANCE
Although input capacitance value is not critical, the input capacitors must be capable of storing fairly large amounts of energy. The primary criteria, though, for choosing the input capacitors is AC ripple current rating. The SIP datasheet contains a chart showing ripple current vs. output current (or output power). The system designer determines the maximum SIP output current required from the SIP. Based on that number, the chart will show a corresponding ripple current rating the designer needs to plan for when choosing input capacitors. Suggested capacitors are OSCONS, MBZ type AL-E or POSCAPS. It is advised that the ripple current capacity of the capacitor be derated to the estimated ambient temperature. Capacitors of at least 16V are necessary and the user should also place >22µF of ceramics close to the module.

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Output Transient Response (Dynamic Loading)

The output voltages will remain within their regulation limits specified for the load steps defined below. The maximum over/undershoot voltages will not exceed those defined below and will not cause any over or undervoltage detection circuits to activate. The load slew rate will not exceed 10A/µS. Recommended input and output capacitors should be used to meet the Spec.

Output Level	Maximum Load Step	Minimum Starting DC Load	Voltage Over/Undershoot
+5V	50%	0A	±4%
+3.3V	50%	0A	±5%
+2.5V	50%	0A	±5%
+1.8V	50%	0A	±7%
+1.5	50%	0A	±7%
1.25V	50%	0A	±10%
1.2V	50%	0A	±10%

Shock and Vibration

Vibration Test

Tri-axis random vibration (as generated by pneumatic hammer)

Typical vibration conditions:

Frequency Range:	Broadband
Vibration Levels:	20 to 55Grms
Step Dwell Time:	10-15 minutes
Final Dwell Time:	30-60 minutes
Unit Line Condition:	Nom Input voltage
Unit Load Condition:	Full Load Output

The UUT will survive any specified vibration level or 30Grms minimum without damage and performance will remain within specification limits during vibration testing

Shock Test

NON-OPERATING/SHIPPING
Drop/Impact

The power supply, in its individual shipping package, will be capable of withstanding the impacts specified in the International Safe Transit Association's Integrity Test Procedure 1A – Impact Test.

Test System:	Free Fall Drop Test System
Orientation:	Six (6) faces, three (3) edges, and one (1) corner
Drop Height:	Height levels determined by product weight (minimum 8 inches (150 lb.), maximum 30 inches (21 lb.))
Number of Drops:	Ten (10)

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