



FDV303N Digital FET, N-Channel

General Description

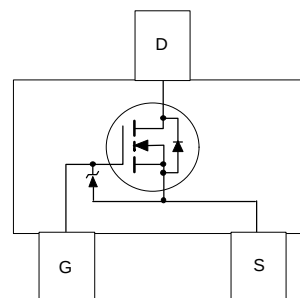
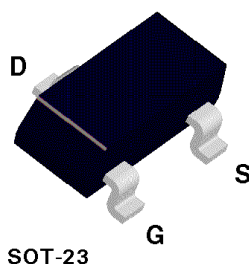
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance at low gate drive conditions. This device is designed especially for application in battery circuits using either one lithium or three cadmium or NMH cells. It can be used as an inverter or for high-efficiency miniature discrete DC/DC conversion in compact portable electronic devices like cellular phones and pagers. This device has excellent on-state resistance even at gate drive voltages as low as 2.5 volts.

Features

- 25 V, 0.68 A continuous, 2 A Peak.
 $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
 $R_{DS(ON)} = 0.6 \Omega @ V_{GS} = 2.7 V$
- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)} < 1V$.
- Gate-Source Zener for ESD ruggedness.>6kV Human Body Model
- Compact industry standard SOT-23 surface mount package.
- Alternative to TN0200T and TN0201T.



Mark:303



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless other wise noted

Symbol	Parameter	FDV303N	Units
V_{DSS}	Drain-Source Voltage, Power Supply Voltage	25	V
V_{GSS}	Gate-Source Voltage, V_{IN}	8	V
I_D	Drain/Output Current - Continuous	0.68	A
	- Pulsed	2	
P_D	Maximum Power Dissipation	0.35	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	$^\circ\text{C/W}$
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Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	25			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		26		mV / °C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V T _J = 55°C			1 10	μA μA
I _{GSS}	Gate - Body Leakage Current	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
ON CHARACTERISTICS (Note)						
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		-2.6		mV / °C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.65	0.8	1	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 4.5 V, I _D = 0.5 A T _J =125°C V _{GS} = 2.7 V, I _D = 0.2 A		0.33 0.52 0.44	0.45 0.8 0.6	Ω
I _{D(ON)}	On-State Drain Current	V _{GS} = 2.7 V, V _{DS} = 5 V	0.5			A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 0.5 A		1.45		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz		50		pF
C _{oss}	Output Capacitance			28		pF
C _{rss}	Reverse Transfer Capacitance			9		pF
SWITCHING CHARACTERISTICS (Note)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = 6 V, I _D = 0.5 A, V _{GS} = 4.5 V, R _{GEN} = 50 Ω		3	6	ns
t _r	Turn - On Rise Time			8.5	18	ns
t _{D(off)}	Turn - Off Delay Time			17	30	ns
t _f	Turn - Off Fall Time			13	25	ns
Q _g	Total Gate Charge	V _{DS} = 5 V, I _D = 0.5 A, V _{GS} = 4.5 V		1.64	2.3	nC
Q _{gs}	Gate-Source Charge			0.38		nC
Q _{gd}	Gate-Drain Charge			0.45		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				0.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.5 A (Note)		0.83	1.2	V

Note:

Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

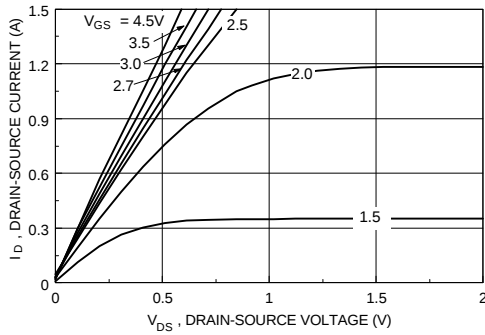


Figure 1. On-Region Characteristics.

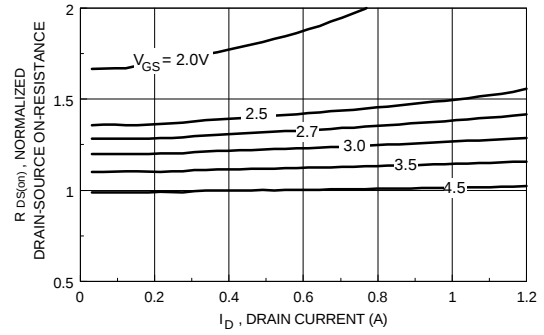


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

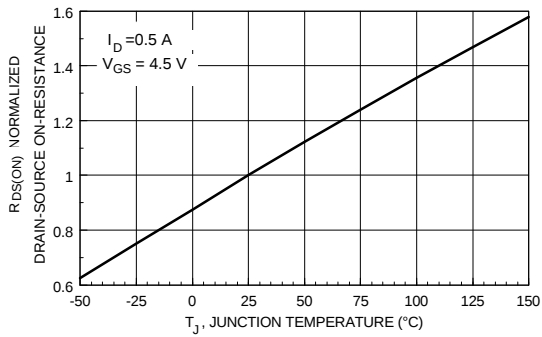


Figure 3. On-Resistance Variation with Temperature.

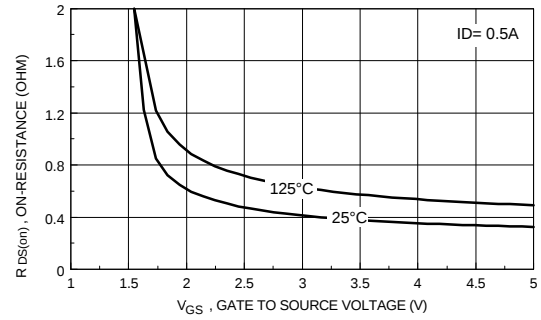


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

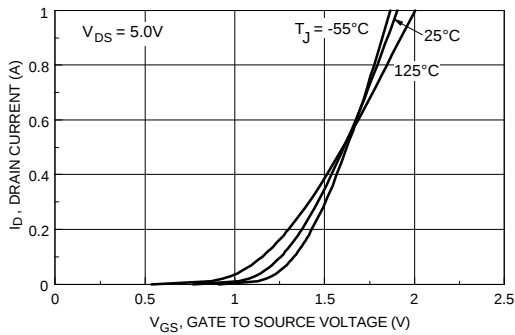


Figure 5. Transfer Characteristics.

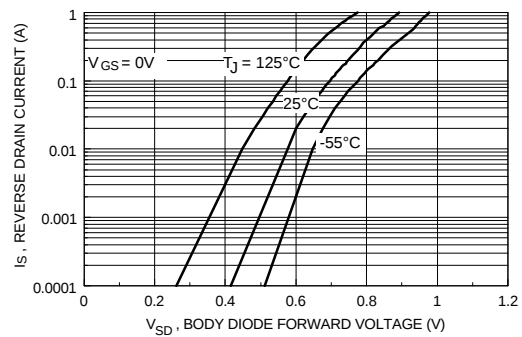


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

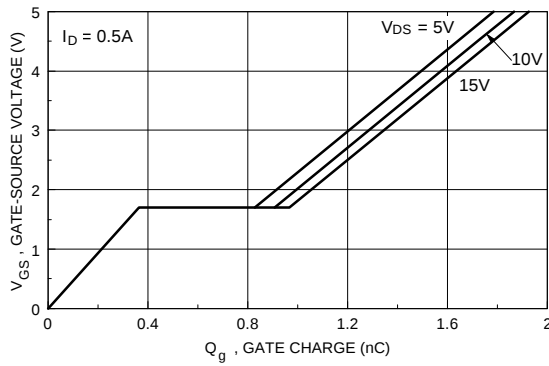


Figure 7. Gate Charge Characteristics.

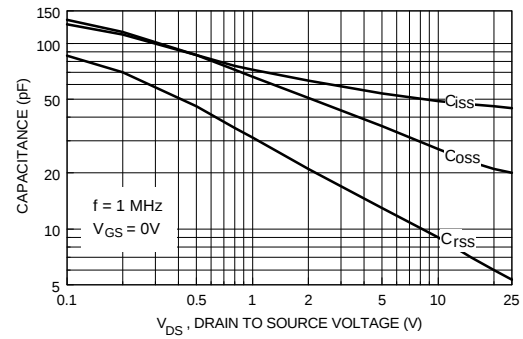


Figure 8. Capacitance Characteristics.

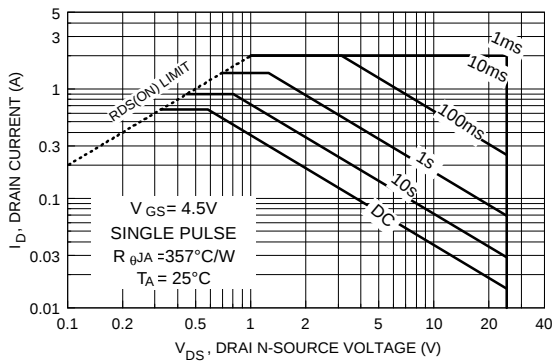


Figure 9. Maximum Safe Operating Area.

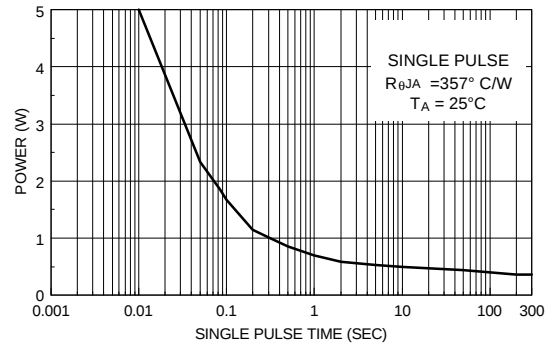


Figure 10. Single Pulse Maximum Power Dissipation.

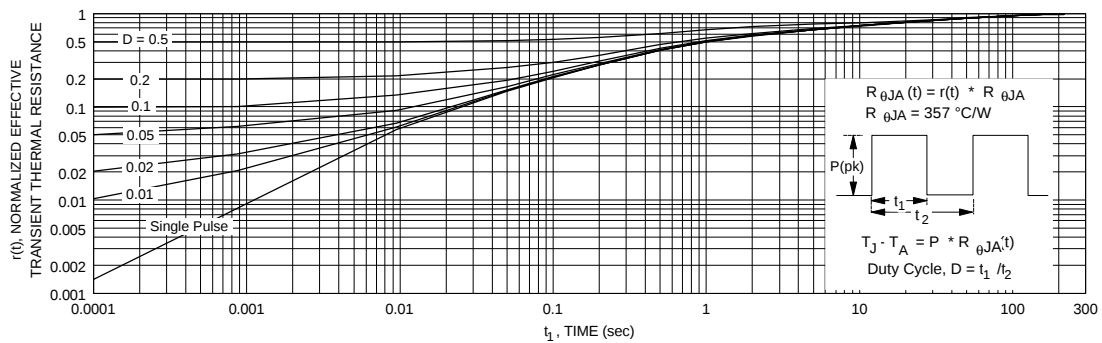
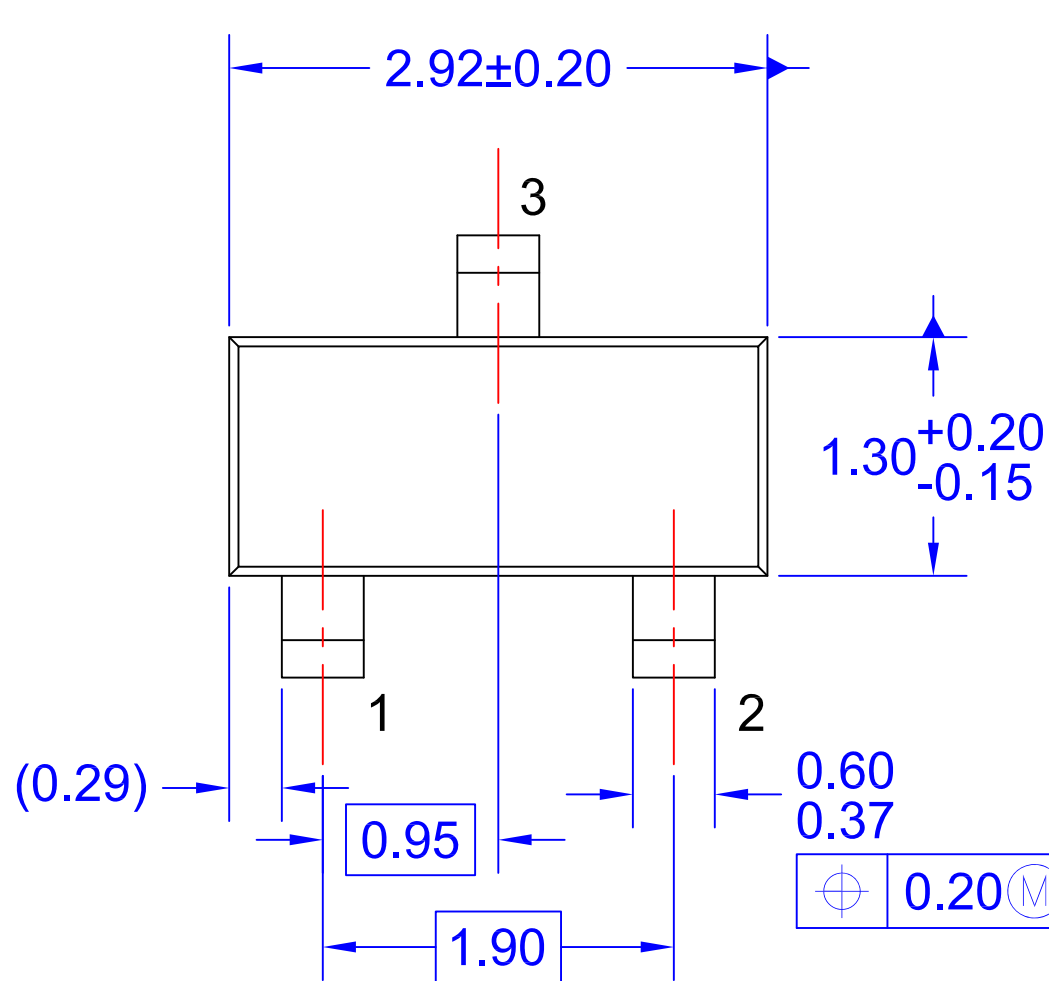
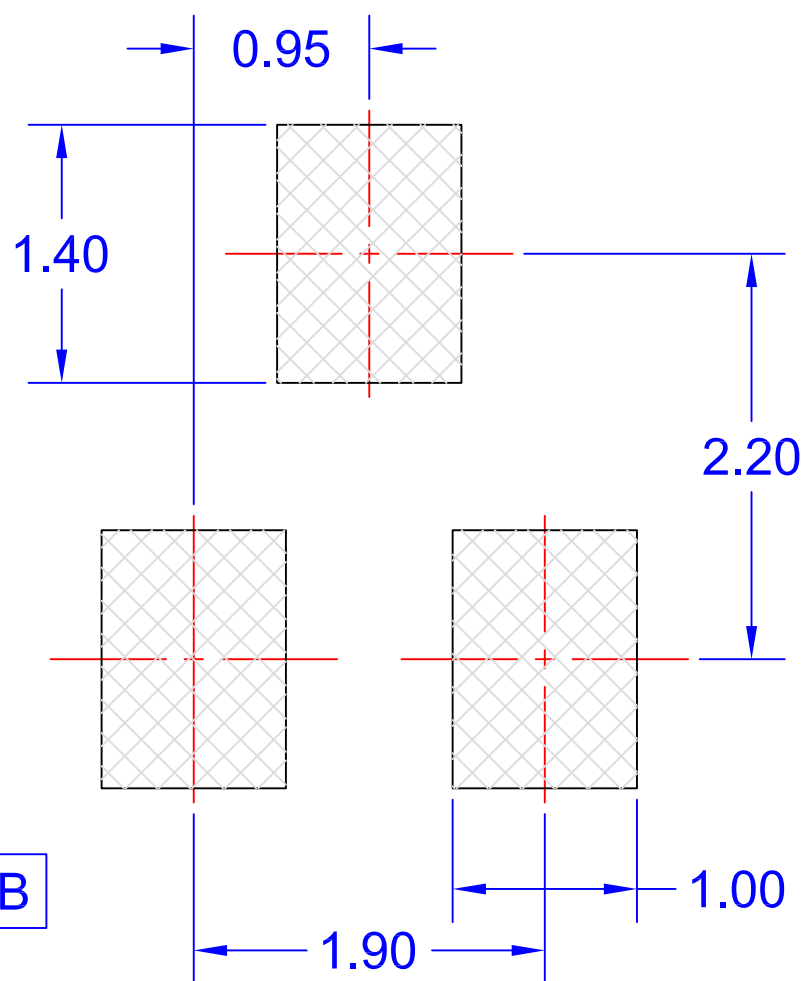


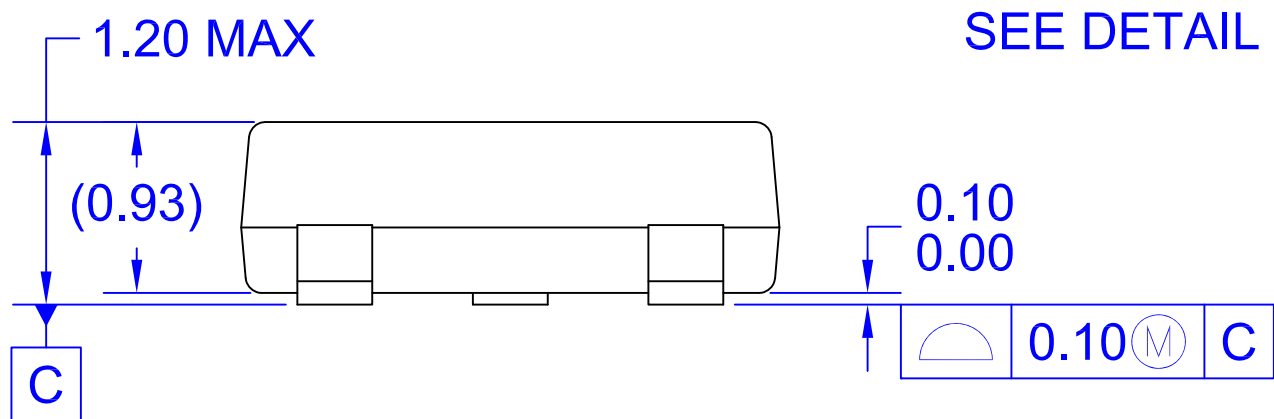
Figure 11. Transient Thermal Response Curve.



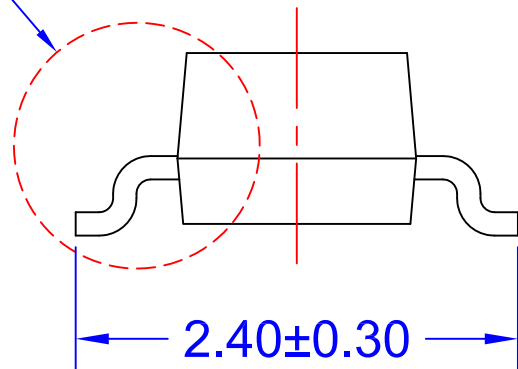
$\oplus$	0.20 (M)	A	B
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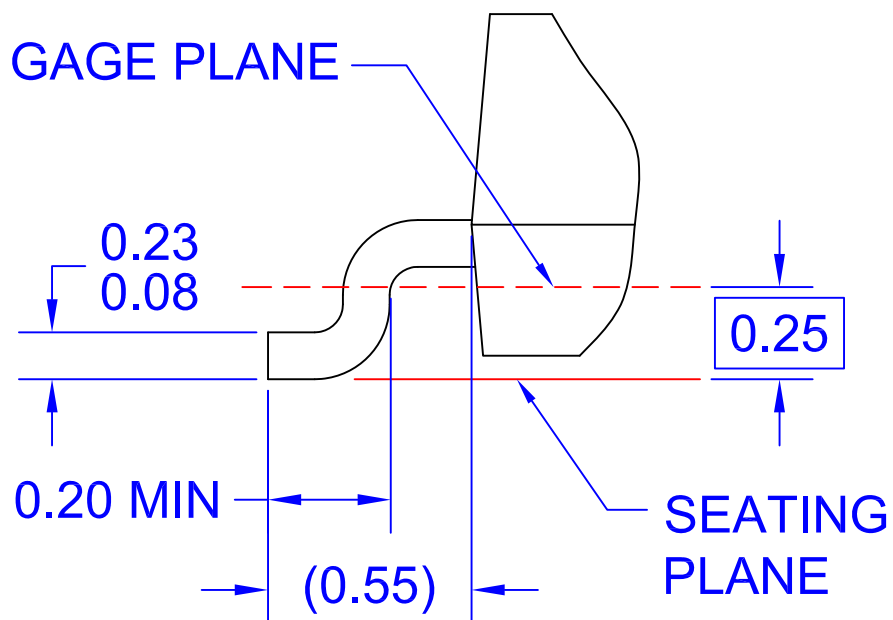
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SEE DETAIL A



NOTES: UNLESS OTHERWISE SPECIFIED



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- E) DRAWING FILE NAME: MA03DREV11





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