NCV4949A

100 mA, 5.0 V, Low Dropout Voltage Regulator with Reset and Sense

The NCV4949A is a monolithic integrated 5.0 V voltage regulator with a very low dropout and additional functions such as reset and an uncommitted voltage sense comparator.

It is designed for supplying microcontroller/microprocessor controlled systems particularly in automotive applications. The NCV4949A has improved reset behavior for lower input and output voltage levels.

Features

- Operating DC Supply Voltage Range 5.0 V to 28 V
- Transient Supply Voltage Up to 40 V
- High Precision Output Voltage 5.0 V ±1%
- Output Current Capability Up to 100 mA
- Very Low Dropout Voltage Less Than 0.4 V
- Reset Circuit Sensing The Output Voltage
- Programmable Reset Pulse Delay
- Voltage Sense Comparator
- Thermal Shutdown and Short Circuit Protections
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb−Free Devices

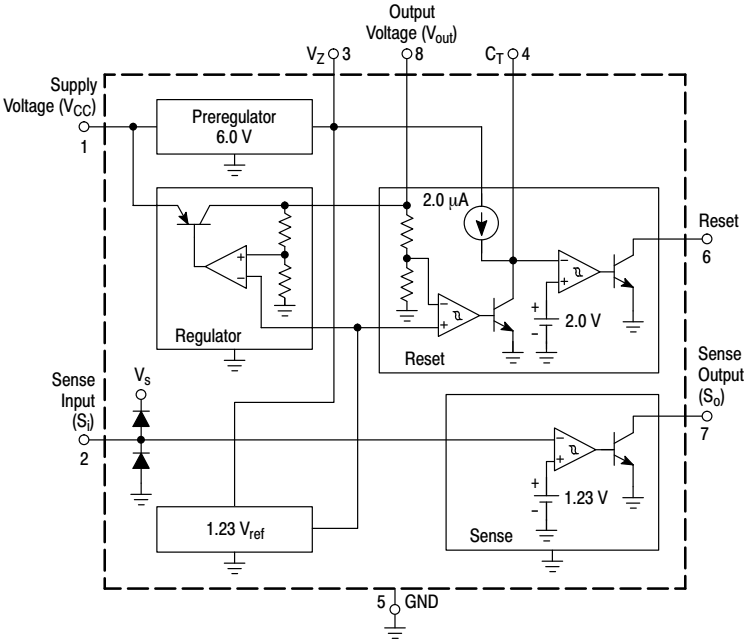


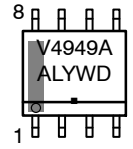
Figure 1. Representative Block Diagram

ON Semiconductor®

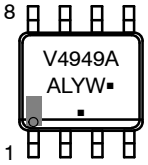
http://onsemi.com

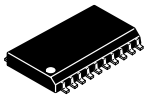
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751

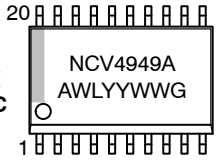


SOIC−8 EP
PD SUFFIX
CASE 751AC





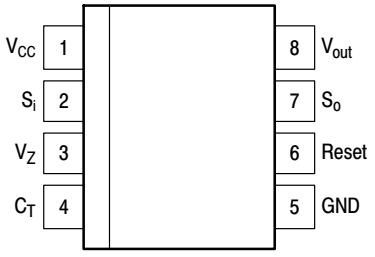
SOIC−20 W
DW SUFFIX
CASE 751AC



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Operating Supply Voltage	V_{CC}	28	V
Transient Supply Voltage (t < 1.0 s)	$V_{CC\ TR}$	40	V
Output Current	I_{out}	Internally Limited	–
Output Voltage	V_{out}	20	V
Sense Input Current	I_{SI}	±1.0	mA
Sense Input Voltage	V_{SI}	V_{CC}	–
Output Voltages			V
Reset Output	V_{Reset}	20	
Sense Output	V_{SO}	20	
Output Currents			mA
Reset Output	I_{Reset}	5.0	
Sense Output	I_{SO}	5.0	
Preregulator Output Voltage	V_Z	7.0	V
Preregulator Output Current	I_Z	5.0	mA
ESD Protection at any pin			V
Human Body Model	–	4000	
Machine Model	–	200	
Charged Device Model (SOIC−20 W)	–	1000	
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$		°C/W
SOIC−8		189.3	
SOIC−8 EP		84.8	
SOIC−20 W		95.8	
Operating Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LEAD TEMPERATURE SOLDERING REFLOW (Note 1)

Rating	Symbol	Min	Max	Unit
Reflow (SMD styles only) lead free 60 – 150 sec above 217, 40 sec max at peak	Tsld	–	260	°C
Moisture Sensitivity Level (SOIC−8)	MSL	Level 1		
Moisture Sensitivity Level (SOIC−8EP)	MSL	Level 2		
Moisture Sensitivity Level (SOIC−20W)	MSL	Level 3		

1. Per IPC / JEDEC J−STD−020C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, −40°C < T_A < 125°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 1.0 mA)	V_{out}	4.95	5.0	5.05	V
Output Voltage (6.0 V < V_{CC} < 28 V, 1.0 mA < I_{out} < 50 mA)	V_{out}	4.9	5.0	5.1	V
Output Voltage (V_{CC} = 35 V, t < 1.0 s, 1.0 mA < I_{out} < 50 mA)	V_{out}	4.9	5.0	5.1	V
Dropout Voltage	V_{drop}				V
I_{out} = 10 mA		–	0.1	0.25	
I_{out} = 50 mA		–	0.2	0.40	

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14 V, −40°C < T_A < 125°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
I_{out} = 100 mA		–	0.3	0.50	
Input to Output Voltage Difference in Undervoltage Condition (V_{CC} = 4.0 V, I_{out} = 35 mA)	V_{IO}	–	0.2	0.4	V
Line Regulation (6.0 V < V_{CC} < 28 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	20	mV
Load Regulation (1.0 mA < I_{out} < 100 mA)	Reg_{load}	–	8.0	30	mV
Current Limit	I_{Lim}				mA
V_{out} = 4.5 V		105	200	400	
V_{out} = 0 V		–	100	–	
Quiescent Current (I_{out} = 0.3 mA, T_A < 100°C)	I_{QSE}	–	150	260	μA
Quiescent Current (I_{out} = 100 mA)	I_Q	–	–	5.0	mA
RESET					
Reset Threshold Voltage	V_{Resth}	–	4.5	–	V
Reset Threshold Hysteresis	$V_{Resth,hys}$				mV
@ T_A = 25°C		50	100	200	
@ T_A = −40 to +125°C		50	–	300	
Reset Pulse Delay (C_T = 100 nF, t_R ≥ 100 μs)	t_{ResD}	55	100	180	ms
Reset Reaction Time (C_T = 100 nF)	t_{ResR}	–	5.0	30	μs
Reset Output Low Voltage (R_{Reset} = 10 kΩ to V_{out}, V_{CC} ≥ 3.0 V)	V_{ResL}	–	–	0.4	V
Reset Output High Leakage Current (V_{Reset} = 5.0 V)	I_{ResH}	–	–	1.0	μA
Delay Comparator Threshold	V_{CTth}	–	2.0	–	V
Delay Comparator Threshold Hysteresis	$V_{CTth,\ hys}$	–	100	–	mV
SENSE					
Sense Low Threshold (V_{SI} Decreasing = 1.5 V to 1.0 V)	V_{SOth}	1.16	1.23	1.35	V
Sense Threshold Hysteresis	$V_{SOth,hys}$	20	100	200	mV
Sense Output Low Voltage (V_{SI} ≤ 1.16 V, V_{CC} ≥ 3.0 V, R_{SO} = 10 kΩ to V_{out})	V_{SOL}	–	–	0.4	V
Sense Output Leakage (V_{SO} = 5.0 V, V_{SI} ≥ 1.5 V)	I_{SOH}	–	–	1.0	μA
Sense Input Current	I_{SI}	−1.0	0.1	1.0	μA
PREREGULATOR					
Preregulator Output Voltage (I_Z = 10 μA)	V_Z	–	6.3	–	V

PIN FUNCTION DESCRIPTION

Pin SO−8, SO−8 EP	Pin SO−20 W	Symbol	Description
1	19	V_{CC}	Supply Voltage
2	20	S_i	Input of Sense Comparator
3	1	V_Z	Output of Preregulator
4	2	C_T	Reset Delay Capacitor
5	4−7, 14−17	GND	Ground
6	10	Reset	Output of Reset Comparator
7	11	S_O	Output of Sense Comparator
8	12	V_{out}	Main Regulator Output
–	3, 8, 9, 13, 18	NC	No Connect

TYPICAL CHARACTERIZATION CURVES

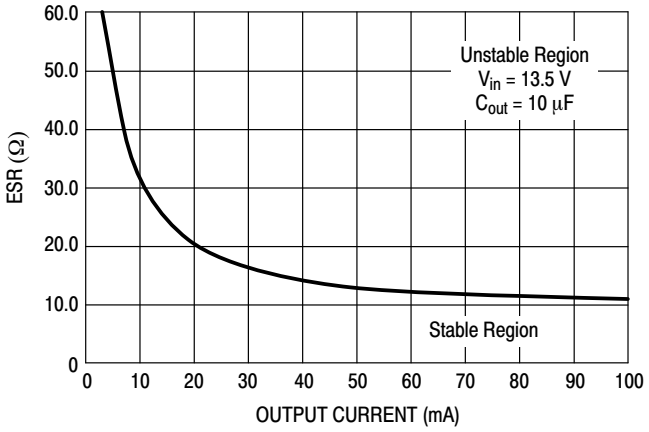


Figure 2. ESR Stability Border Vs. Output Current (Full ESR Range)

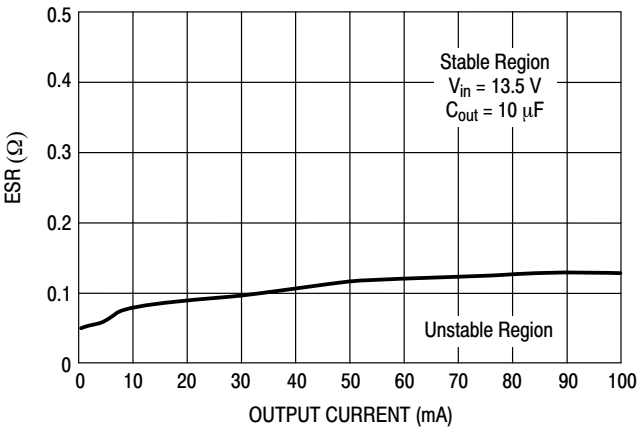


Figure 3. ESR Stability Border Vs. Output Current (Very Low ESR)

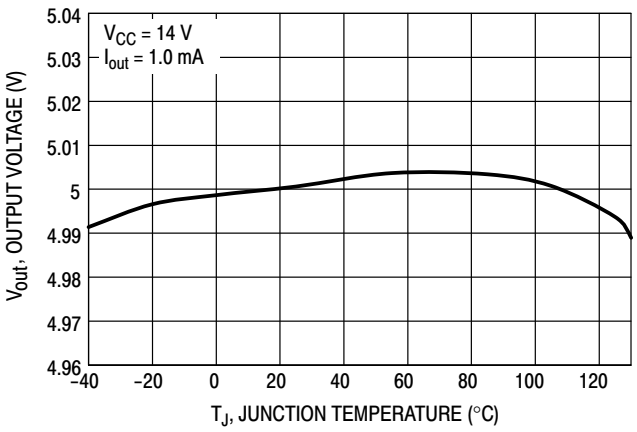


Figure 4. Output Voltage versus Junction Temperature

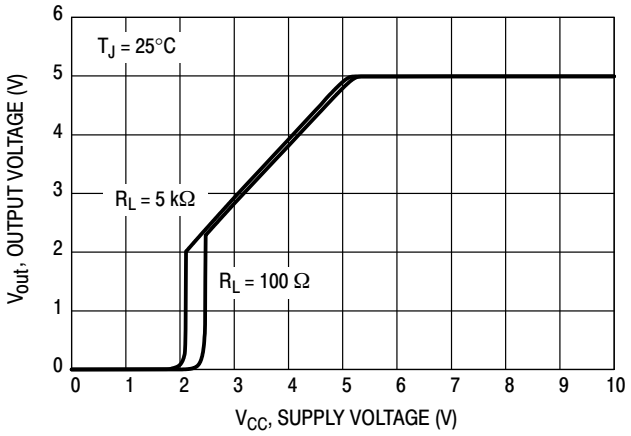


Figure 5. Output Voltage versus Supply Voltage

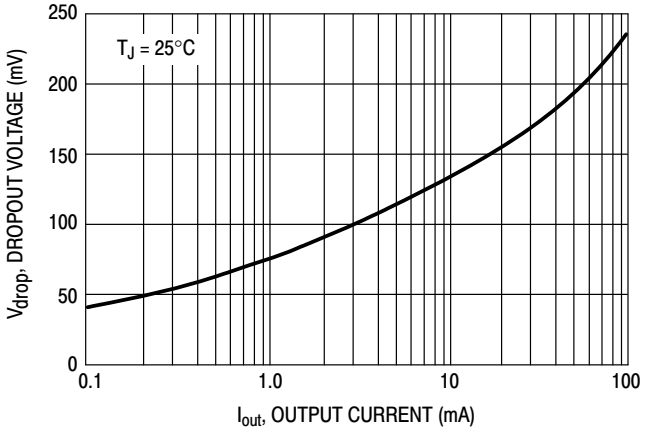


Figure 6. Dropout Voltage versus Output Current

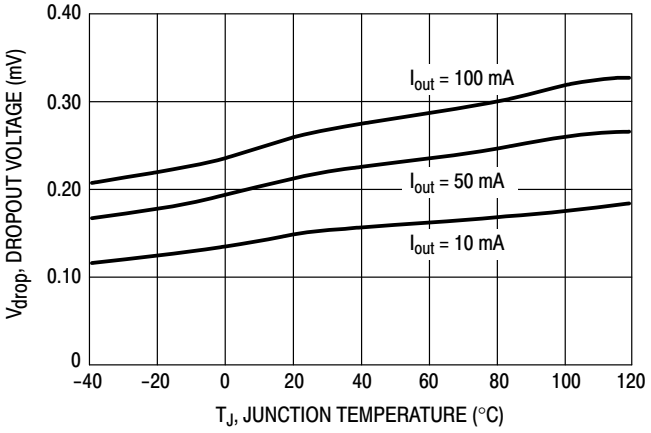


Figure 7. Dropout Voltage versus Junction Temperature

TYPICAL CHARACTERIZATION CURVES (continued)

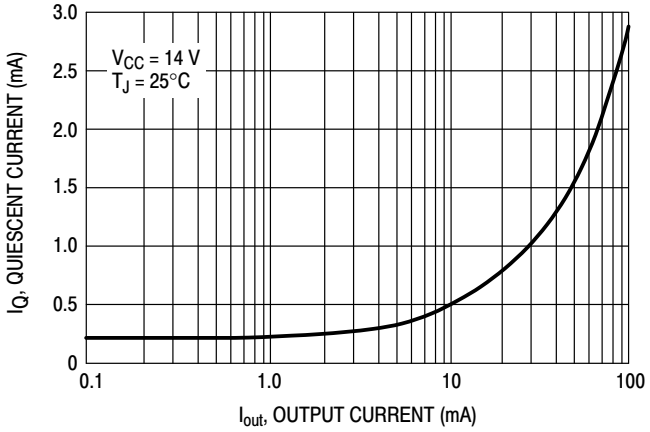


Figure 8. Quiescent Current versus Output Current

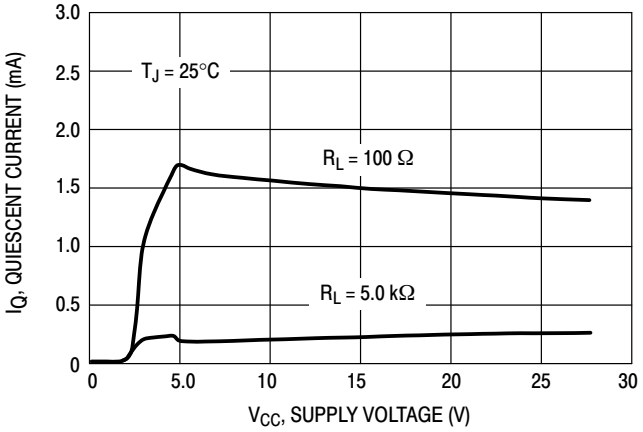


Figure 9. Quiescent Current versus Supply Voltage

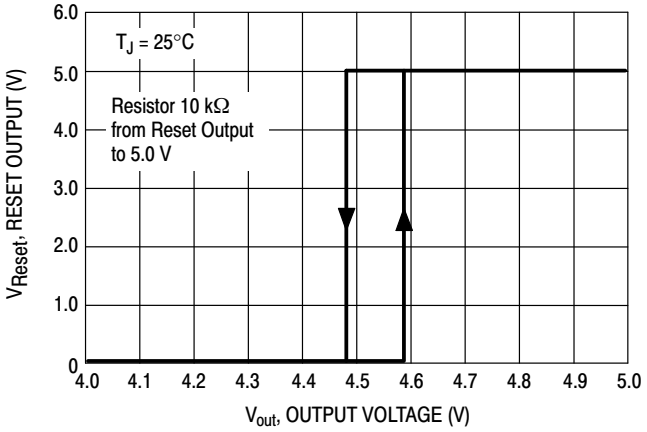


Figure 10. Reset Output versus Regulator Output Voltage

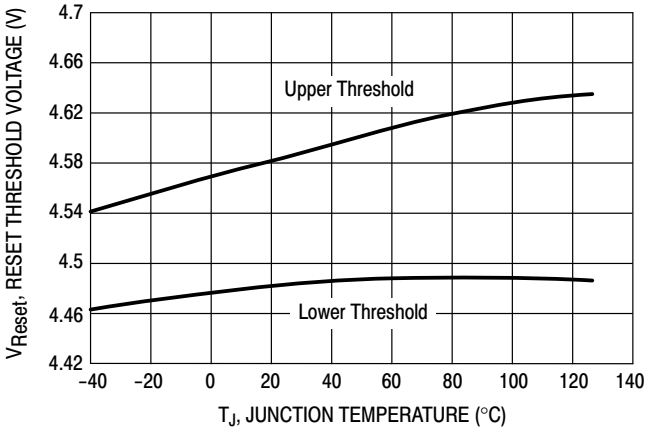


Figure 11. Reset Thresholds versus Junction Temperature

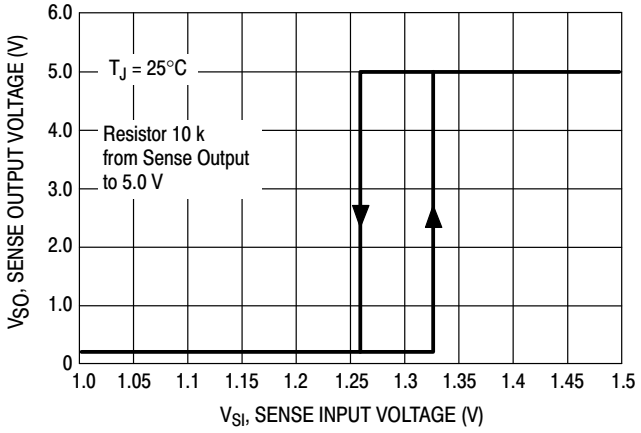


Figure 12. Sense Output versus Sense Input Voltage

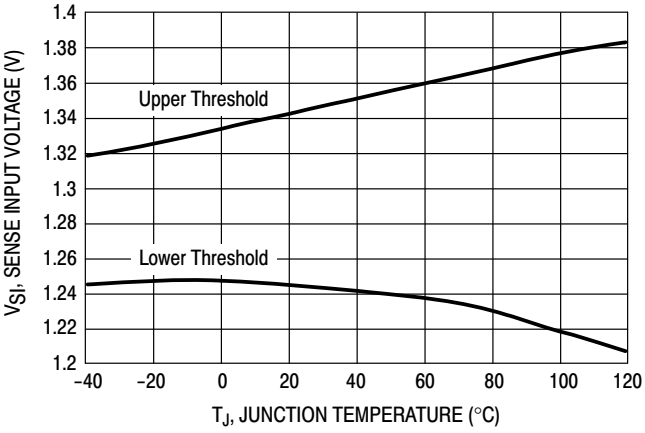
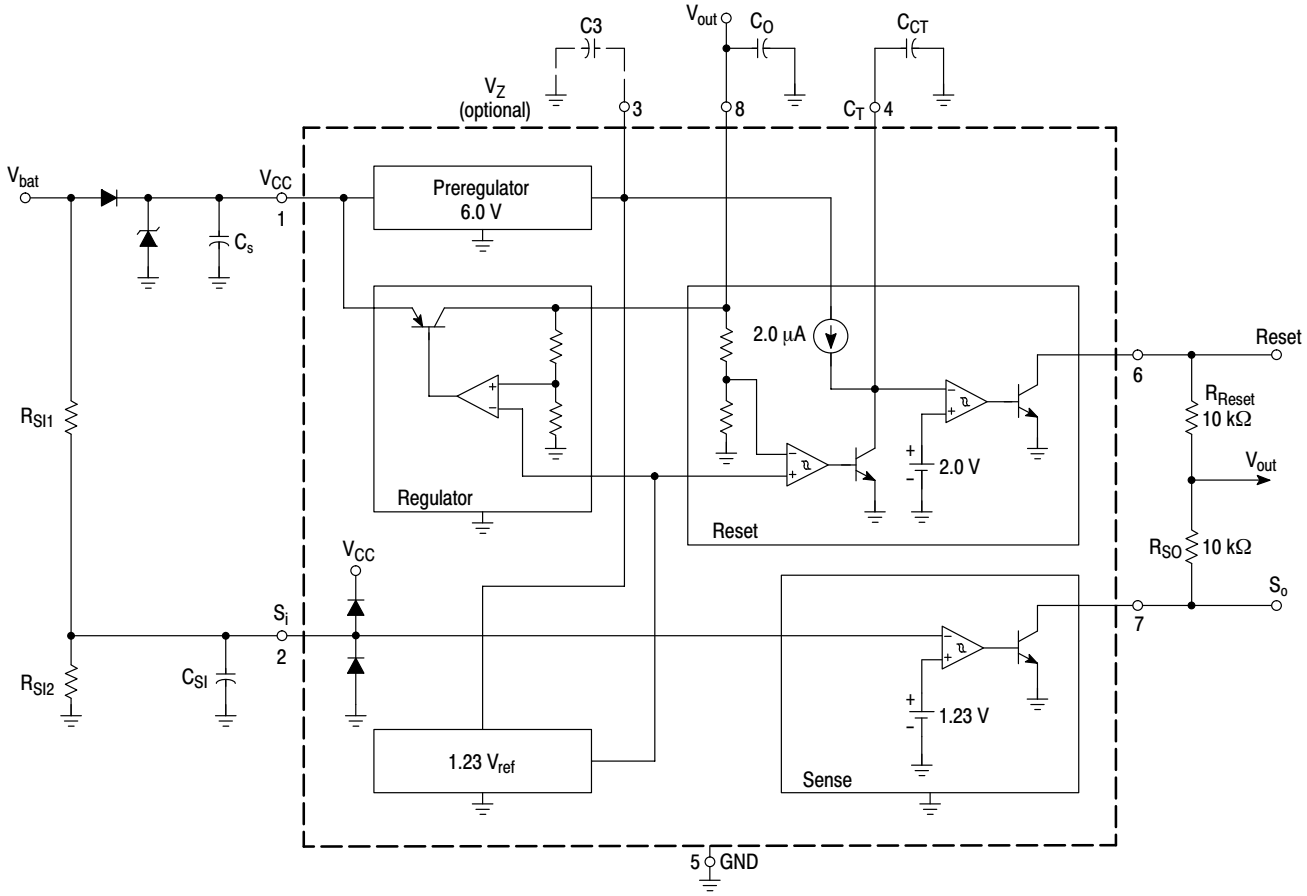


Figure 13. Sense Thresholds versus Junction Temperature

APPLICATION INFORMATION

Supply Voltage Transient

High supply voltage transients can cause a reset output signal perturbation. For supply voltages greater than 8.0 V the circuit shows a high immunity of the reset output against supply transients of more than 100 V/μs. For supply voltages less than 8.0 V supply transients of more than 0.4 V/μs can cause a reset signal perturbation. To improve the transient behavior for supply voltages less than 8.0 V a capacitor at Pin 3 can be used. A capacitor at Pin 3 (C3 ≤ 1.0 μF) also reduces the output noise.



NOTE: 1. For stability: $C_s \geq 1.0$ μF, $C_O \geq 4.7$ μF, ESR < 10 Ω at 10 kHz
2. Recommended for application: C_s = 10 μF, C_O = 10 μF to 74 μF @ T_A = 125°C
By using higher C_s it is possible to use higher C_O.

Figure 14. Application Schematic

OPERATING DESCRIPTION

The NCV4949A is a monolithic integrated low dropout voltage regulator. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. It is also suitable in other applications where the included functions are required. The modular approach of this device allows the use of other features and functions independently when required.

Voltage Regulator

The voltage regulator uses an isolated collector vertical PNP transistor as a regulating element. With this structure, very low dropout voltage at currents up to 100 mA is obtained. The dropout operation of the standby regulator is maintained down to 3.0 V input supply voltage. The output voltage is regulated up to a transient input supply voltage of 35 V.

A typical curve showing the standby output voltage as a function of the input supply voltage is shown in Figure 16.

The current consumption of the device (quiescent current) is less than 200 μA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. The quiescent current as a function of the supply input voltage is shown in Figure 17.

Short Circuit Protection:

The maximum output current is internally limited. In case of short circuit, the output current is foldback current limited as described in Figure 15.

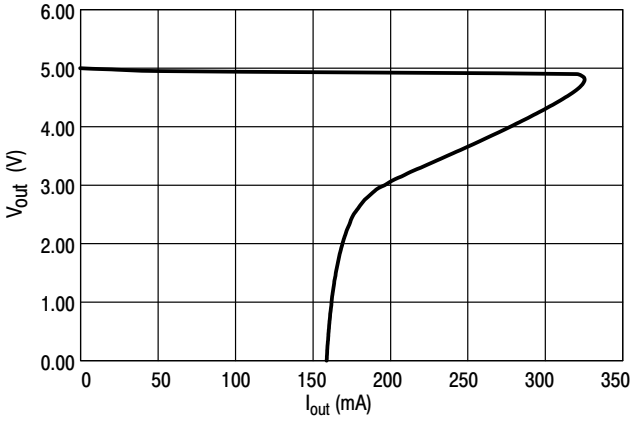


Figure 15. Foldback Characteristic of V_{out}

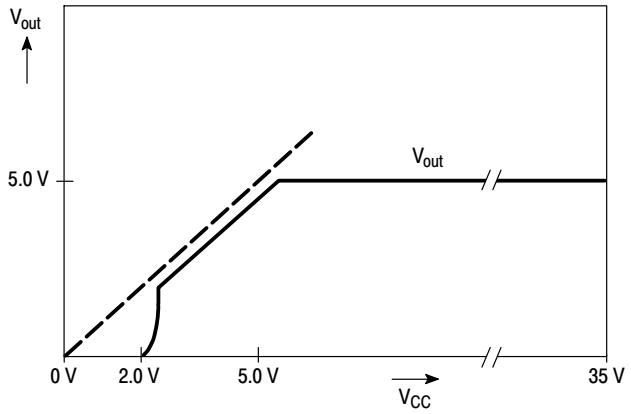


Figure 16. Output Voltage versus Supply Voltage

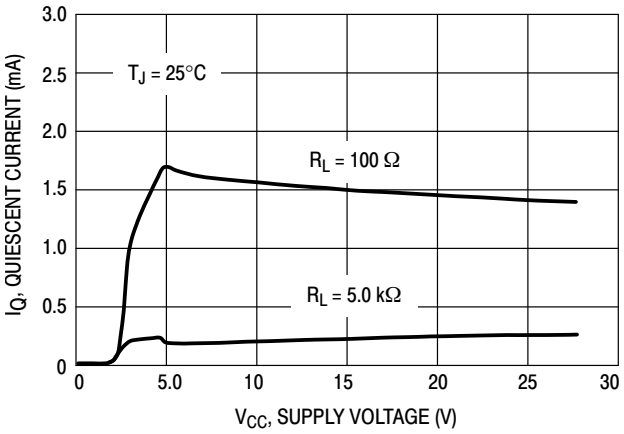


Figure 17. Quiescent Current versus Supply Voltage

Preregulator

To improve transient immunity a preregulator stabilizes the internal supply voltage to 6.0 V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small (≤ 100 μA).

This output may be used to improve transient behavior for supply voltages less than 8.0 V. In this case a capacitor (100 nF – 1.0 μF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in Figure 18.

The reset circuit supervises the output voltage. The reset threshold of 4.5 V is defined by the internal reference voltage and standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T:

$$t_{RD} = \frac{C_T \times 2.0\ V}{2.0\ \mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T. The reaction time of the reset circuit increases the noise immunity.

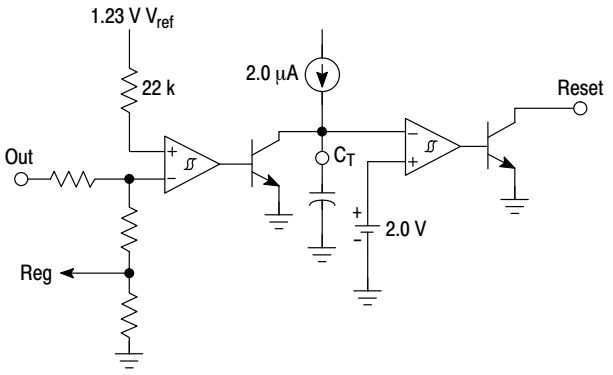


Figure 18. Reset Circuit

Output voltage drops below the reset threshold only marginally longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for output voltage drops longer than approximately 50 μs. The typical reset output waveforms are shown in Figure 19.

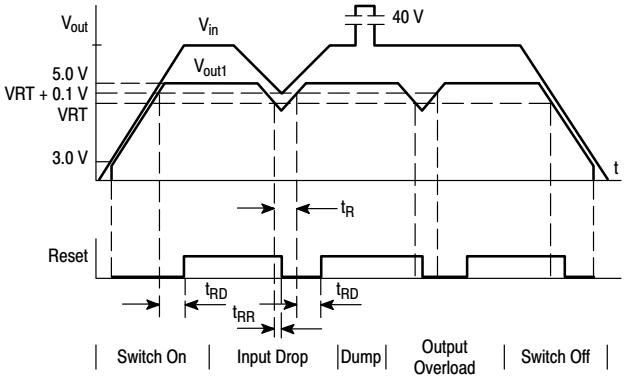


Figure 19. Typical Reset Output Waveforms

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23 V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after a protection diode and to provide additional information to the microprocessor such as low voltage warnings.

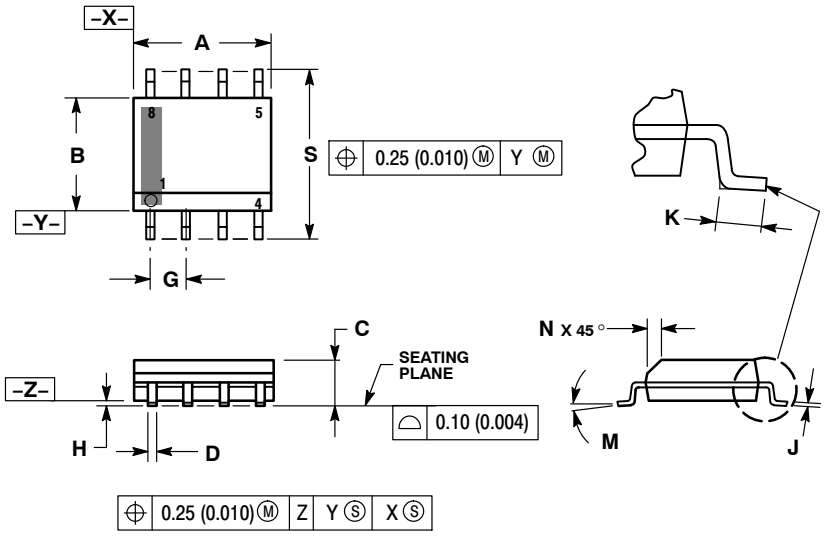
ORDERING INFORMATION

Device	Package	Shipping†
NCV4949ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV4949APDR2G	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel
NCV4949ADWR2G	SOIC−20 WB (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

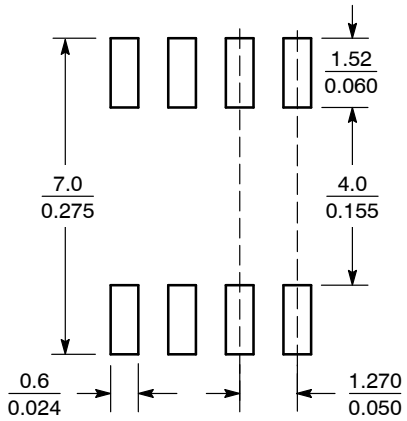
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

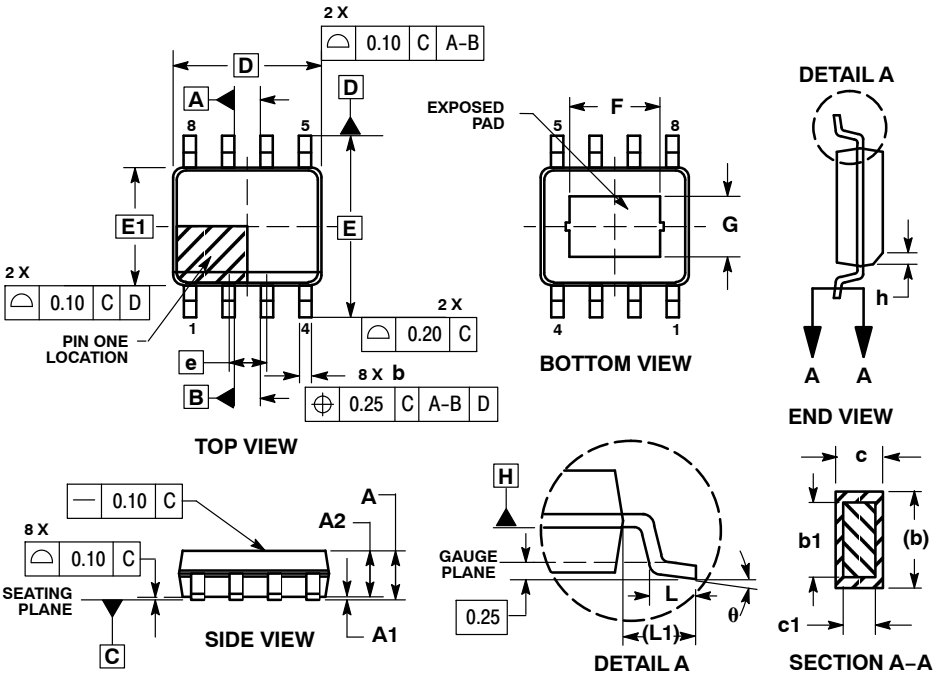


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

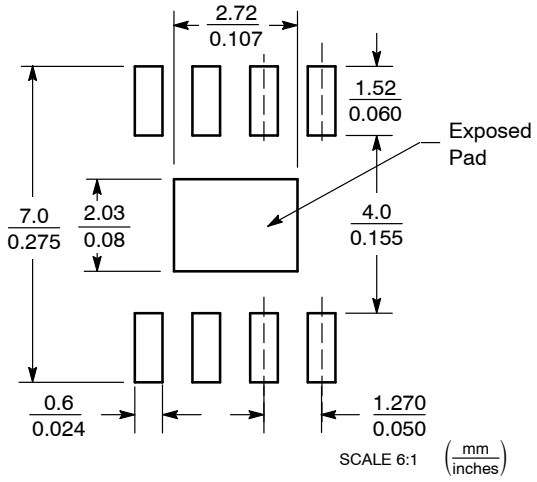
SOIC−8 EP
CASE 751AC−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

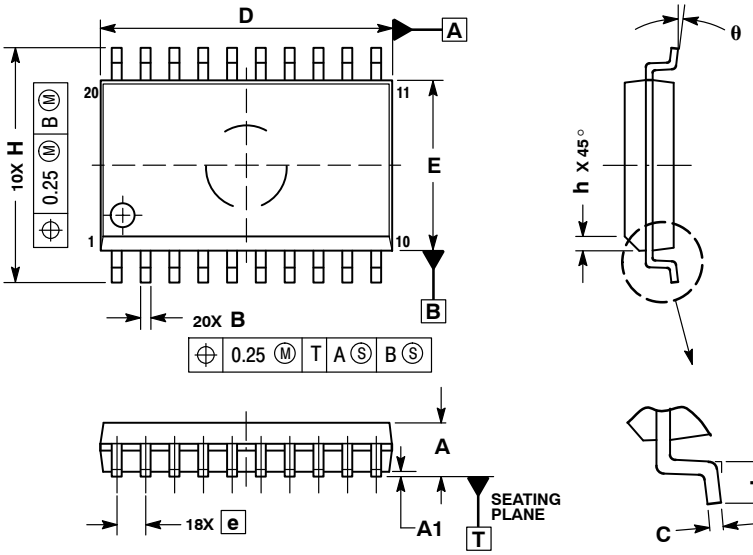
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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