8k, 16k bit EEPROMs for direct connection to serial ports

BR9080AF-W / BR9080ARFV-W / BR9080ARFVM-W / BR9016AF-W / BR9016ARFV-W / BR9016ARFVM-W

The BR9080A and BR9016A series are serial EEPROMs that can be connected directly to a serial port and can be erased and written electrically. Writing and reading is performed in word units, using four types of operation commands. Communication occurs though $\overline{CS}$, $\overline{SK}$, DI, and DO pins, $\overline{WC}$ pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing, operation is checked via the internal status check.

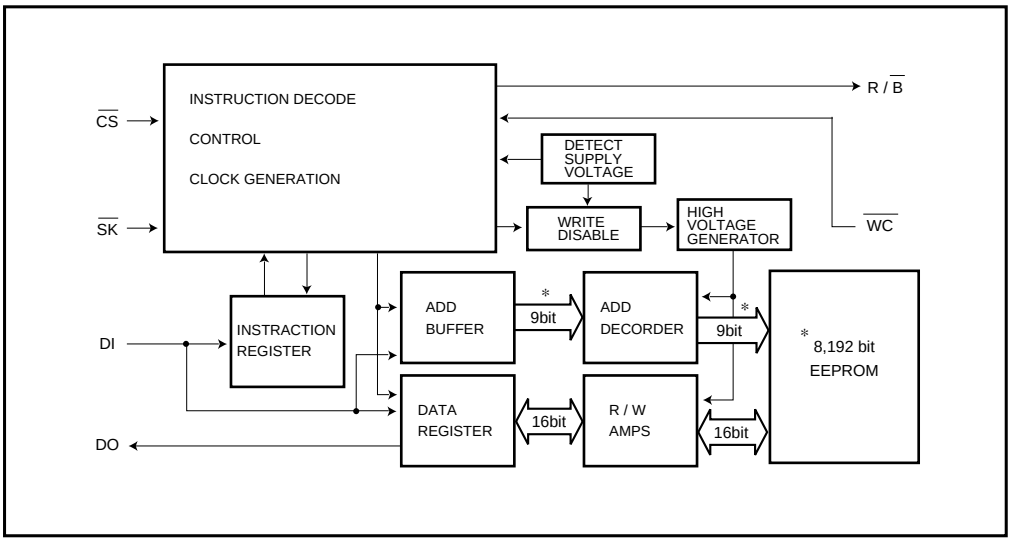
●Applications

Movie, camera, cordless telephones, car stereos, VCRs, TVs, DIP switches, and other battery-powered equipment requiring low voltage and low current

●Features

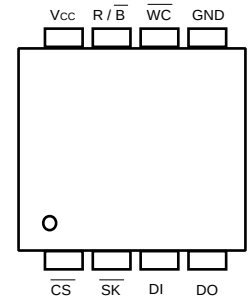
1) BR9080AF-W / ARFV-W / ARFVM-W (8k bit) : 512 words ×16 bits
   BR9016AF-W / ARFV-W / ARFVM-W (16k bit) : 1024 words × 16bits
2) Single power supply operation
3) Serial data input and output
4) Automatic erase-before-write
5) Low current consumption
   Active (5V) : 5mA (max.)
   Standby (5V) : 3μA (max.)
6) Noise filter built into $\overline{SK}$ pin
7) Write protection when V_{CC} is low
   Inhibition on inadvertant write with the $\overline{WC}$ pin.
8) SOP8 / SSOP-B8 / MSOP8
9) High reliability CMOS process
10) 100,000 ERASE / WRITE cycles
11) 10 years Data Retention

●Block diagram

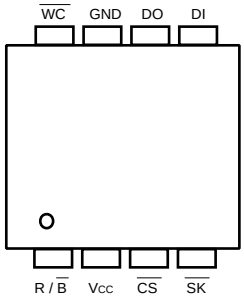


∗ BR9016A is 10bit, 16,384bit
BR9080A is 9bit, 8,192bit

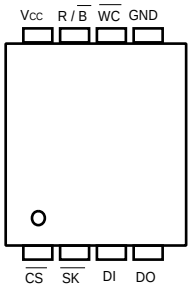
●Pin descriptions



BR9080ARFVM
BR9016ARFVM : MSOP8



BR9080AF
BR9016AF : SOP8



BR9080ARFV
BR9016ARFV : SSOP-B8

Fig.1

Pin No.		Pin name	Function
MSOP / SSOP	SOP		
1	3	$\overline{CS}$	Chip Select Control
2	4	$\overline{SK}$	Serial Data Clock Input
3	5	DI	Op code, address, Serial Data Input
4	6	DO	Serial Data Output
5	7	GND	Ground 0V
6	8	$\overline{WC}$	Write Control Input
7	1	R / $\overline{B}$	READY / $\overline{BUSY}$ Output
8	2	Vcc	Power supply

●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits		Unit
Supply voltage	V_{CC}	–0.3~+7.0		V
Power dissipation	Pd	SOP8	450*1	mW
		SSOP-B8	300*2	
		MSOP8	310*3	
Storage temperature	Tstg	–65~+125		°C
Operation temperature	Topr	–40~+85		°C
Input voltage	–	–0.3~V_{CC}+0.3		V

*1 Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.
*2 Reduced by 3.0mW for each increase in Ta of 1°C over 25°C.
*3 Reduced by 3.1mW for each increase in Ta of 1°C over 25°C.

●**Recommended operating conditions** (Ta=25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	WRITE	V_{CC}	2.7	–	5.5	V
	READ		2.7	–	5.5	V
Input voltage		V_{IN}	0	–	V_{CC}	V

●Electrical characteristics

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W : 5V

(Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.7V~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	–	–	0.3×V_{CC}	V	DI pin
Input high level voltage 1	V_{IH1}	0.7×V_{CC}	–	–	V	DI pin
Input low level voltage 2	V_{IL2}	–	–	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Input high level voltage 2	V_{IH2}	0.8×V_{CC}	–	–	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Output low level voltage	V_{OL}	0	–	0.4	V	I_{OL}=2.1mA
Output high level voltage	V_{OH}	V_{CC}–0.4	–	V_{CC}	V	I_{OH}=–0.4mA
Input leak current	I_{LI}	–1	–	1	μA	V_{IN}=0V~V_{CC}
Output leak current	I_{LO}	–1	–	1	μA	V_{OUT}=0V~V_{CC}, $\overline{CS}$=V_{CC}
Operating current	I_{CC1}	–	–	5	mA	$f_{\overline{SK}}$=2MHz tE / W=10ms (WRITE)
	I_{CC2}	–	–	3	mA	$f_{\overline{SK}}$=2MHz (READ)
Standby current	I_{SB}	–	–	3	μA	$\overline{CS}$ / $\overline{SK}$ / DI / $\overline{WC}$=V_{CC} DO, R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	–	–	2	MHz	–

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W : 3V

(Unless otherwise noted, Ta=–40~85°C, V_{CC}=2.7V~3.3V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	–	–	0.3×V_{CC}	V	DI pin
Input high level voltage 1	V_{IH1}	0.7×V_{CC}	–	–	V	DI pin
Input low level voltage 2	V_{IL2}	–	–	0.2×V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Input high level voltage 2	V_{IH2}	0.8×V_{CC}	–	–	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ pin
Output low level voltage	V_{OL}	0	–	0.4	V	I_{OL}=100μA
Output high level voltage	V_{OH}	V_{CC}–0.4	–	V_{CC}	V	I_{OH}=–100μA
Input leak current	I_{LI}	–1	–	1	μA	V_{IN}=0V~V_{CC}
Output leak current	I_{LO}	–1	–	1	μA	V_{OUT}=0V~V_{CC}, $\overline{CS}$=V_{CC}
Operating current	I_{CC1}	–	–	3	mA	$f_{\overline{SK}}$=2MHz tE / W=10ms (WRITE)
	I_{CC2}	–	–	0.75	mA	$f_{\overline{SK}}$=2MHz (READ)
Standby current	I_{SB}	–	–	2	μA	$\overline{CS}$ / $\overline{SK}$ / DI / $\overline{WC}$=V_{CC} DO, R / $\overline{B}$=OPEN
$\overline{SK}$ frequency	f_{SK}	–	–	2	MHz	–

◎ Not designed for radiation resistance

●Operating timing characteristics

BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W

(Unless otherwise noted, Ta=−40~85°C, V_{CC}=2.7V~5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	100	–	–	ns
$\overline{CS}$ hold time	t_{CSH}	100	–	–	ns
Data setup time	t_{DIS}	100	–	–	ns
Data hold time	t_{DIH}	100	–	–	ns
DO rise delay time	t_{PD1}	–	–	150	ns
DO fall delay time	t_{PD0}	–	–	150	ns
Self-timing programming cycle	$t_{E/W}$	–	–	10	ms
$\overline{CS}$ minimum high level time	t_{CS}	250	–	–	ns
READY / $\overline{BUSY}$ display valid time	t_{SV}	–	–	150	ns
Time when DO goes HIGH-Z (via $\overline{CS}$)	t_{OH}	0	–	150	ns
Data clock high level time	t_{WH}	230	–	–	ns
Data clock low level time	t_{WL}	230	–	–	ns
Write control setup time	t_{WCS}	0	–	–	ns
Write control hold time	t_{WCH}	0	–	–	ns

●Timing chart

Synchronous Data Input Output Timing

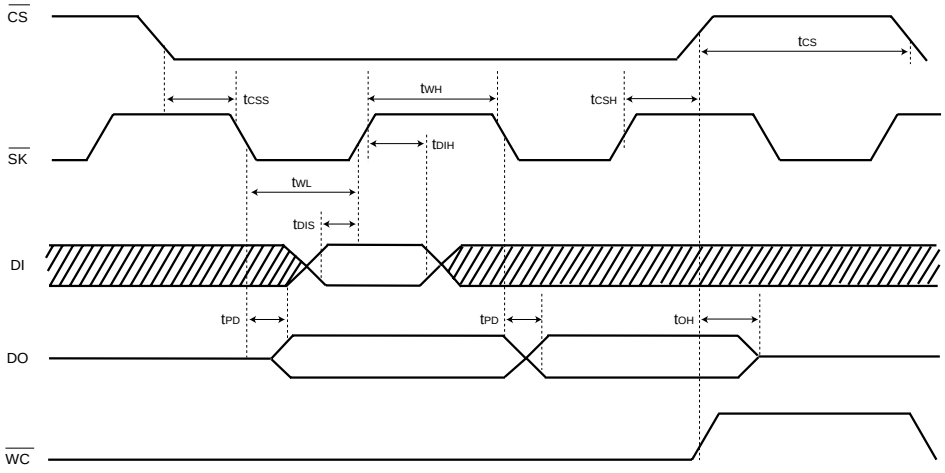


Fig.2

· Input data are clocked in to DI at the rising edge of the clock ($\overline{SK}$).

· Output data will toggle on the falling edge of the $\overline{SK}$ clock.

· The $\overline{WC}$ pin does not have any effect on the READ, EWEN and EWDS operations.

●Circuit operation

(1) Command mode

BR9080A

Instruction	Start Bit	Op Code	Address	Data
Read (READ)	1010	100 A0	A1 A2 A3 A4 A5 A6 A7 A8	
Write (WRITE)	1010	010 A0	A1 A2 A3 A4 A5 A6 A7 A8	D0 D1 – D14 D15
Write enable (WEN)	1010	0011	* * * * * * * *	
Write disable (WDS)	1010	0000	* * * * * * * *	

* : Means either V_{IH} or V_{IL}
Address and data are transferred from LSB.

BR9016A

Instruction	Start Bit	Op Code	Address	Data
Read (READ)	1010	10 A0 A1	A2 A3 A4 A5 A6 A7 A8 A9	
Write (WRITE)	1010	01 A0 A1	A2 A3 A4 A5 A6 A7 A8 A9	D0 D1 – D14 D15
Write enable (WEN)	1010	0011	* * * * * * * *	
Write disable (WDS)	1010	0000	* * * * * * * *	

* : Means either V_{IH} or V_{IL}
Address and data are transferred from LSB.

(2) Writing enabled / disabled

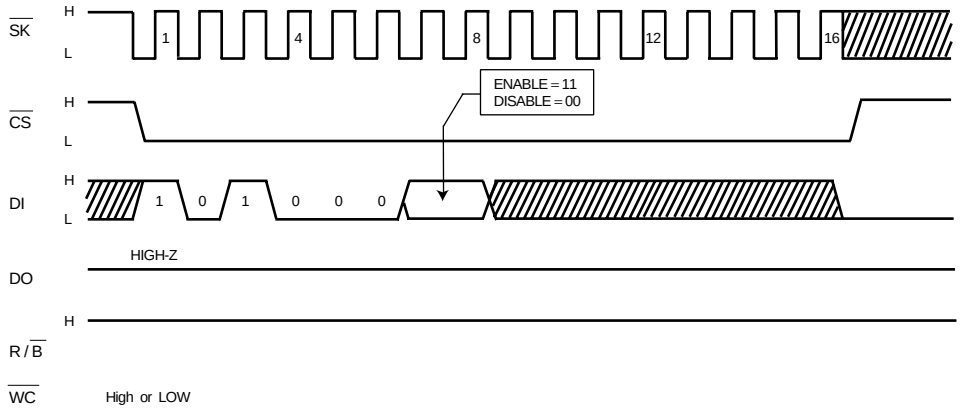


Fig.3

1) When $\overline{CS}$ is “HIGH” during power up, BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W comes up in the write disabled (WDS) state. In order to be programmable, it must receive a write enable (WEN) instruction.
   The device remains programmable until a disable (WDS) instruction is entered, or until it is powered down.
2) It is unnecessary to add the clock after 16th clock.

(3) Read cycle

BR9080AF-W / ARFV-W / ARFVM-W

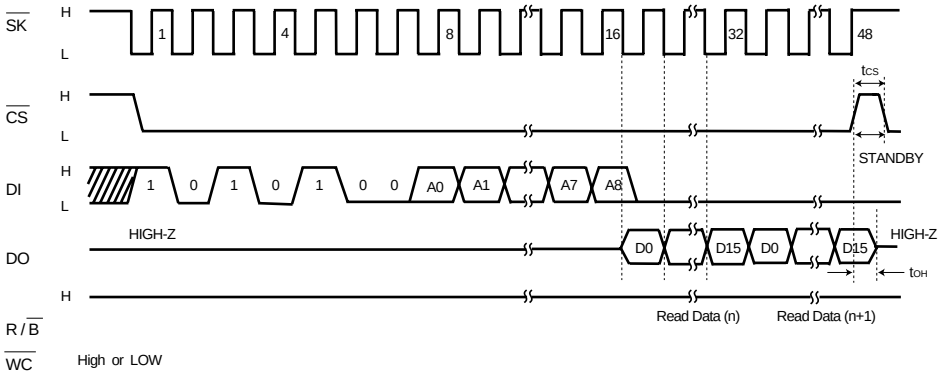


Fig.4 BR9080AF-W / ARFV-W / ARFVM-W

BR9016 AF-W / ARFV-W / ARFVM-W

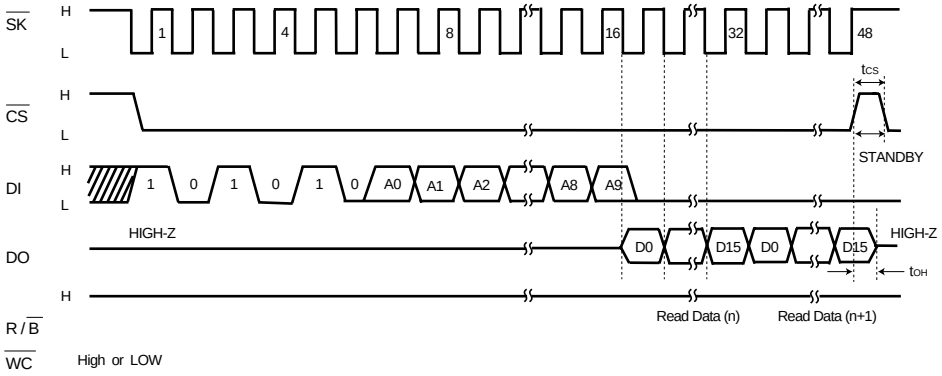


Fig.5 BR9016AF-W / ARFV-W / ARFVM-W

1) After the fall of the 16th clock pulse, 16-bit data is output from the DO pin in synchronization with the falling edge of the $\overline{SK}$ signal.
(DO output changes at a time lag of t_{PD0}, t_{PD1} because of internal circuit delay following the falling edge of the $\overline{SK}$ signal. During the t_{PD0} and t_{PD1} timing, the t_{PD} time should be assured before data is read, to avoid the previous data being lost. See the synchronized data input / output timing chart in Fig.2.)
2) The data stored in the next address is clocked out of the device on the falling edge of 32nd clock. The data stored in the upper address every 16 clocks is output sequentially by the continual $\overline{SK}$ input. Also the read operation is reset by $\overline{CS}$ High.

(4) Write cycle

BR9080AF-W / ARFV-W / ARFVM-W

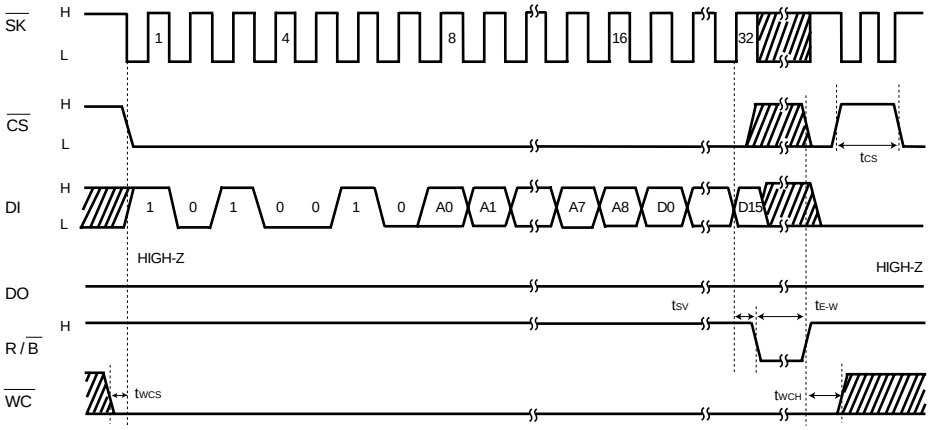


Fig.6 BR9080AF-W / ARFV-W / ARFVM-W

BR9016 AF-W / ARFV-W / ARFVM-W

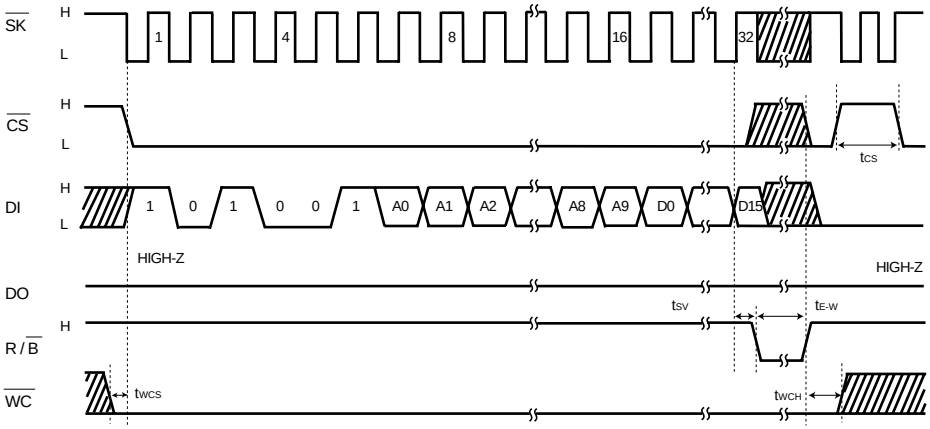


Fig.7 BR9016AF-W / ARFV-W / ARFVM-W

1) At the rising edge of 32nd clock, R / $\overline{B}$ pin will be come out “LOW” after the specified time delay (tSV).
2) From above edge R / $\overline{B}$ will indicate the ready / busy status of the chip: “LOW” indicated programming is all in progress: “HIGH” indicates the write cycle is complete and this part is ready for another instruction.
3) During the input of Write command, $\overline{CS}$ must be “LOW”. However, once the write operation started, $\overline{CS}$ could be either “HIGH” or “LOW”.
4) If $\overline{WC}$ becomes “HIGH” during Write Cycle, the write operation is halted. In this case, the address data in writing is no guaranteed. It is necessary to rewrite it.

(5) READY / $\overline{\text{BUSY}}$ display

(R / $\overline{\text{B}}$ pin and DO pin: BR9080AF-W / ARFV-W / ARFVM-W, BR9016AF-W / ARFV-W / ARFVM-W)

1) This display outputs the internal status signal; the R / $\overline{\text{B}}$ pin outputs the HIGH or LOW status at all times. The display can also be output from the DO pin. Following completion of the writing command, if $\overline{\text{CS}}$ falls while $\overline{\text{SK}}$ is LOW, either HIGH or LOW is output. (The display can also be output without using the R / $\overline{\text{B}}$ pin, leaving it open.)

2) When writing data to a memory cell, the READY / $\overline{\text{BUSY}}$ display is output from the rise of the 32nd clock pulse of the $\overline{\text{SK}}$ signal after tSV, from the R / $\overline{\text{B}}$ pin.

R / $\overline{\text{B}}$ display = LOW: writing in progress

(The internal timer circuit is activated, and after the tE / W timing has been created, the timer circuit stops automatically. Writing of data to the memory cell is done during the tE / W timing, during which time other commands cannot be received.)

R / $\overline{\text{B}}$ display = HIGH: command standby state

(Writing of data to the memory cell has been completed and the next command can be received.)

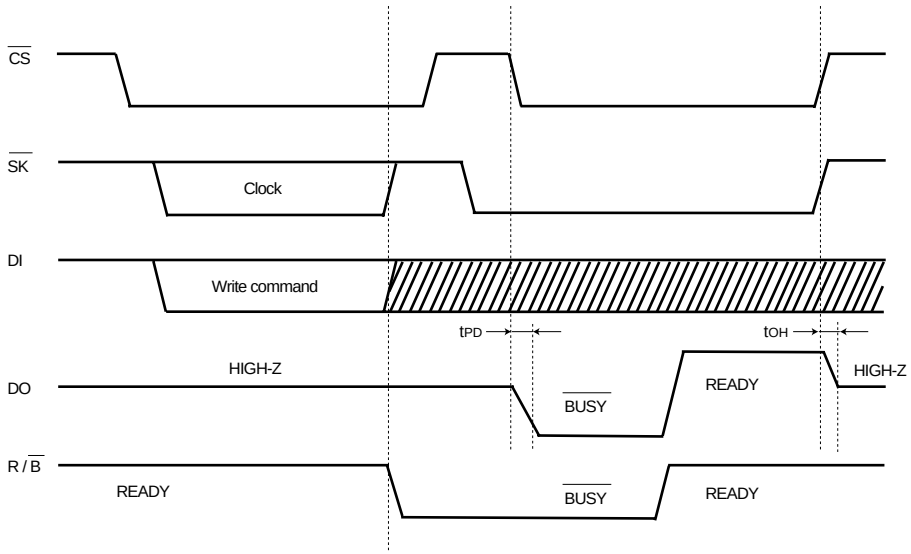


Fig.8 R / $\overline{\text{B}}$ Status Output timing chart

1) DO will output R / $\overline{\text{B}}$ status after $\overline{\text{CS}}$ is held low during $\overline{\text{SK}}$=L, until $\overline{\text{CS}}$ is held high.

Note : The document may be strategic technical data subject to COCOM regulations.

●Operation notes

(1) Turning the power supply on and off

1) When the power supply is turned on and off, $\overline{CS}$ should be set to HIGH (=V_{CC}).

2) When $\overline{CS}$ is LOW, the command input reception state (active) is entered. If the power supply is turned on in this state, erroneous operations and erroneous writing can occur because of noise and other factors. To avoid this, make sure $\overline{CS}$ is set to HIGH (=V_{CC}) before turning on the power supply.

(Good example) Here, the $\overline{CS}$ pin is pulled up to V_{CC}.

When turning off the power supply, wait at least 10msec before turning it on again. Failing to observe this condition can result in the internal circuit failing to be reset when the power supply is turned on.

(Bad example) $\overline{CS}$ is LOW when the power supply is turned on or off.

In this case, because $\overline{CS}$ remains LOW, the EEPROM may perform erroneous operations or write erroneous data because of noise or other factors.

* Please be aware that the case shown in this example can also occur if $\overline{CS}$ input is HIGH-Z.

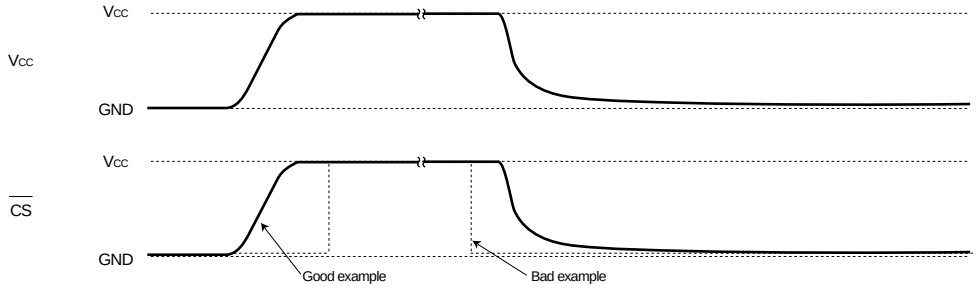


Fig.9

(2) Noise countermeasures

1) $\overline{SK}$ noise

If noise occurs at the rise of the $\overline{SK}$ clock input, the clock is assumed to be excessive, and this can cause malfunction because the bits are out of alignment.

2) $\overline{WC}$ noise

During a writing operation, noise at the $\overline{WC}$ pin can be erroneously judged to be data, and this can cause writing to be forcibly interrupted.

3) V_{CC} noise

Noise and surges on the power supply line can cause malfunction. We recommend installing a bypass capacitor between the power supply and ground to eliminate this problem.

(3) Canceling modes

1) Read commands

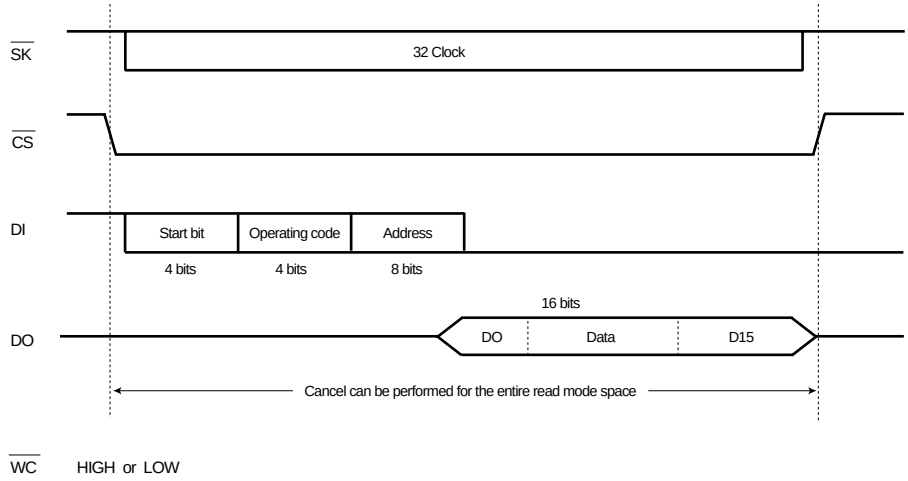


Fig.10

Cancellation method: $\overline{CS}$ HIGH

2) Write commands

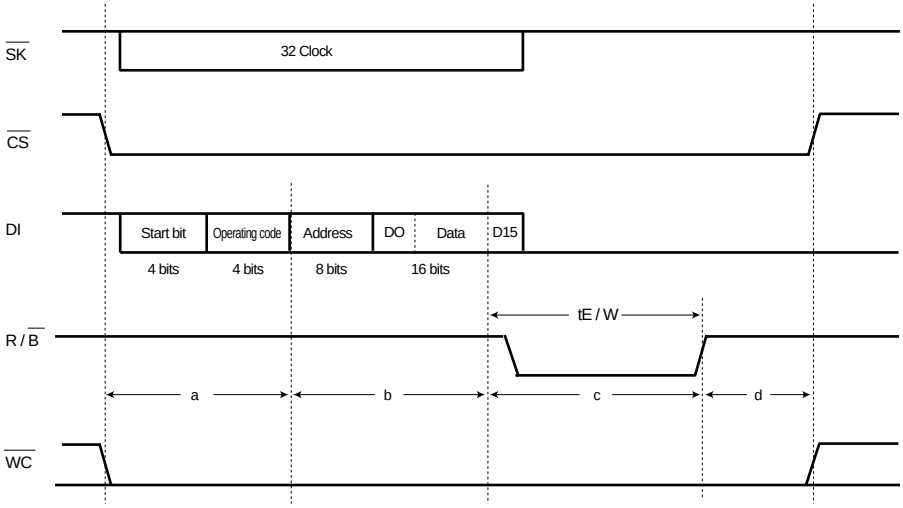


Fig.11

Canceling methods

a : Canceled by setting $\overline{CS}$ HIGH. The $\overline{WC}$ pin is not involved.

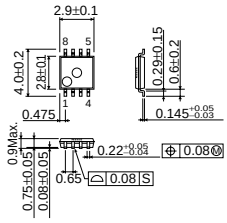
b : If the $\overline{WC}$ pin goes HIGH for even a second, writing is forcibly interrupted. Cancellation occurs even if the $\overline{CS}$ pin is HIGH. At this point, data has not been written to the memory, so the data in the designated address has not yet been changed.

c : The operation is forcibly canceled by setting the $\overline{WC}$ pin to HIGH or turning off the power supply (although we do not recommend using this method). The data in the designated address is not guaranteed and should be written once again.

d : If $\overline{CS}$ is set to HIGH while the R / $\overline{B}$ signal is HIGH (following the tE / W timing), the IC is reset internally, and waits for the next command to be input.

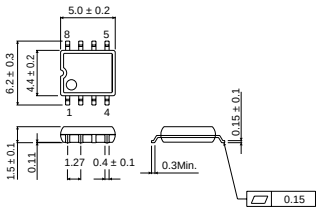
●**External dimension** (Units : mm)

BR9080ARFVM-W
BR9016ARFVM-W



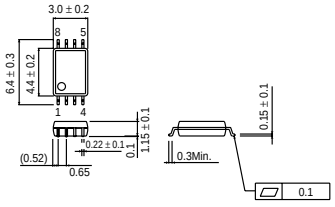
MSOP8

BR9080AF
BR9016AF



SOP8

BR9080ARFV
BR9016ARFV



SSOP-B8

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