32-Channel LCD Driver with Separate Backplane Output

Features

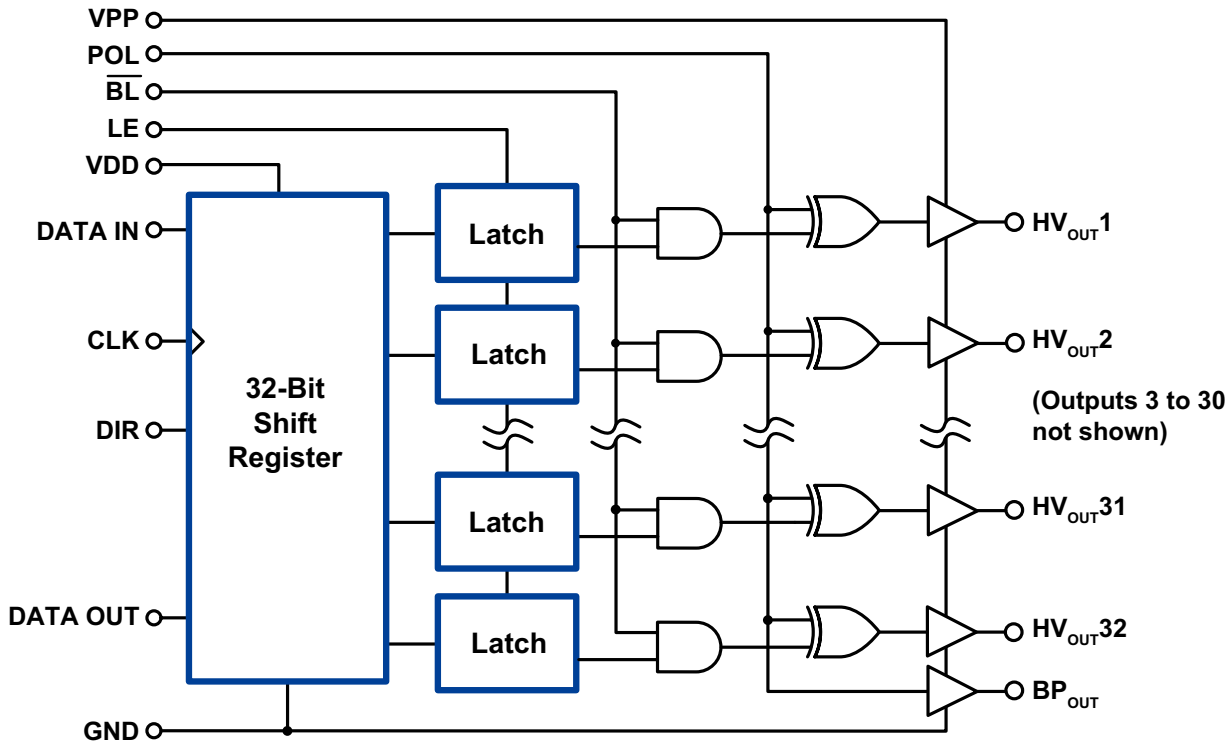
- HVCMOS® technology
- 32 push-pull CMOS output up to 60V
- Low power level shifting
- Shift register speed 5.0MHz
- Latched data outputs
- Bidirectional shift register (DIR)
- Backplane output

General Description

The HV66 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a driver circuit for LCD displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform blanking and polarity control of the outputs. $HV_{OUT}1$ is connected to the first stage of the shift register. Data is shifted through the shift register on the logic rising transition of the clock. A DIR pin causes data shifting clockwise when grounded and counter clockwise when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the LE (latch enable), $\overline{BL}$ (blank) or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored after LE transitions from high to low.

Functional Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV66PG-G	44-Lead PQFP	96/Tray
HV66PG-G M919	44-Lead PQFP	500/Reel
HV66PJ-G	44-Lead PLCC	27/Tube
HV66PJ-G M903	44-Lead PLCC	500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings[1]

Parameter	Value
Supply voltage, V_{DD}[2]	-0.5V to +7.0V
Supply voltage, V_{PP}[2]	-0.5V to +70V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[3]	1.5A
Continuous total power dissipation[4]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +125°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

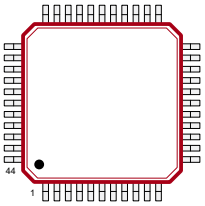
Notes:

1. *Device will survive (but operation may not be specified or guaranteed) at these extremes*
2. *All voltages are referenced to GND*
3. *Duty cycle is limited by the total power dissipated in the package*
4. *For operation above 25°C ambient derate linearly to 85°C at 20mW/°C*

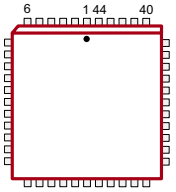
Typical Thermal Resistance

Package	θ_{ja}
44-Lead PQFP	51°C/W
44-Lead PLCC	37°C/W

Pin Configuration



44-Lead PQFP
(top view)

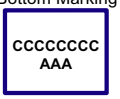


44-Lead PLCC
(top view)

Product Marking

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PQFP

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
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**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PLCC

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	High voltage supply	12	60	V
V_{IH}	High-level input voltage	2.4	V_{DD}	V
V_{IL}	Low-level input voltage	0	0.8	V
f_{CLK}	Clock frequency	0	5.0	MHz
T_A	Operating free-air temperature	-40	+85	°C
I_{OD}	Allowable current through output diodes	-	200	mA

Electrical Characteristics *(over recommended operating conditions unless otherwise noted)*

DC Characteristics *(V_{DD} = 5.0V, V_{PP} = 60V)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	V_{DD} = 5.5V, f_{CLK} = 5.0MHz
I_{PPQ}	Quiescent V_{PP} supply current		-	0.5	mA	Outputs high
			-	0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		-	0.5	mA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	50	-	V	I_O = -5.0mA, V_{PP} = +60V
		DATA OUT	4.6	-		I_O = -100µA
V_{OL}	Low-level output	HV_{OUT}	-	8.0	V	I_O = +5.0mA, V_{PP} = +60V
		DATA OUT	-	0.4		I_O = +100µA
I_{IH}	High-level input current		-	1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level input current		-	-1.0	µA	V_{IL} = 0V
V_{OLBP}	Low-level output voltage, backplane		-	3.0	V	I_O = +10mA
V_{OHBP}	High-level output voltage, backplane		57	-	V	I_O = -10mA

AC Characteristics *(V_{DD} = 5.0V, V_{PP} = 60V, T_A = 25°C, logic input rise/fall time = 10ns.)*

f_{CLK}	Clock frequency	-	5.0	MHz	---
$t_{WL,}$ t_{WH}	Clock width high or low	100	-	ns	---
t_{SU}	Data set-up time before clock rises	25	-	ns	---
t_H	Data hold time after clock rises	50	-	ns	---
t_{HON}, t_{HOFF}	Time from latch enable or POL to HV_{OUT}	-	500	ns	C_L = 20pF
t_{BON}, t_{BOFF}	Time from POL to BP_{OUT}	-	500	ns	C_L = 20pF
t_{DHL}	Delay time clock to data high to low	-	200	ns	C_L = 10pF
t_{DLH}	Delay time clock to data low to high	-	200	ns	C_L = 10pF
t_{DLE}	Delay time clock to LE low to high	50	-	ns	---
t_{WLE}	Width of LE pulse	100	-	ns	---
t_{SLE}	LE set-up time before clock rises	50	-	ns	---
t_{BR}, t_{BF}	BP_{OUT} rise/fall time	10	1000	µs	C_L = 350pF
$\|t_{BR} - t_{BF}\|$	BP_{OUT} rise and fall difference	-	100	µs	C_L = 350pF

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, EN, etc.) to a known state.
4. Apply V_{PP}.

The V_{PP} should not drop below V_{DD} during operation.

Power-down sequence should be the reverse of the above.

Function Table

Function	Inputs						Outputs			
	Data	CLK	LE	$\overline{BL}$	POL	DIR	Shift Reg 1, 2, ... 32	HV_{OUT} 1, 2, ... 32	Data Out	BP_{OUT}
Load S/R, R/L Shift	L or H	↑	L	Ignore	Ignore	H	Data → Q_1... → Q_{32}	Ignore	Q_{32}	Ignore
	L or H	↑	L	Ignore	Ignore	L	Q_1← ...Q_{32} ← Data	Ignore	Q_1	Ignore
Load Latches	X	H or L	H	H	H	X	*...*	/*...*	No Change	H
	X	H or L	H	H	L	X	*...*	*...*	No Change	L
Transparent Mode	L or H	↑	H	H	H	H	Data → Q_1... → Q_{32}	/*...*	Q_{32}	H
	L or H	↑	H	H	L	H	Data → Q_1... → Q_{32}	*...*	Q_{32}	L
	L or H	↑	H	H	H	L	Q_1← ...Q_{32} ← Data	/*...*	Q_1	H
	L or H	↑	H	H	L	L	Q_1← ...Q_{32} ← Data	*...*	Q_1	L
Blank Control	X	X	X	L	L	X	X	L...L	Ignore	L
	X	X	X	L	H	X	X	H...H	Ignore	H

Notes:

H - *High level*

L - *Low level*

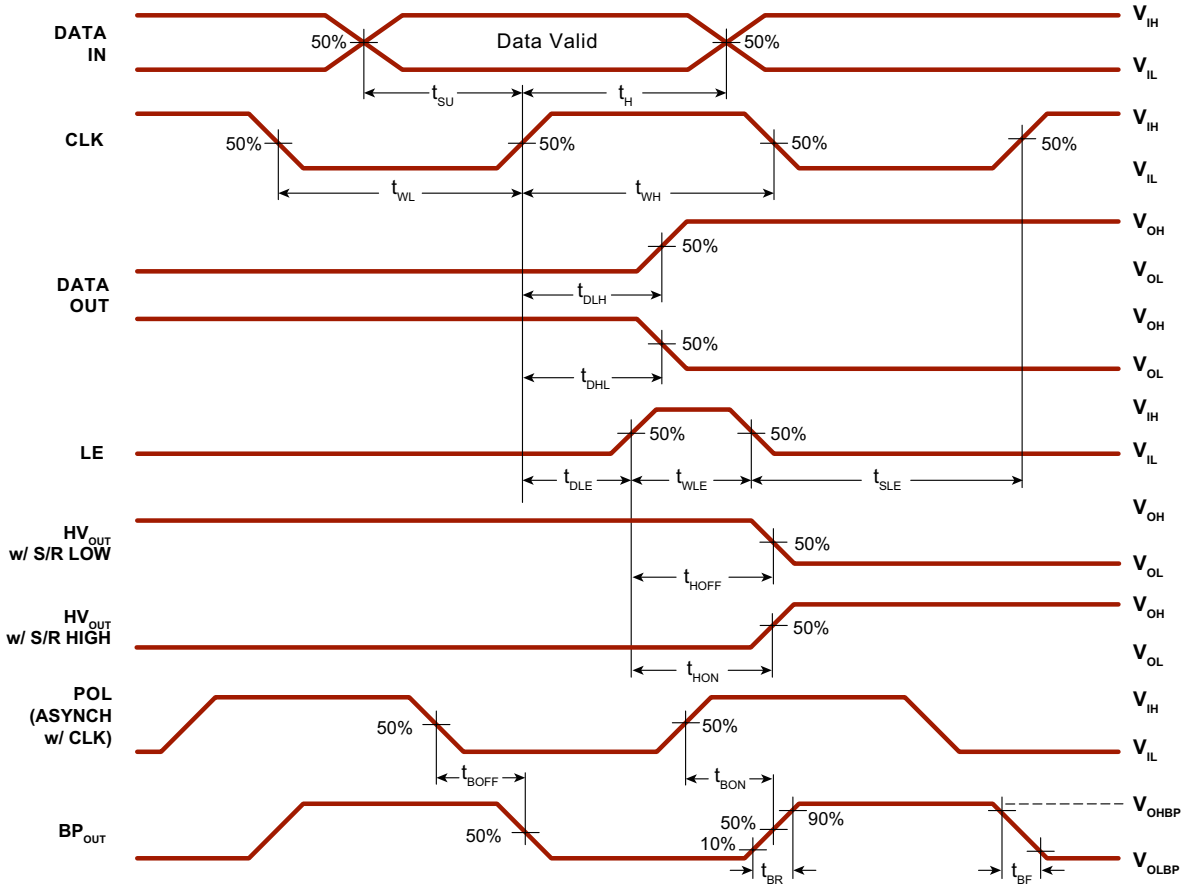
X - *Don't care*

Ignore - *The state of the specific input or output is irrelevant to demonstrate the occurred event*

↑ - *Low to High transition*

* - *Dependent on previous stage's state before the last CLK or last LE high*

Switching Waveforms



44-Lead PQFP Pin Description

Pin #	Function
1	$HV_{OUT}11$
2	$HV_{OUT}12$
3	$HV_{OUT}13$
4	$HV_{OUT}14$
5	$HV_{OUT}15$
6	$HV_{OUT}16$
7	$HV_{OUT}17$
8	$HV_{OUT}18$
9	$HV_{OUT}19$
10	$HV_{OUT}20$
11	$HV_{OUT}21$
12	$HV_{OUT}22$
13	$HV_{OUT}23$
14	$HV_{OUT}24$
15	$HV_{OUT}25$

Pin #	Function
16	$HV_{OUT}26$
17	$HV_{OUT}27$
18	$HV_{OUT}28$
19	$HV_{OUT}29$
20	$HV_{OUT}30$
21	$HV_{OUT}31$
22	$HV_{OUT}32$
23	DATA OUT
24	GND
25	N/C
26	$\overline{BL}$
27	POL
28	LE
29	VDD
30	CLK

Pin #	Function
31	DIR
32	DATA IN
33	VPP
34	BP_{OUT}
35	$HV_{OUT}1$
36	$HV_{OUT}2$
37	$HV_{OUT}3$
38	$HV_{OUT}4$
39	$HV_{OUT}5$
40	$HV_{OUT}6$
41	$HV_{OUT}7$
42	$HV_{OUT}8$
43	$HV_{OUT}9$
44	$HV_{OUT}10$

44-Lead PLCC Pin Description

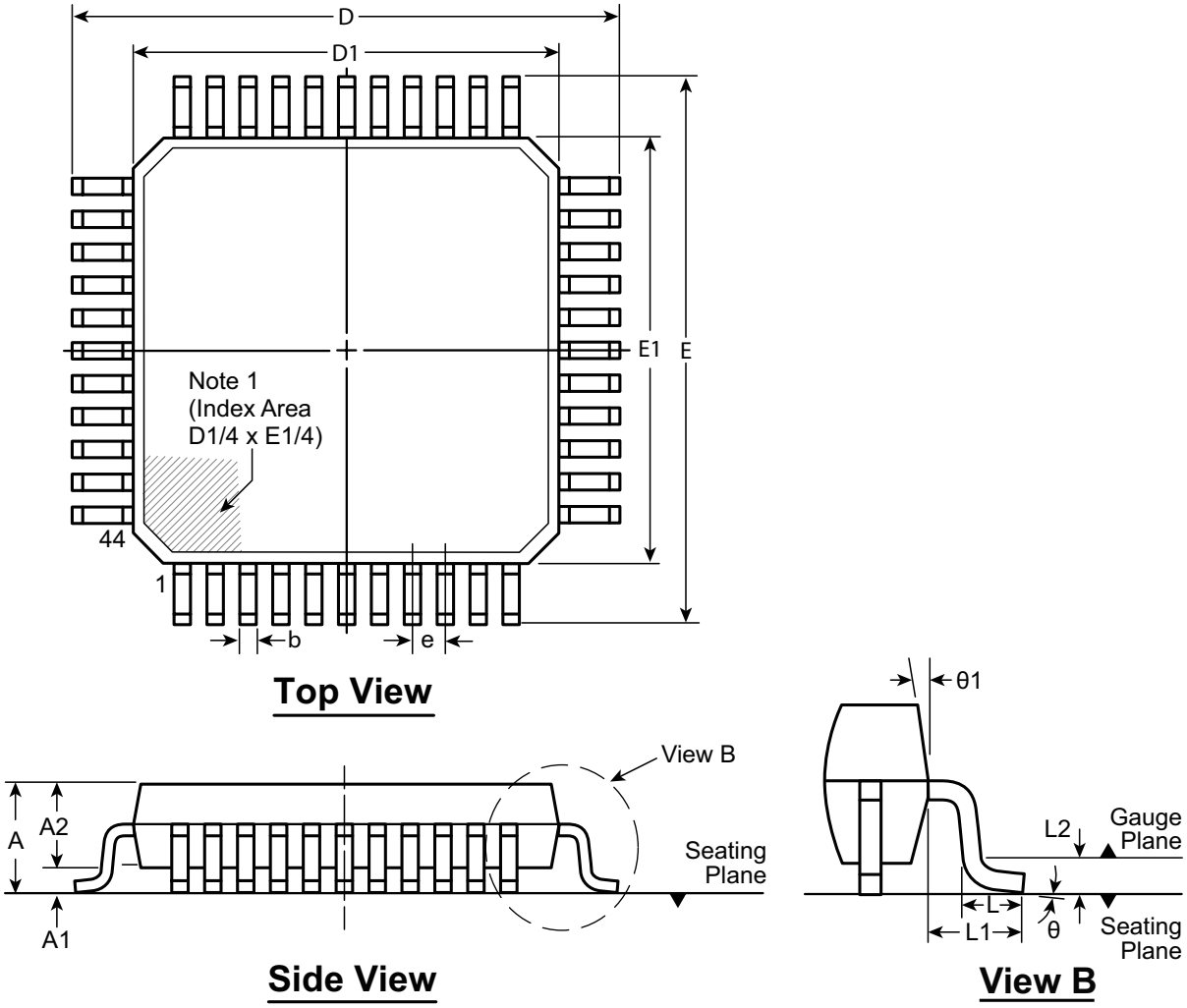
Pin	Function
1	$HV_{OUT}16$
2	$HV_{OUT}17$
3	$HV_{OUT}18$
4	$HV_{OUT}19$
5	$HV_{OUT}20$
6	$HV_{OUT}21$
7	$HV_{OUT}22$
8	$HV_{OUT}23$
9	$HV_{OUT}24$
10	$HV_{OUT}25$
11	$HV_{OUT}26$
12	$HV_{OUT}27$
13	$HV_{OUT}28$
14	$HV_{OUT}29$
15	$HV_{OUT}30$

Pin	Function
16	$HV_{OUT}31$
17	$HV_{OUT}32$
18	DATA OUT
19	GND
20	N/C
21	$\overline{BL}$
22	POL
23	LE
24	VDD
25	CLK
26	DIR
27	DATA IN
28	VPP
29	BP_{OUT}
30	$HV_{OUT}1$

Pin	Function
31	$HV_{OUT}2$
32	$HV_{OUT}3$
33	$HV_{OUT}4$
34	$HV_{OUT}5$
35	$HV_{OUT}6$
36	$HV_{OUT}7$
37	$HV_{OUT}8$
38	$HV_{OUT}9$
39	$HV_{OUT}10$
40	$HV_{OUT}11$
41	$HV_{OUT}12$
42	$HV_{OUT}13$
43	$HV_{OUT}14$
44	$HV_{OUT}15$

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note:

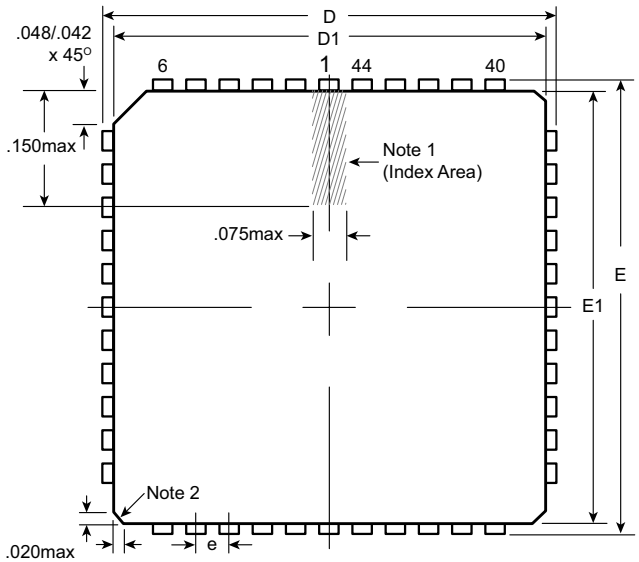
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

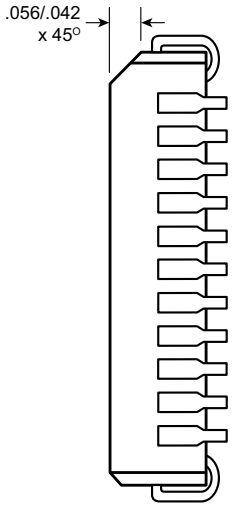
JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex** Doc. #: DSPD-44PQFPPG, Version C041309.*

44-Lead PLCC Package Outline (PJ)

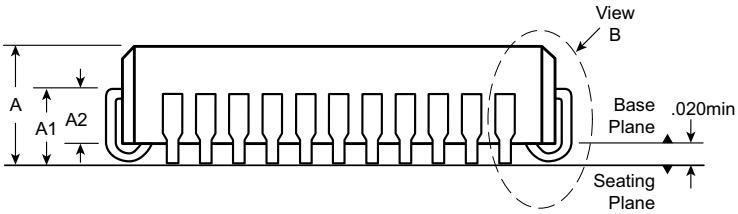
.653x.653in body, .180in height (max), .050in pitch



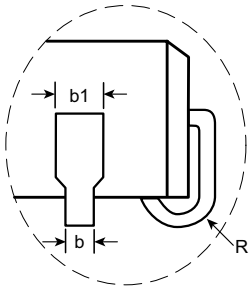
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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