HOTLink® CY7B933 $\overline{\text{RDY}}$ Pin Description

This application note describes the behavior of the $\overline{\text{RDY}}$ (Ready) pin in several modes of operation: Encoded, Bypass, and BIST (Built-In Self-Test). The $\overline{\text{RDY}}$ pin indicates the status of the HOTLink® Receiver control logic and output pins. Its function and timing are dependent on the state of the MODE, $\overline{\text{BISTEN}}$ (Built-In Self-Test Enable), and RF (Reframe) pins. The following sections describe $\overline{\text{RDY}}$ behavior in detail.

Normal $\overline{\text{RDY}}$ Timing

The HOTLink CY7B933 datasheet specifies signal transitions for the receiver in bit-times relative to the rising edge of CKR. A bit-time refers to the period of the internal receiver bit-rate clock. The period of the recovered byte-rate clock, CKR, is ten times the bit period (bit period $t_B = t_{CKR} \div 10$). In the following discussions on timing, the rising edge of CKR is referenced as bit-time zero. The next rising edge of CKR occurs ten bit-times later (unless CKR stretches due to reframing). Transitions on other signal pins are defined in bit-times relative to bit-time zero. These timing conventions are adhered to throughout this application note.

The normal timing of the $\overline{\text{RDY}}$ pin refers to its behavior in Encoded or Bypass mode with $\overline{\text{BISTEN}}$ HIGH (Built-In Self-Test disabled). In either of these modes, $\overline{\text{RDY}}$ rests HIGH in its inactive state. During its active state, $\overline{\text{RDY}}$ transitions LOW on bit-time five and then transitions HIGH on bit-time one of the next clock cycle. *Figure 1* illustrates $\overline{\text{RDY}}$ timing in relation to CKR and DATA. For the exact timing margins[1] of these signals, refer to the HOTLink datasheet. In BIST mode, $\overline{\text{RDY}}$ assumes much different behavior and timing. These differences are explained later in the sections on BIST.

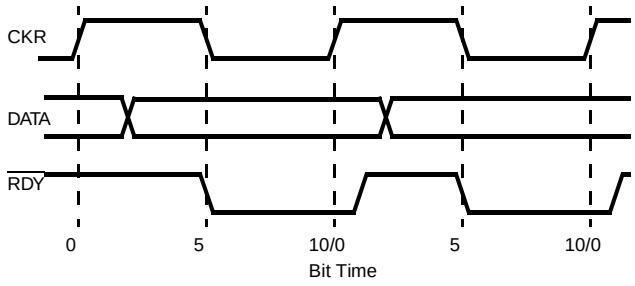

Figure 1. Normal $\overline{\text{RDY}}$ Timing

$\overline{\text{RDY}}$ in Encoded Mode

This section describes the operation of $\overline{\text{RDY}}$ in Encoded mode (MODE = LOW). In Encoded mode, the raw ten-bit serial data is decoded in the 10B/8B decoder and then presented at the parallel output pins.

Unframed Operation

Starting from a power-on situation, the receiver is in an unframed state. While unframed, the receiver will continue to output $\overline{\text{RDY}}$ pulses, as characters (either valid or invalid) are received, *Figure 2.*

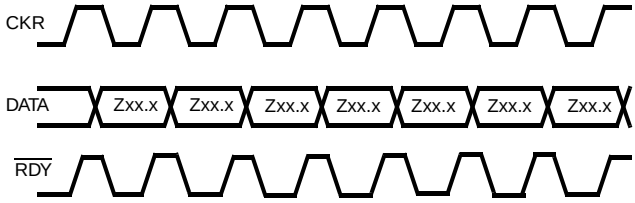

Figure 2. $\overline{\text{RDY}}$ in Unframed Operation

If RF is LOW (framing disabled), and some of these characters just happen to be SYNC (K28.5) characters, and they just happen to fall on the same character boundaries as the framer is presently operating, then these characters will also generate $\overline{\text{RDY}}$ pulses just like the other characters, as shown in *Figure 3.*

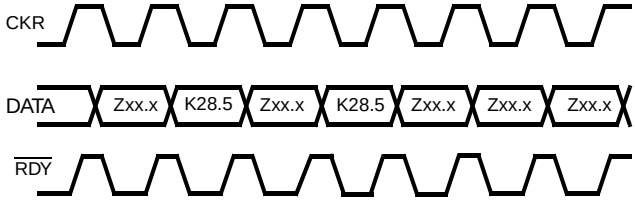

Figure 3. $\overline{\text{RDY}}$ Prior to Framing

If by chance (or design) more than one K28.5 character is received as continuous characters, the receiver will only generate a $\overline{\text{RDY}}$ pulse on the last K28.5 in the string, as shown below in *Figure 4.*

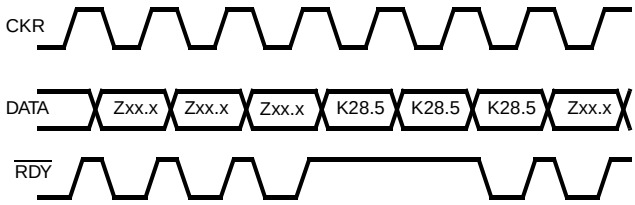

Figure 4. $\overline{\text{RDY}}$ Pulse on Last in a String of K28.5s

The receiver has not yet gone through any framing operation. The only reason that the $\overline{\text{RDY}}$ signal goes HIGH is because a string of K28.5s was received that matched the character boundaries that the receiver powered up with. If these exact same K28.5s were received offset in time by one bit, the receiver would decode these as some type of valid or invalid character (mostly invalid), and would generate a $\overline{\text{RDY}}$ pulse on every one.

Normal Operation

The normal operation of the $\overline{\text{RDY}}$ pin in Encoded mode (MODE = LOW, RF = LOW, $\overline{\text{BISTEN}}$ = HIGH) is to signal when new data is available at the parallel output pins (Q_{0-7}, SC/$\overline{\text{D}}$, RVS). $\overline{\text{RDY}}$ pulses LOW with a 60% LOW/40% HIGH duty cycle only when new data is present at the output. The timing of $\overline{\text{RDY}}$ is optimized for a seamless interface to industry standard FIFOs (First-In First-Out memories). $\overline{\text{RDY}}$ does not pulse LOW in a field of SYNC (K28.5) characters; however, $\overline{\text{RDY}}$ does pulse LOW for the last K28.5 in the field or for any single K28.5. This behavior helps prevent a FIFO from filling with meaningless strings of SYNC characters. *Figure 5* illustrates normal $\overline{\text{RDY}}$ behavior in Encoded mode.

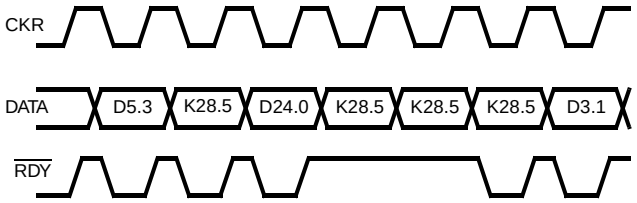

Figure 5. Normal $\overline{\text{RDY}}$ Operation in Encoded Mode

Entering Framing

When the RF pin is asserted HIGH, the receiver byte framer is enabled and the $\overline{\text{RDY}}$ pin leaves normal Encoded mode operation. The receiver latches the RF signal on the falling edge of CKR[2]. When RF is latched HIGH, $\overline{\text{RDY}}$ is forced HIGH one bit time after the next rising edge of CKR (approximately $6t_B$ later). The exception to this is when there is a K28.5 in the framer when RF is asserted HIGH. In this case, an additional $\overline{\text{RDY}}$ pulse will occur after RF is latched HIGH. $\overline{\text{RDY}}$ will then pulse LOW when the data byte boundary is framed to an incoming SYNC character (K28.5). The timing of $\overline{\text{RDY}}$ while entering framing is outlined in *Figure 6*. The dotted $\overline{\text{RDY}}$ signal shows the additional pulse due to a K28.5 being present in the framer when RF is asserted HIGH. When this happens the K28.5 will be presented on the output bus as either C5.0, C1.7 or C2.7.

Another situation occurs if a string of properly framed K28.5s is being received when the RF pin is asserted (the K28.5 filter is already operating). In this case, the $\overline{\text{RDY}}$ pin will pulse once during the fourth clock cycle after $\overline{\text{RDY}}$ is latched to indicate proper reframing. This is the only case that will cause a $\overline{\text{RDY}}$ pulse during the fourth clock cycle after RF is latched. The timing of $\overline{\text{RDY}}$ for this case is shown in *Figure 7*.

$\overline{\text{RDY}}$ will never pulse LOW on the third clock period following RF being latched. The latency of the receiver data pipeline and control logic insure that $\overline{\text{RDY}}$ will not pulse LOW to indicate a proper reframe any earlier than the third clock cycle

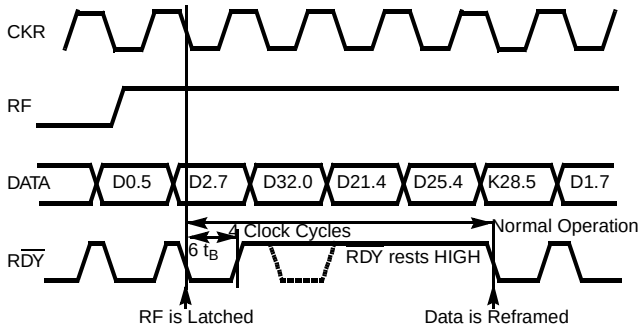

Figure 6. $\overline{\text{RDY}}$ During Framing in Encoded Mode

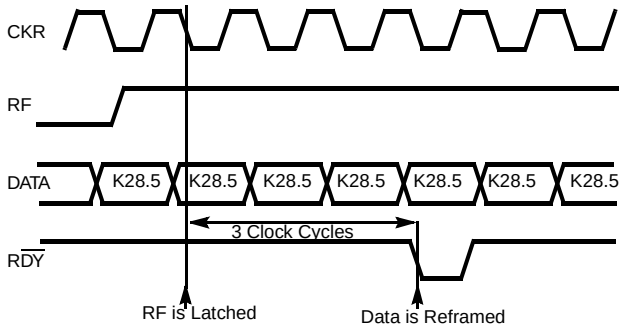

Figure 7. $\overline{\text{RDY}}$ During Framing in Encoded Mode While Receiving a Stream of K28.5s

after RF is latched HIGH. External framing logic should be designed to examine the $\overline{\text{RDY}}$ pin only after the three-clock-cycle delay. However, for the majority of cases, the $\overline{\text{RDY}}$ pulse that indicates proper reframing will not occur any earlier than the fourth clock cycle after RF is latched.

In summary, normal data will place a $\overline{\text{RDY}}$ pulse in the first clock cycle after RF is latched. If a K28.5 was present in the framer when RF was latched a $\overline{\text{RDY}}$ pulse will occur in the second clock cycle after RF is latched. A $\overline{\text{RDY}}$ pulse can never occur in the third clock cycle after RF is latched. If a string of K28.5's is received a $\overline{\text{RDY}}$ pulse will occur in the fourth clock cycle after RF is latched and for all other cases, the earliest that framing can occur is following the fourth clock cycle. Therefore if $\overline{\text{RDY}}$ ever pulses LOW at or beyond the fourth clock cycle the receiver is properly framed. If $\overline{\text{RDY}}$ has never pulsed LOW, this indicates that the receiver has still not located a K28.5 framing character. The receiver continues to operate this way until it enters multi-byte framing mode.

After the data has been framed, $\overline{\text{RDY}}$ will assume its normal Encoded mode behavior (pulsing LOW for every character except strings of K28.5s). If RF remains HIGH, the framer still continues to frame the data to any K28.5 pattern found in the data stream. If RF is asserted HIGH for more than 2048 REFCLK cycles, the framer converts to a double-byte framer requiring two K28.5s within five bytes for framing. The function and timing of $\overline{\text{RDY}}$, however, remain unchanged.

Leaving Framing

When RF is deasserted, the framer is disabled and the $\overline{RDY}$ pin assumes its normal Encoded mode operation. If the data was framed during the assertion of RF, $\overline{RDY}$ will have already assumed its normal operation. If the framer is disabled without having framed the data, one clock cycle will pass before $\overline{RDY}$ assumes normal operation. *Figure 8* shows the framer being disabled before the data is framed. $\overline{RDY}$ resumes normal operation one cycle after RF is latched LOW.

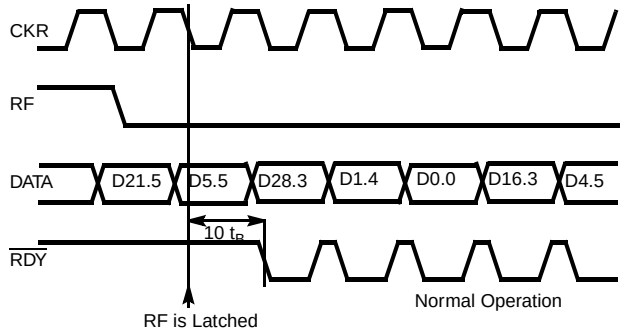

Figure 8. $\overline{RDY}$ While Leaving Framing

Multi-byte Framing

The multi-byte framer is enabled if RF is asserted HIGH for approximately 2048 byte clocks[3]. Once multi-byte framing is enabled, the requirements for framing change and the indication that framing has occurred also changes. If a K28.5 character has never been received following RF first being latched HIGH, then the $\overline{RDY}$ line will still be HIGH. It will remain HIGH until the receiver finally frames. If the $\overline{RDY}$ line ever starts to pulse LOW, this indicates that framing has occurred at least once. If $\overline{RDY}$ has not pulsed LOW at least once before the multi-byte framer is enabled, then it will take two K28.5s to finally frame the receiver.

Once the multi-byte framer is enabled, and the part has framed at least once since RF went HIGH, the $\overline{RDY}$ line cannot be used to indicate that framing has occurred. The receiver data bus can be used instead however. If any form of K28.5 (C5.0, C1.7 or C2.7) is ever output on the receiver output bus, then there was at least one K28.5 on the same character boundaries somewhere in the previous four characters. This also means that all of the following characters should be received correctly. If one, two or three characters are located between the two K28.5 characters, these intermediate characters can be anything. They do not have to be valid 8B/10B characters, they do not have to have valid running disparity[4], but they must all be exactly 10-bits in length.

$\overline{RDY}$ in Bypass Mode

This section describes the operation of $\overline{RDY}$ in Bypass mode (MODE = HIGH). In Bypass mode, the raw ten bit serial data bypasses the 8B/10B decoder and is presented at the parallel output pins.

Normal Operation

The normal operation of the $\overline{RDY}$ pin in Bypass mode (MODE=HIGH, RF=LOW, $\overline{BISTEN}$=HIGH) is to signal when a data pattern matching K28.5 character is present on the receiver's parallel output pins (Q_{a-j}). $\overline{RDY}$ will remain HIGH during all other data patterns. *Figure 9* shows an example of $\overline{RDY}$ in Bypass mode.

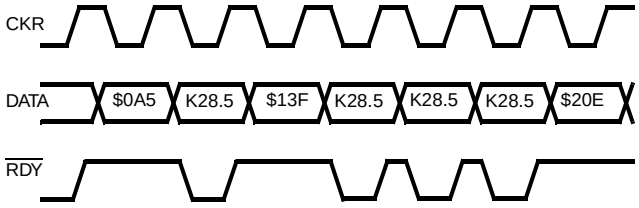

Figure 9. Normal $\overline{RDY}$ Operation in Bypass Mode

Entering Framing

The behavior of $\overline{RDY}$ while entering framing from Bypass mode is very similar to entering from Encoded mode. When RF is latched HIGH, $\overline{RDY}$ leaves normal Bypass mode operation and is forced HIGH one bit time after the next rising edge of CKR. When the framer is enabled, a LOW pulse on $\overline{RDY}$ indicates that the serial data has been framed to an incoming SYNC character (K28.5). The latency of the data pipeline and control logic insure that $\overline{RDY}$ does not pulse LOW any earlier than the third clock cycle after RF is latched HIGH. External framing logic should be designed to examine the $\overline{RDY}$ pin only after the three-clock-cycle delay. As in Encoded mode, the $\overline{RDY}$ pin pulses LOW to indicate proper framing after three clock cycles for the case where a string of properly framed K28.5s are being received when the RF pin is asserted. If a string of K28.5s is not being received, then the $\overline{RDY}$ pulse will not occur until at least four clock cycles have passed. After the data has been framed, $\overline{RDY}$ assumes its normal Bypass mode behavior (pulsing LOW only on K28.5 characters). While RF is HIGH, the framer continues to frame the data to any K28.5 pattern in the data stream. The timing of $\overline{RDY}$ while entering framing from Bypass mode is outlined in *Figure 10*.

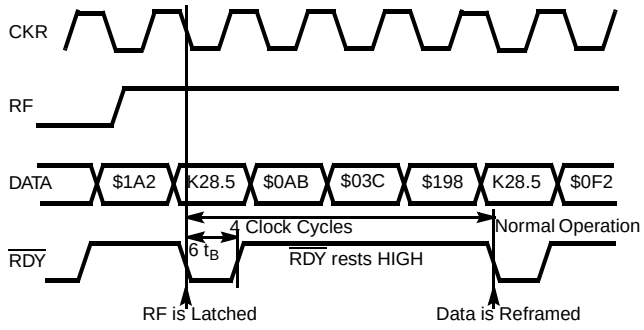

Figure 10. $\overline{RDY}$ During Framing in Bypass Mode

Leaving Framing

When RF is deasserted (LOW), the framer is disabled and the RDY pin assumes normal Bypass mode behavior. If the data was framed during the assertion of RF, RDY will have already assumed its normal operation. If Reframe is exited without having framed the data, one clock cycle passes before RDY assumes normal operation. *Figure 11* shows RF deasserted before the serial data has been framed.

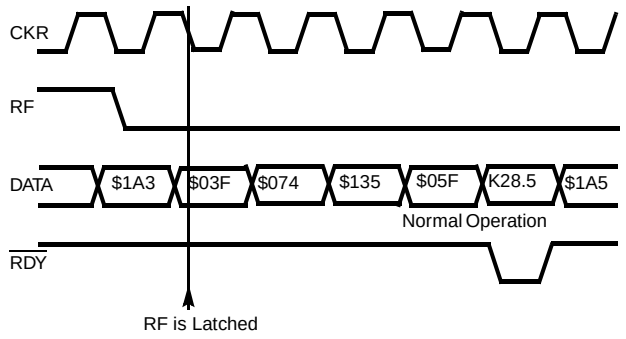

Figure 11. RDY While Leaving Framing

RDY and CKR Stretching

During framing (RF = HIGH), RDY and CKR may stretch as the byte boundary is synchronized to an incoming K28.5 character. If a K28.5 pattern is found in the serial data stream that is not aligned with the current byte boundary, the framer will realign the phase of CKR so that the receiver shift register properly deserializes the K28.5 character (and the following data). The HIGH or LOW phase of CKR and RDY will be stretched so that these signals maintain proper byte synchronization with the data. *Figure 12* shows RDY and CKR being stretched during framing due to a K28.5 character in the data stream. In this example, RF is held HIGH so that the framer remains enabled after RDY has assumed its normal operation according to the MODE pin (Encoded mode). The period of RDY and CKR may stretch up to a length of 19 bit-times depending on the position of the K28.5 character relative to the old byte boundary. Note that the K28.5 character comes out of the receiver one cycle after the CKR and RDY stretch due to the receiver pipeline.

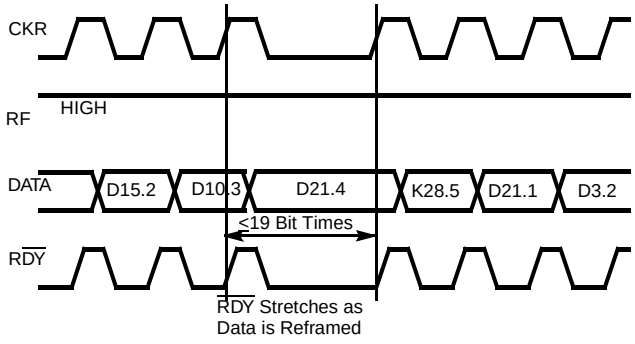

Figure 12. RDY and CKR Stretching (Encoded Mode)

RDY in BIST Mode

The Built-In Self-Test (BIST) feature provides a simple but exhaustive method for testing the integrity of the physical link. BIST Mode is entered by asserting the BISTEN pin LOW in either Encoded or Bypass mode. RDY has two normal modes of operation while in BIST. RDY initially rests HIGH when BIST is entered, signaling that the BIST logic has not started checking the received data. When a valid start of BIST sequence is received, the RDY pin will rest LOW, indicating that BIST checking is in progress. The timing of these transitions is discussed below. For more information on BIST, consult the "HOTLink Built-In Self-Test" application note.

Entering BIST Mode

BIST mode is entered by asserting BISTEN LOW. BISTEN is latched into the receiver on the falling edge of CKR. When BISTEN is latched LOW, RDY leaves its current mode of operation (Encoded or Bypass) and is asserted LOW for one full CKR cycle. On bit-time one of the next clock cycle, RDY is forced HIGH. The BIST logic will check the incoming data stream for the start of BIST sequence (D1.0 followed by D0.0). RDY rests HIGH while the BIST logic waits for this sequence. *Figure 13* shows the behavior of RDY when BISTEN is asserted LOW.

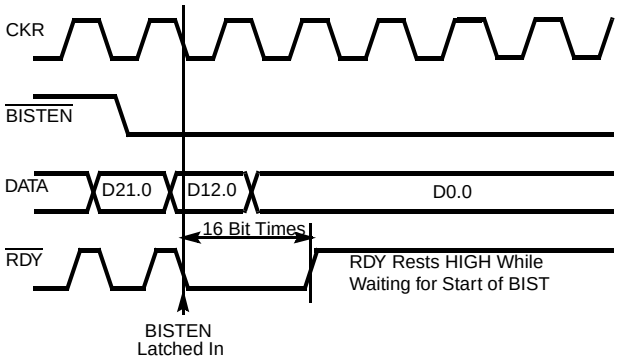

Figure 13. RDY while Entering BIST

Start of BIST

When the start of the BIST pattern is found, RDY will transition LOW one bit time after CKR rises. Due to the pipeline nature of the receiver, there is a one-cycle delay from when the start of BIST is detected and when RDY is asserted LOW. RDY will remain LOW for the duration of BIST except to pulse HIGH for one clock cycle each time a BIST Loop starts (once every 511 bytes). *Figure 14* shows the RDY pin during the start of BIST sequence.

BIST Loop

Figure 15 shows RDY behavior once BIST checking has begun. RDY rests LOW and pulses HIGH at the start of each new BIST loop. During this pulse, RDY rises on bit-time one and then falls one cycle later on bit-time one. This pulse is useful for counting the number of BIST loops complete.

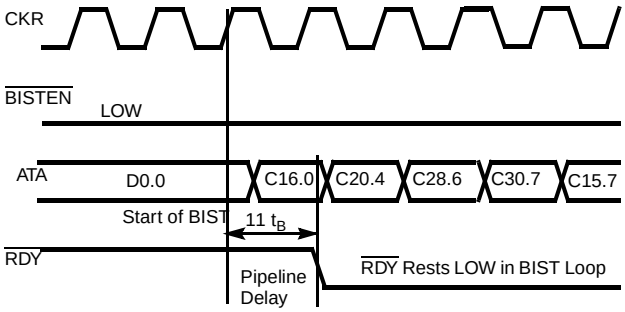

Figure 14. $\overline{RDY}$ at Start of BIST

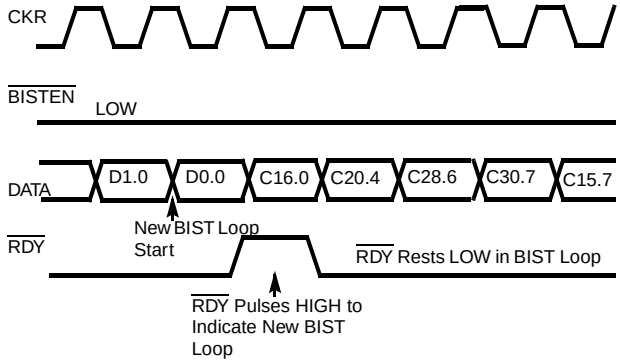

Figure 15. $\overline{RDY}$ in BIST Loop

Leaving BIST

BIST is disabled by setting $\overline{BISTEN}$ HIGH. $\overline{RDY}$ will assume the behavior dictated by the MODE pin (Encoded or Bypass) one clock cycle after $\overline{BISTEN}$ is latched HIGH. *Figure 16* shows the $\overline{RDY}$ pin while leaving BIST Mode.

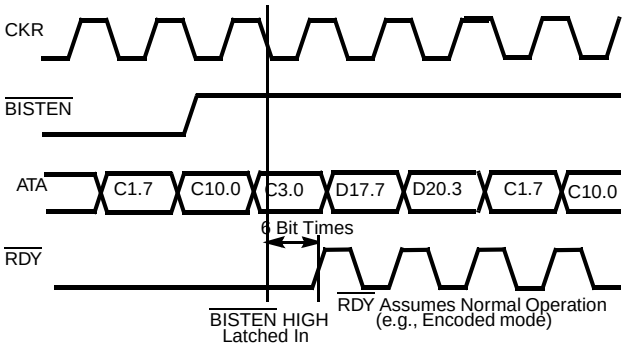

Figure 16. $\overline{RDY}$ While Leaving BIST

Framing While in BIST

Framing may be performed while in BIST Mode. The BIST pattern includes one alias K28.5 and several instances of byte aligned SYNC characters. If the framer is enabled (RF = HIGH), the data byte boundaries are aligned to any incoming K28.5 characters found in the serial data. $\overline{RDY}$ ceases its normal BIST behavior and rests HIGH while the framer waits for a K28.5 character. The timing for the $\overline{RDY}$ pin to be forced HIGH is the same as the timing discussed in the preceding sections on entering framing (i.e., $6t_B$ after RF is latched HIGH). When a K28.5 character is found, $\overline{RDY}$ will pulse LOW for one clock cycle. During this cycle, $\overline{RDY}$ falls on bit-time five and then rises on bit-time one of the next clock cycle. $\overline{RDY}$ then resumes its normal BIST behavior after one more clock cycle (see *Figure 17* and *Figure 18*).

Figure 17 shows RF asserted HIGH (framer enabled) while BIST is in the middle of checking the data. $\overline{RDY}$ initially rests LOW and then transitions HIGH when the framer is enabled. When a K28.5 character is found, $\overline{RDY}$ pulses LOW and then rests HIGH again. One cycle later, $\overline{RDY}$ transitions LOW as it resumes its normal BIST behavior (resting LOW during BIST).

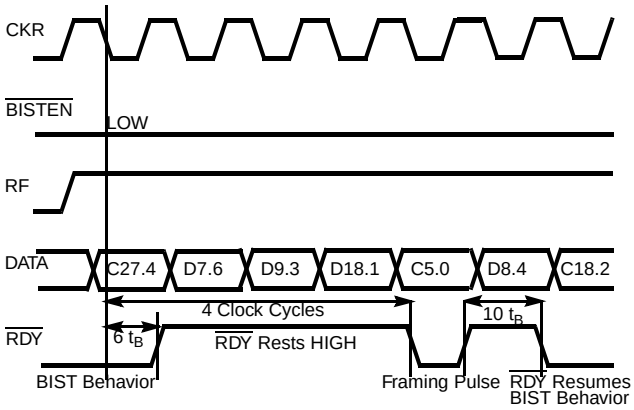

Figure 17. $\overline{RDY}$ While Framing in BIST

Figure 18 shows $\overline{RDY}$ behavior while BIST is waiting for the start of the BIST sequence. Initially, $\overline{RDY}$ rests HIGH while waiting for the start of the BIST sequence. When RF is asserted HIGH, the framer checks the serial data for a K28.5 character. $\overline{RDY}$ pulses LOW when a K28.5 is encountered and then returns HIGH. $\overline{RDY}$ then returns to its normal mode of operation (resting HIGH until start of BIST is received).

If RF is deasserted before a K28.5 is found by the framer, $\overline{RDY}$ will resume its normal BIST behavior on the next clock cycle.

Enabling the framer while in BIST Mode may cause the BIST data to become temporarily misaligned. If the enabled framer encounters the alias K28.5 character in the BIST data stream, the BIST data will be aligned to the incorrect byte boundary. This will result in a large number of errors reported on the RVS (Receive Violation Symbol) pin until the data is framed again to one of the properly aligned K28.5s. If RF is asserted HIGH for less than 2048 clock cycles, the BIST data will be misaligned each time the alias K28.5 is found (once per BIST loop). If RF is asserted for more than 2048 clock cycles (>4 BIST Loops), the double-byte framer will be enabled, and the framer will no longer frame the data to the alias K28.5 character.

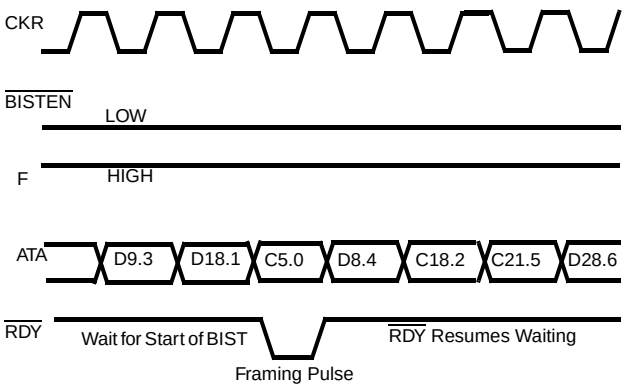

Figure 18. $\overline{\text{RDY}}$ While Framing in BIST

Conclusion

The Receiver $\overline{\text{RDY}}$ pin indicates the status of the control logic and data pins in various modes of operation. The behavior and timing of the $\overline{\text{RDY}}$ pin have been optimized for easy integration with interface control logic and FIFO memories. The detailed information contained in this application note should serve as an aid when integrating the $\overline{\text{RDY}}$ pin into the interface logic.

Notes

1. Data sheet timing parameters that are defined in terms of bit times (t_B) include additional timing margin to account for internal buffer and routing delays and output load (e.g., $t_A = 2t_B$ +4/–2 ns).
2. A minimum set-up time (from RF transitioning HIGH to the falling edge of CKR) is not specified as it is difficult to obtain a single number for this that is valid across all data rates and process corners. For most implementations this is not an issue. The link protocol is generally set up to make sure that it doesn't matter which edge RF is latched on. For those implementations that must know for sure on which CKR falling edge RF was latched it is necessary to monitor the action of RVS and the output data bus.
3. The 2048 is a worst-case number of byte clocks. This mode could actually be enabled as early as 2048-255 byte clocks from when RF is latched HIGH. This is because the byte counter that enables multi-byte framing is actually driven by the carry from a free-running divide-by-256 counter. Multi-byte framing is enabled following the eighth carry from this divide-by-256 counter. Since the free running counter is not cleared by RF, it is possible that the first carry pulse could occur immediately after RF is latched, or as late as 255 byte times after RF was latched.
4. In the HOTLink Receiver the character error detection logic is separate from the logic used for framing. They do not interact. This is why the received K28.5 characters do not have to have proper running disparity to allow framing to occur.

approved dsg 3/7/02