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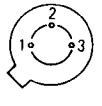
*Consult Motorola if a direct replacement is necessary.

TABLE 1 — METAL TO-204, TO-204AE (continued)

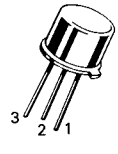
I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
50	200	BUS51•		15 min	50					350
	400	MJ10015•##		10 min	40	2.5	1	20		250
	500	BUT34•##		15 min	32	3	1.5	32		250
		MJ10016•##		10 min	40	2.5	1	20		250
56	400	BUT33•##		20 min	36	3.3	1.6	36		250
60	60	MJ14000•	MJ14001•	15/100	50					300
	80	MJ14002•	MJ14003•	15/100	50					300
	200	MJ10020•##		75 min	15	3.5	0.5	30		250
	250	MJ10021•##		75 min	15	3.5	0.5	30		250
70	125	BUS50•		15 min	50					350

• Modified TO-3, 60 mil pins, # $|h_{fe}|$ @ 1 MHz, ## Darlington

TABLE 2 — METAL TO-205 (Formerly TO-39)



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(Pin 3 connected to case)



CASE 79-04 (TO-205AD)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	300		MJ4646	20 min	0.5	0.72*		0.05	40	5
	400		MJ4647	20 min	0.5	0.72*		0.05	30	5
3	40		2N3719	25/180	1	0.4*		1	60	6
			2N3867	40/200	1.5	0.4*		1.5	60	6
	60		2N3720	25/180	1	0.4*		1	60	6
			2N3868	30/150	1.5	0.4*		1.5	60	6
	80		2N6303	30/150	1.5	0.4*		1.5	60	6
4	60	2N4877		20/100	4	1.5	0.5	4	4	10
5	80	2N5336	2N6190	30/120	2	2	0.2	2	30	6
		2N5337	2N6191	60/240	2	2	0.2	2	30	6
	100	2N5338		30/120	2	2	0.2	2	30	10
		2N5339	2N6193	60/240	2	2	0.2	2	30	6

*t_{off}

JAN, JTX, JTXV Available

2N6190
2N6191
2N6193

MEDIUM-POWER PNP SILICON TRANSISTORS

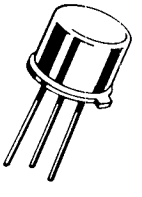
. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-205AD Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

5 AMPERE

POWER TRANSISTORS
PNP SILICON

80-100 VOLTS
10 WATTS



*MAXIMUM RATINGS

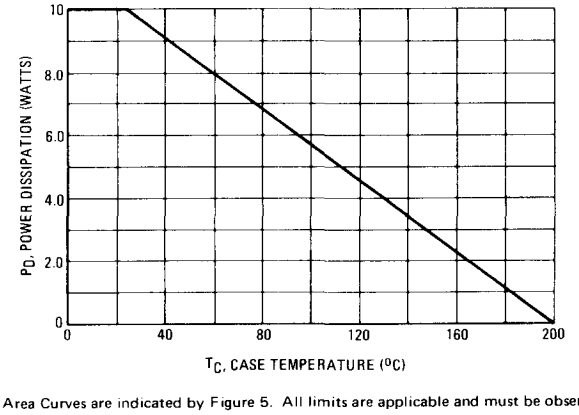
Rating	Symbol	2N6190 2N6191	2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	10		Watts
Derate above 25^oC		57.1		$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

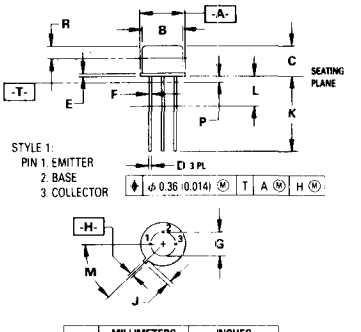
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

CASE 79-04
TO-205AD
(TO-39)

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* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6190, 2N6191		80	–	
	2N6193		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6190, 2N6191		–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6193		–	100	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6190, 2N6191		–	10	
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6193		–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6190, 2N6191		–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6193		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N6190, 2N6191		–	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N6193		–	10	
Emitter Cutoff Current		I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)			–	100	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N6190		30	–	
	2N6191, 2N6193		60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6190		30	120	
	2N6191, 2N6193		60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6190		20	–	
	2N6191, 2N6193		40	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)			–	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)			–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.8	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (2)		f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)			30	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)			–	300	
Input Capacitance		C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)			–	1250	
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc,	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 0.2 Adc)	t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) f_T = $|h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

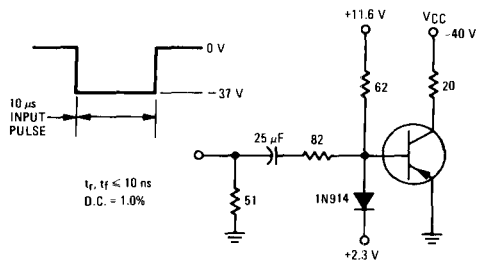


FIGURE 3 – TURN ON TIME

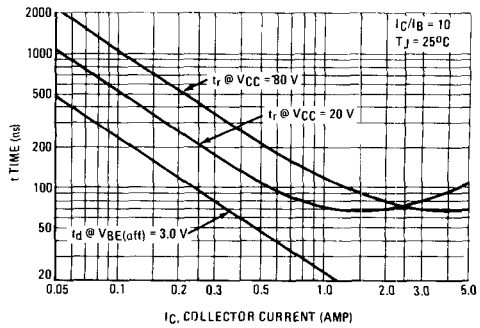


FIGURE 4 – THERMAL RESPONSE

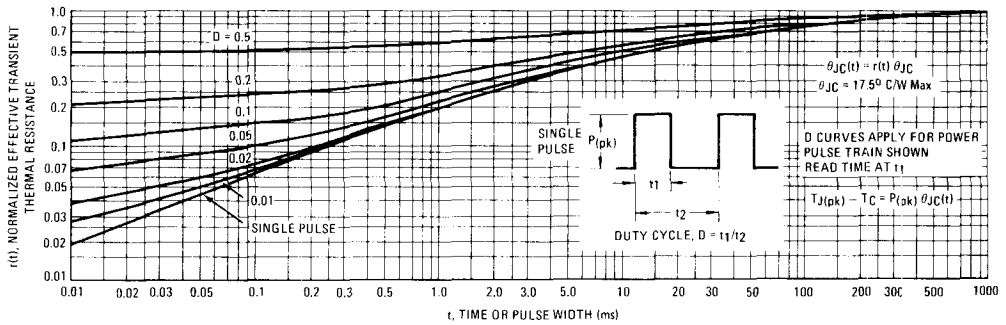
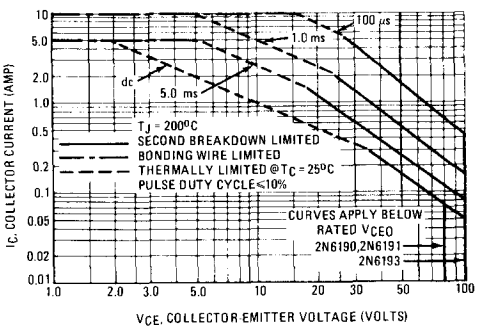


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitaitons imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

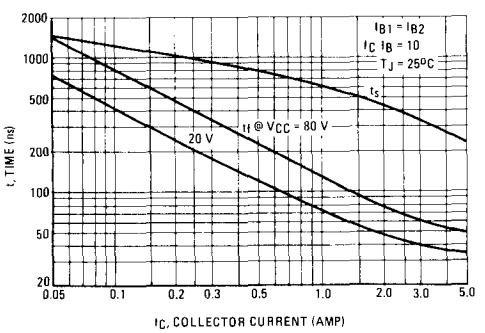


FIGURE 7 – CAPACITANCE versus VOLTAGE