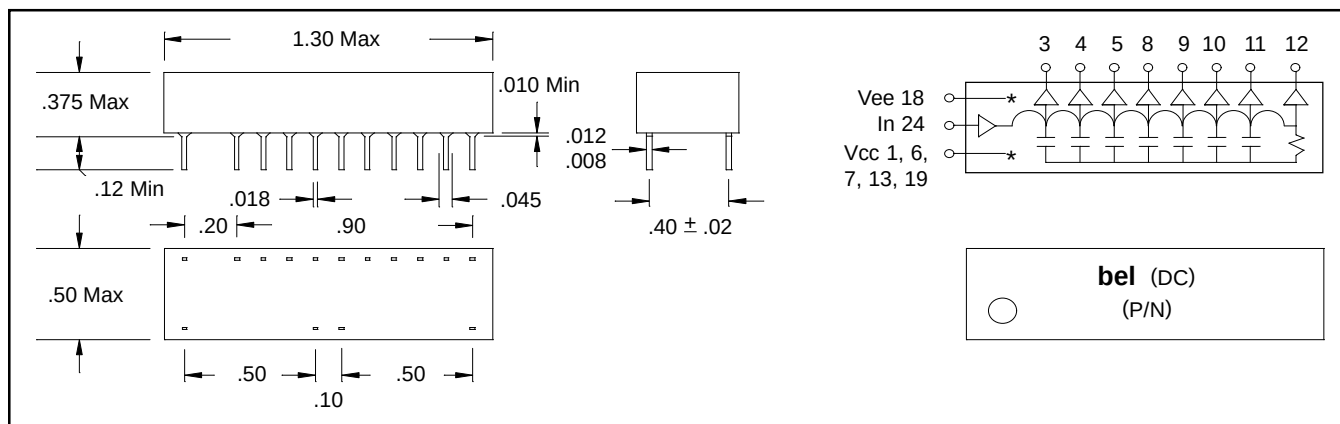


8 TAP LEADING EDGE CONTROL 100K ECL DELAY MODULES

Cat 42-R0



Part Numbers

Thru-Hole	Total Delay	Delay per Tap	Rise Time
0461-0016-01	16 ns	2.0 ns	3 ns
0461-0020-01	20 ns	2.5 ns	3 ns
0461-0024-01	24 ns	3.0 ns	3 ns
0461-0028-01	28 ns	3.5 ns	3 ns
0461-0032-01	32 ns	4.0 ns	3 ns
0461-0036-01	36 ns	4.5 ns	3 ns
0461-0040-01	40 ns	5.0 ns	3 ns
0461-0044-01	44 ns	5.5 ns	3 ns
0461-0048-01	48 ns	6.0 ns	3 ns
0461-0052-01	52 ns	6.5 ns	3 ns
0461-0056-01	56 ns	7.0 ns	3 ns
0461-0060-01	60 ns	7.5 ns	4 ns
0461-0064-01	64 ns	8.0 ns	4 ns
0461-0068-01	68 ns	8.5 ns	4 ns
0461-0072-01	72 ns	9.0 ns	4 ns
0461-0076-01	76 ns	9.5 ns	4 ns
0461-0080-01	80 ns	10.0 ns	4 ns

Test Conditions @ 25°C

Ein	Pulse Voltage, Logic 1	-0.9 Volts
	Pulse Voltage, Logic 0	-1.7 Volts
Trin	Rise Time	1.0 ns (20%-80%)
PW	Pulse Width	Total Delay + 10 ns
PP	Pulse Period	4 x Pulse Width
Vee	Supply Voltage	-5.0 Volts

Electrical Characteristics

		Min.	Max.	Units
V _{ee}	Supply Voltage	-4.2	-5.7	V
V _{ih}	Logic 1 Input Voltage	-1165	-870	mV
V _{il}	Logic 0 Input Voltage	-1830	-1475	mV
V _{oh}	Logic 1 Output Voltage	-1025	-870	mV
V _{ol}	Logic 0 Output voltage	-1830	-1620	mV
I _{ih}	Logic 1 Input Current		240	ua
I _{il}	Logic 0 Input Current	0.50		ua
T _a	Operating Free Air Temperature	0°	70°	C
PW	Min. Input Pulse Width of Total Delay	40		%
d	Maximum Duty Cycle		50	%
T _c	Temp. Coeff. of Total Delay (TD)	300 PPM/°C Typ.		

Tolerances

Input to Taps ± 1 ns or 4% , Whichever is Greater
Delays measured @ 50% levels on Leading Edge only
with outputs terminated in 50 ohm $\pm 1\%$ to -2 V
Rise Times measured from 20% to 80% levels

Notes

Epoxy encapsulated
Compatible with 100K ECL circuits
Performance warranty is limited to specified parameters listed

Drive Capabilities

Fan-out capabilities 70 ECL Loads Max.

Other Delays and Tolerances Available Consult Sales

Specifications subject to change without notice.

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