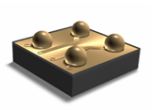
M24C64X-FCU M24C64X-FCP

Datasheet

64-Kbit serial I²C bus EEPROM with configurable device address and software write protection, delivered in 4-ball CSP



WLCSP
(CU, CP)

Product status link
M24C64X-FCU
M24C64X-FCP

Features

- Compatible with the 400 kHz I²C protocol
- High speed 1 MHz transfer rate
- Memory array:
  - 64 Kbit (8 Kbyte) of EEPROM
  - Page size: 32 byte
- Supply voltage range:
  - 1.7 V to 5.5 V over –40 °C / +85 °C
  - 1.6 V to 5.5 V over 0 °C / +85 °C
- Write
  - Byte write within 5 ms
  - Page write within 5 ms
- Random and sequential read modes
- Configurable device address
- Specific device address (on demand)
- Software write protection
- ESD protection
  - Human body model: 4 kV
- Enhanced ESD / Latch-Up protection
- More than 4 million write cycles
- More than 200-year data retention
- Package
  - RoHS and halogen free (ECOPACK2)

1 Description

This EEPROM device supports standard I²C instruction set.

The M24C64X is a 64-Kbit I2C-compatible EEPROM (electrically erasable programmable memory) organized as 8 K × 8 bits and delivered in a 4-ball WLCSP package.

The M24C64X can operate with a supply voltage of 1.7 V to 5 V, over an ambient temperature range of -40 °C/+85 °C. It can also operate down to 1.6 V, under some restricting conditions.

The M24C64X offers an additional 8-bit chip enable register for the configurable device address (CDA) and memory write protection feature.

On demand, the M24C64X can be delivered with a specific chip enable address.

Thanks to these two features, the device offers the configurable device address, authorizing, through software, to configure up to eight possibilities of chip enable address, and the write protection of the whole memory array, by setting, always through software, the software write protection bit.

Figure 1. Logic diagram

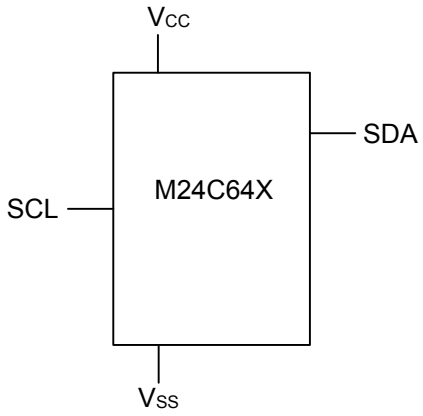


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial Data	I/O
SCL	Serial Clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. **4-bump WLCSP connections**

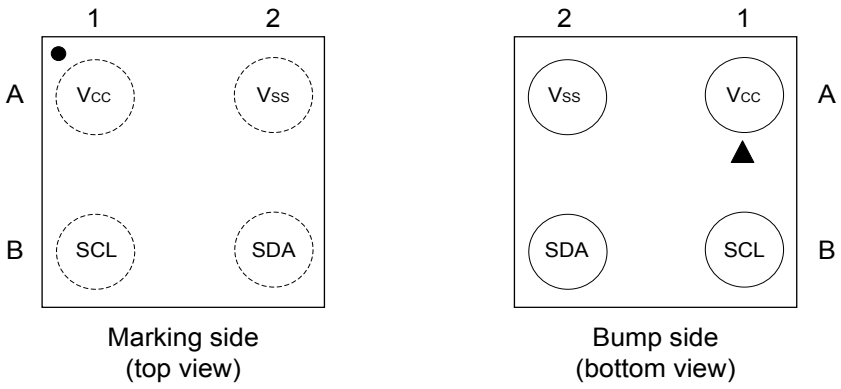


Table 2. **Signals vs. bump position**

Position	A	B
1	V_{CC}	SCL
2	V_{SS}	SDA

2 Signal description

2.1 Serial Clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (Figure 12 indicates how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 10. Operating conditions in Section 9 DC and AC parameters). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from 10 to 100 nF) close to the V_{CC} / V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Table 10. Operating conditions in Section 9 DC and AC parameters).

2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Table 10. Operating conditions in Section 9 DC and AC parameters). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range(see Table 10. Operating conditions in Section 9 DC and AC parameters).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

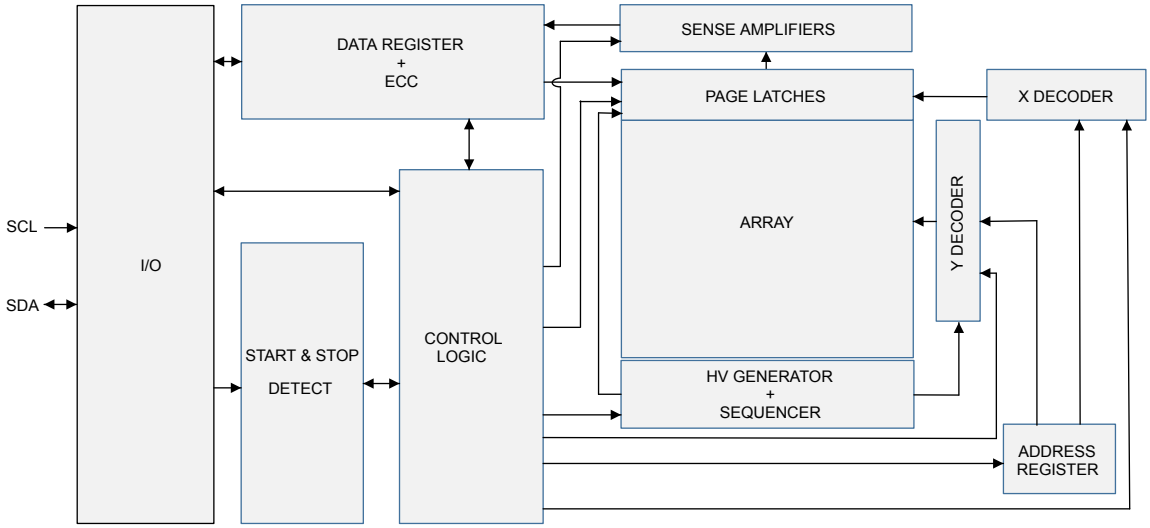
2.4.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

Figure 3. Block diagram



4 Features

4.1 Chip enable register

As the M24C64X is delivered in 4-ball WLCSP without chip enable inputs, the device provides a non-volatile 8-bit register allowing the user to define a configurable device address (CDA) and a software write protection. This register can be written and read with the device type identifier (1010b) and with a specific address.The description of the chip enable register is given Table 3.

Table 3. Chip enable register values

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x (1)	x(1)	x(1)	x(1)	C2	C1	C0	b0
				Configurable device address bit	Configurable device address bit	Configurable device address bit	SWP: Write protection activation bit

1. *x = Don't care bits.*

Bit 7:4 Don't care bits

Bits 3:1 Chip enable address configuration:

- (b3,b2,b1) = (0,0,0): the chip enable address is 000 (factory delivery value if no specific)
- (b3,b2,b1) = (0,0,1): the chip enable address is 001
- (b3,b2,b1) = (0,1,0): the chip enable address is 010
- (b3,b2,b1) = (1,0,0): the chip enable address is 100
- (b3,b2,b1) = (1,1,0): the chip enable address is 110
- (b3,b2,b1) = (1,1,1): the chip enable address is 111
- (b3,b2,b1) = (0,1,1): the chip enable address is 011
- (b3,b2,b1) = (1,0,1): the chip enable address is 101

Bit 0 Enables or disables the write protection of the memory array:

- b0 = 0: the whole memory array can be written and read (factory delivery value)
- b0 = 1: the whole memory array is write protected and is in read-only mode

4.2 Configurable device address

C2, C1 and C0 are defining the chip enable address in the Device Select Code. These bits can be written and re-configured with a Write command.

At power up or after reprogramming, the device loads the last configuration of C2, C1 and C0 values.

Factory delivery value is 000b if no specific request.

On demand, the C2,C1,C0 bit values can be programmed by STMicroelectronics. In this case, the factory delivery value by default is given Table 4.

The corresponding commercial product number with specific chip enable address are given in Table 4.

Table 4. Commercial product number versus chip enable address at factory delivery

Commercial product number	A digit	Chip enable address value at factory delivery		
		C2	C1	C0
M24C64X-FCUT/TF M24C64X-FCPT/TF	-	0	0	0
M24C64X-FCUT1TF M24C64X-FCPT1TF	1	0	0	1
M24C64X-FCUT2TF M24C64X-FCPT2TF	2	0	1	0
M24C64X-FCUT3TF M24C64X-FCPT3TF	3	0	1	1
M24C64X-FCUT4TF M24C64X-FCPT4TF	4	1	0	0
M24C64X-FCUT5TF M24C64X-FCPT5TF	5	1	0	1
M24C64X-FCUT6TF M24C64X-FCPT6TF	6	1	1	0
M24C64X-FCUT7TF M24C64X-FCPT7TF	7	1	1	1

4.3 Software write protect

In order to prevent unwanted write sequence, the M24C64X offers the SWP feature, which makes it possible to protect the whole memory content. write operations are disabled (read-only memory) when the SWP is set to 1 (SWP=1b). In the same way, the write operations are enabled when the SWP is set to 0 (SWP=0b).

Factory default values is 0b.

At power up, the device will load the last configuration of the SWP value.

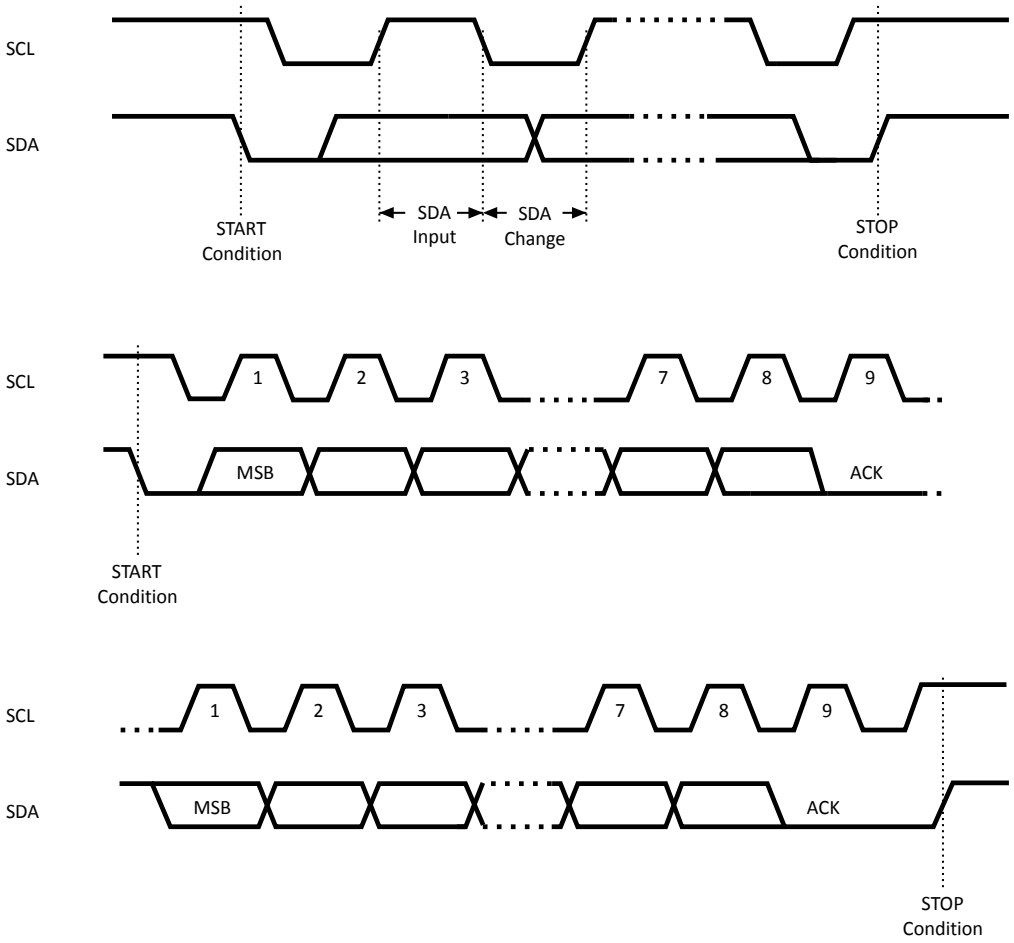
Updating the SWP to a new value is a reversible action: the SWP bit can be updated from 0 to 1 and from 1 to 0.

When SWP is set to '1', device select and address bytes are acknowledged, data bytes are not acknowledged.

5 Device operation

The device supports the I²C protocol. This is summarized in Figure 4. I²C bus protocol. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 4. I²C bus protocol



5.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

5.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

5.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven low.

5.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

5.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 5. Device select code on Serial Data (SDA), most significant bit first.

Table 5. Device select code

Device type identifier (1)				Chip enable address (2)			RW
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	C2	C1	C0	RW

1. *The most significant bit, b7, is sent first.*
2. *b3, b2 and b1 are compared with the C2, C1 and C0 values programmed in the chip enable register.*

When the device select code is received, the device responds only if the b3, b2 and b1 values match the values of the C2, C1 and C0 bits programmed in the chip enable register.

If a match occurs, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time.

If the device does not acknowledge the device select code, the device de-selects itself from the bus, and goes into Standby mode (therefore will not acknowledge the device select code).

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

6 Instructions

6.1 Write operations on memory array

Following a start condition the bus master sends a device select code with the R/W bit (RW) reset to 0. The device acknowledges this, as shown in Figure 5, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 6. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 7. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a stop condition immediately after a data byte ACK bit (in the “10^{th} bit” time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

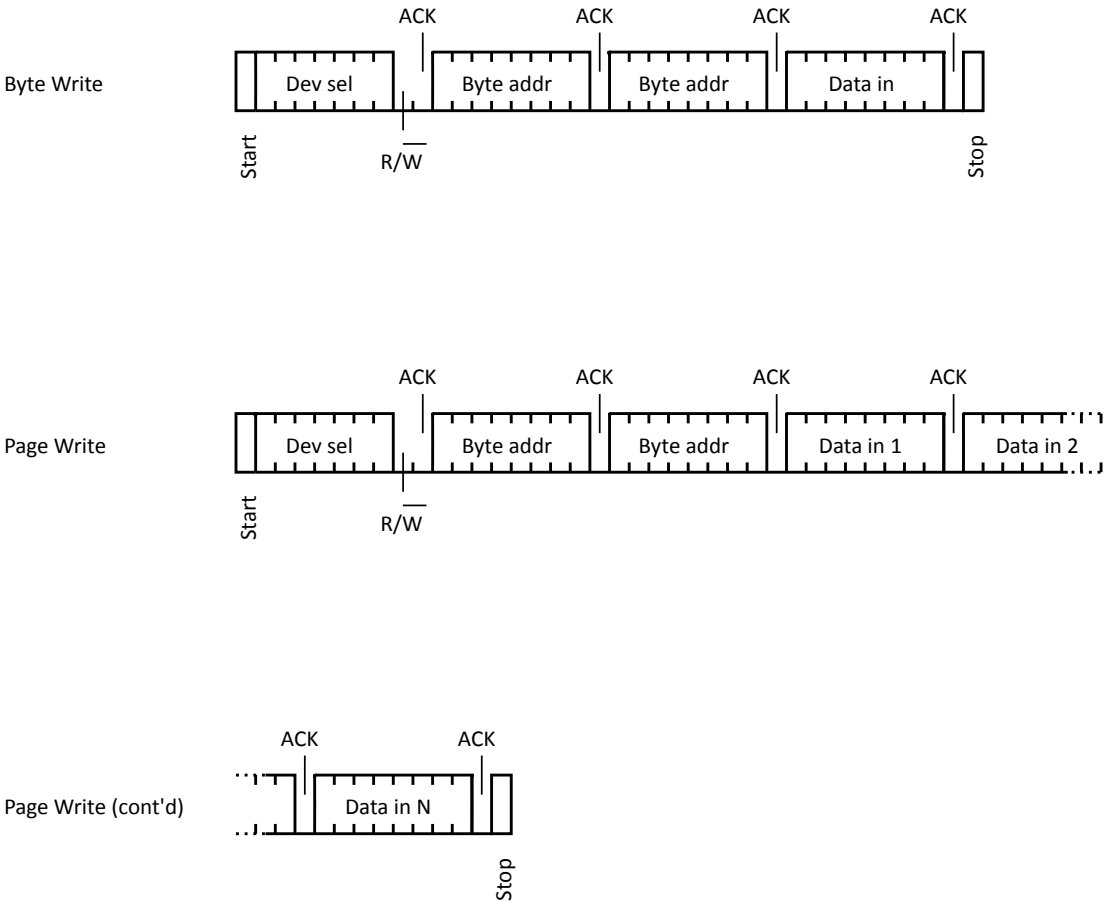
During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

If the software write protection is enabled with the SWP bit set to '1', the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 5.

6.1.1 Byte write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is write-protected, with the SWP bit set to '1', the device replies with NoACK, and the location is not modified, as shown in Figure 6 . If, instead, the addressed location is not Write-protected, the device replies with ACK. The bus master terminates the transfer by generating a stop condition, as shown in Figure 5.

Figure 5. Write mode sequence SWP bit = 0 (data write enabled)



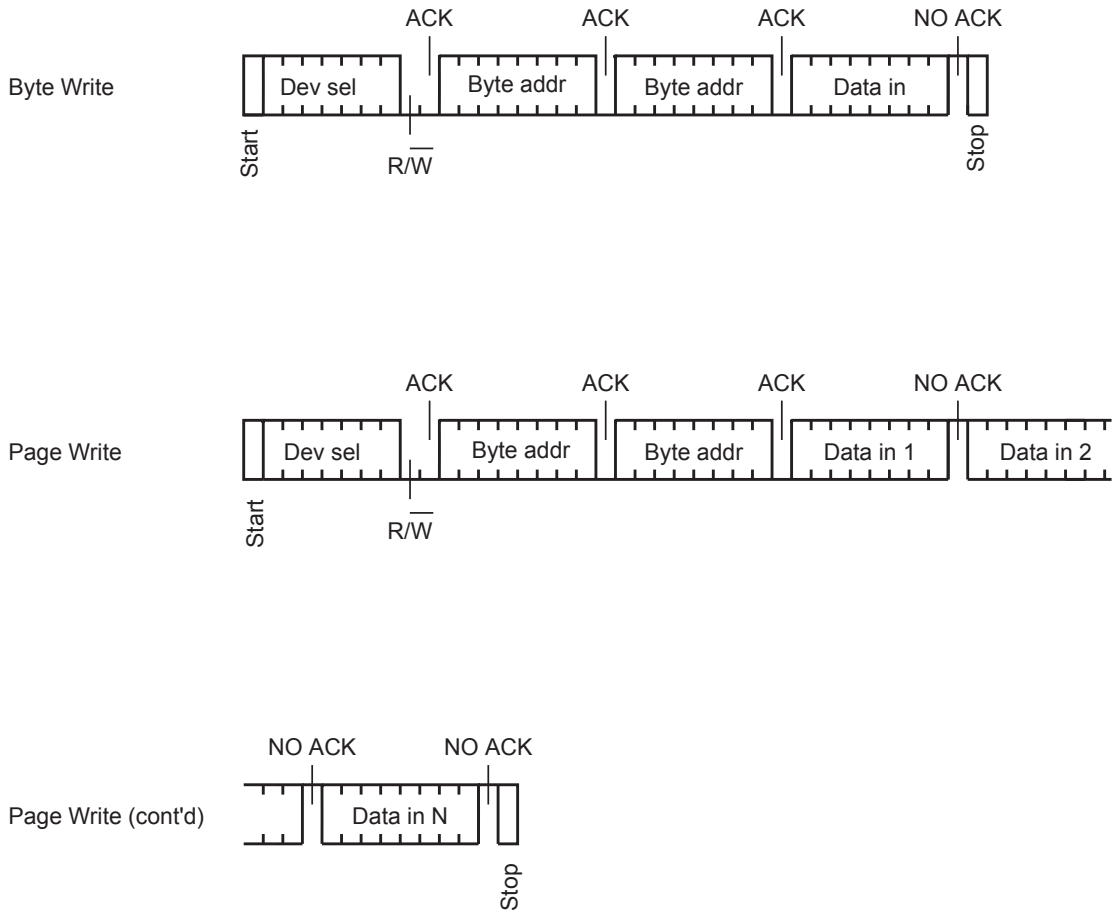
6.1.2 Page write

The page write mode allows up to 32 bytes to be written in a single write cycle, provided they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes than those that will fit up to the end of the page are sent, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each one is acknowledged by the device if the software write protection is disabled with the SWP bit set to '0'. If the software write protection is enabled with the SWP bit set to '1', the contents of the addressed memory location are not modified, and each data byte is followed by a NoACK, as shown in Figure 6. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a stop condition.

Figure 6. Write mode sequence with SWP bit = 1 (data write inhibited)



6.1.3 Minimizing write delays by polling on ACK

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in AC characteristics tables in Section 9 DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 7, is:

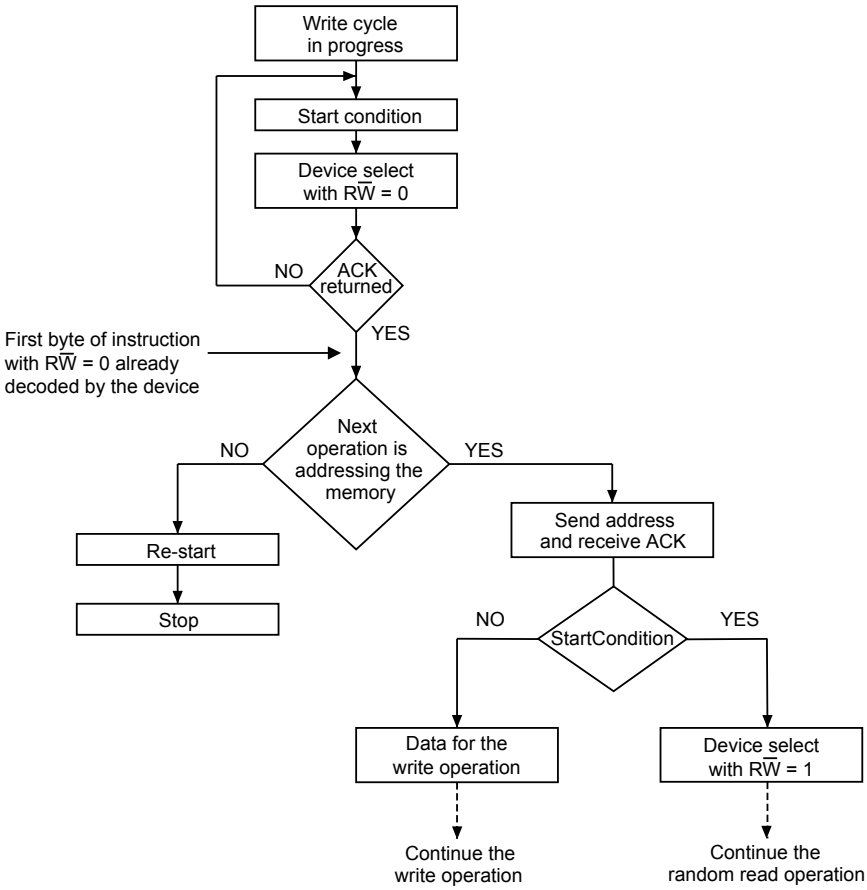
- Initial condition: a write cycle is in progress.
- Step 1: the bus master issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK will be returned and the bus master goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Note: In case of write to chip enable register when C2, C1 and C0 are re-configured, the device will return ACK only if:

- chip enable address of the device select code is equal to the new C2, C1 and C0 values

- an internal write cycle is completed (new C2, C1 and C0 values have been programmed in the chip enable register).

Figure 7. Write cycle polling flowchart using ACK



1. The seven most significant bits of the device select code of a random read (bottom right box in the figure) must be identical to the seven most significant bits of the device select code of the write (polling instruction in the figure).

6.2 Write operations on chip enable register

Write operations on chip enable register are performed independently of the state software write protect bit (SWP) .

Following a start condition the bus master sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this, as shown in Figure 8, and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

In order to write the chip enable register, address bytes must have A15 bit set to 1, all other bits A14 to A0 being don't care.

Table 8. Address of the chip enable register

A15 (1)	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	X (2)	X	X	X	X	X	X	X	X	X	X	X	X	X	X

1. *MSB A15 is sent first.*
2. *X means Don't Care bits.*

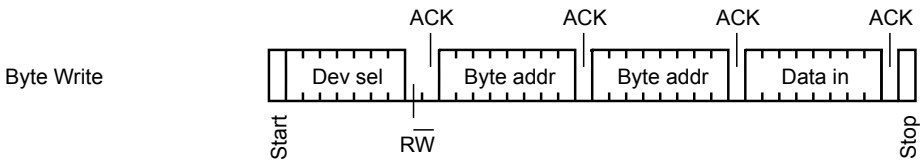
When the bus master generates a stop condition immediately after the data byte ACK bit (in the "10th bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (NoACK).

If the three bits C2, C1 and C0 have been re-configured with a correct write command, the device will acknowledge if the chip enable address of the device select code is equal to the new values of C2, C1 and C0, otherwise NoACK.

Sending more than one byte will abort the write cycle (chip enable register content will not be changed).

Figure 8. Write on chip enable register



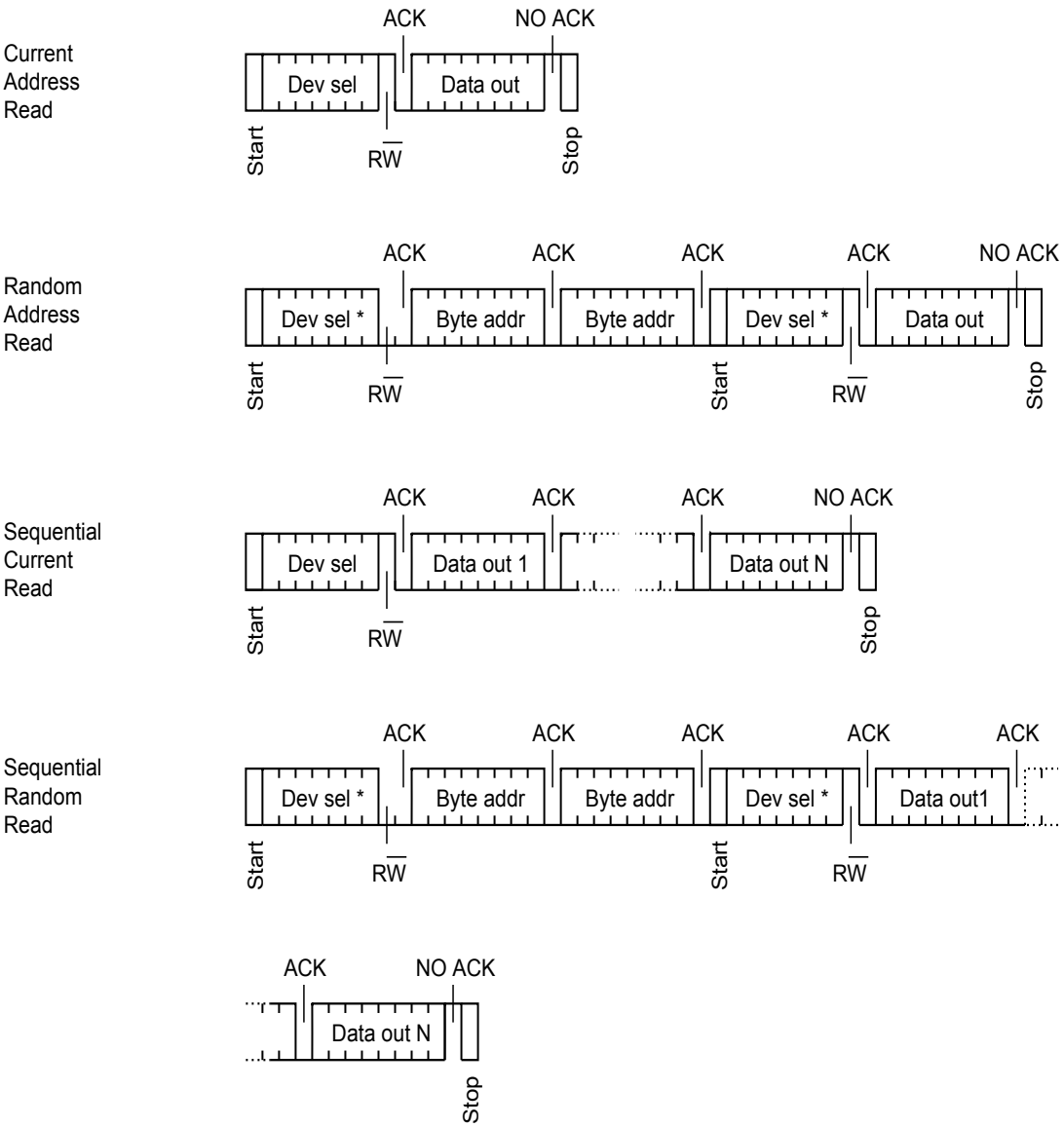
6.3 Read operations on memory array

Read operations are performed independently of the state of the software write protect bit (SWP).

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the read instructions, after each byte read (data out), the device waits for an acknowledgement (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 9. Read mode sequences



6.3.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 9) but without sending a stop condition. Then, the bus master sends another start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a stop condition.

6.3.2 Current address read

For the current address read operation, following a start condition, the bus master only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a stop condition, as shown in Figure 9, without acknowledging the byte.

When accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

6.3.3 Sequential read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 9. Read mode sequences.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

6.4 Read operations on chip enable register

Read operations are performed independently of the state software write protect bit (SWP).

Following a start condition the bus master sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge. Then, the bus master sends another start condition, and repeats the device select code with the RW bit set to 1. The device acknowledges this, and outputs the contents of the chip enable register.

To terminate the stream of data byte, the bus master must not acknowledge the byte, and must generate a stop condition, as shown in Figure 10.

After the successful completion of a read operation, the device internal address counter is not incremented by one, to point to the next byte address. Reading more than one byte will loop on reading the chip enable register value.

Reading the chip enable register is performed with a random read instruction at address 1xxx.xxxx.xxxx.xxxxb:

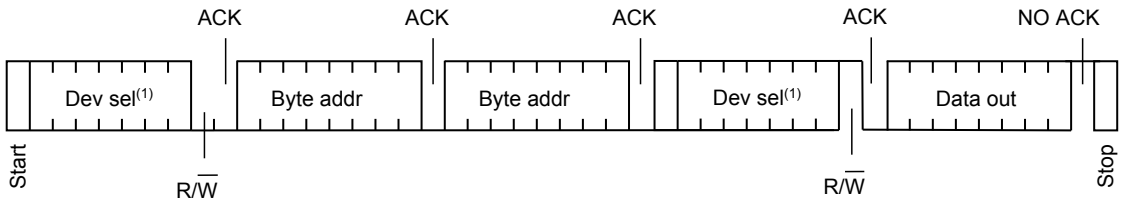
- Bits b7, b6, b5, b4 of the chip enable register content are read as 0, 0, 0, 0.
- The configurable device address bits b3, b2, b1 are described in Section 4.1 Chip enable register.
- The software write protection bit b0 is defined in Section 4.1 Chip enable register.

The chip enable register cannot be read while a write cycle (t_w) is ongoing.

The chip enable address value can be checked by sending the device select code.

- If the chip enable address b3, b2, b1 sent in the device select code is matching with the C2, C1 and C0 values, device will send an acknowledge.
- Otherwise, device will answer NoACK.

Figure 10. Read on chip enable register



1. The seven most significant bits of the device select code of a random read (in the first and fourth bytes) must be identical.

7 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

The chip enable register is delivery with following values:

- b7 to b5 set to '0'
- SWP sets to '0'
- C2, C1 and C0 set to '0' (unless specific chip enable address, in this case the value given in Table 4.

8 Maximum ratings

Stressing the device outside the ratings listed in Table 9 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (human body model)(2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to AECQ100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012, C1=100 pF, R1=1500 Ω).*

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 10. Operating conditions

Symbol	Parameter	Min.		Max.	Unit
V_{CC}	Supply voltage	1.6	1.7	5.5	V
T_A	Ambient operating temperature: Read	–40	-40	85	°C
	Ambient operating temperature: Write	0	-40		
f_C	Operating clock frequency V_{CC} = 1.6 V	-		400	kHz
	Operating clock frequency V_{CC} ≥ 1.7 V	-		1000	

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 11. AC measurement I/O waveform

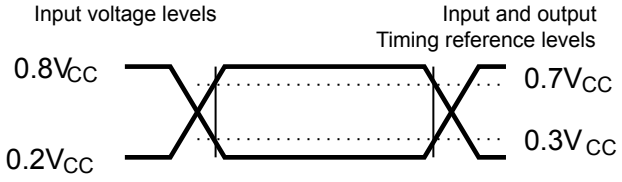


Table 12. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF

1. *Characterized only, not tested in production.*

Table 13. Cycling performance

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance (1)	T_A = 25 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	4,000,000	Write cycles (2)
		T_A = 85°C, V_{CC}(min) < V_{CC} < V_{CC}(max)	1.200.000	

1. *The Write cycle endurance is defined by characterization and qualification.*
2. *A Write cycle is executed when either a page write, or a byte write or a write chip enable register instruction is decoded.*

Table 14. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	T_A = 55 °C	200	Year
Cycling	T_A = 25 °C	4 million	Cycle

1. *The data retention behaviour is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.*

Table 15. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 10)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} < 1.8 V, f_C = 400 kHz	-	0.8	mA
		V_{CC} ≥ 1.8 V, f_C = 400 kHz	-	2	
		V_{CC} ≥ 1.8 V, f_C = 1 MHz	-	2.5	
I_{CC0}	Supply current (Write)(1)	During t_W	-	2	mA
I_{CC1}	Standby supply current	Device not selected, (2) V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8 V	-	1	µA
		Device not selected, (2) V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5 V	-	2	
		Device not selected, (2) V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5 V	-	3	
V_{IL}	Input low voltage (SCL, SDA)	-	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.75 V_{CC}	6.5	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} < 1.8 V	-	0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V	-	0.4	V
		I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. *Characterized value, not tested in production*
2. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*

Table 16. 400 kHz AC characteristics (fast mode);

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2} (1)	t_F	SDA (out) fall time	20 (2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50	ns

1. *Characterized only, not tested in production.*
2. *With C_L = 10 pF.*
3. *There is no min. or max. value for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in Figure 12.*

Table 17. 1 MHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	700	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	(1)	ns
t_{QL1QL2} (2)	t_F	SDA (out) fall time	20 (3)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	50	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	650	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (2)	-	Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. *There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.*
2. *Characterized only, not tested in production.*
3. *With CL = 10 pF.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in Figure 13.*

Figure 12. Maximum R_{bus} value vs. bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

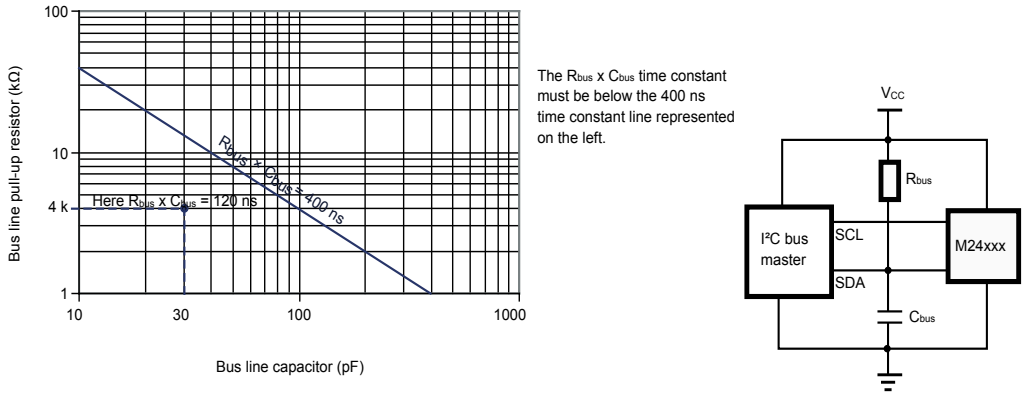


Figure 13. Maximum R_{bus} value vs. bus parasitic capacitance (C_{bus}) for an I^2C bus at f_C = 1MHz

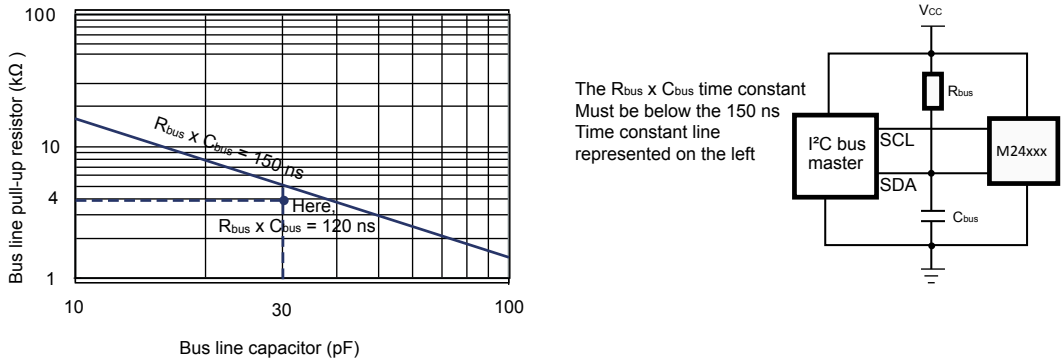
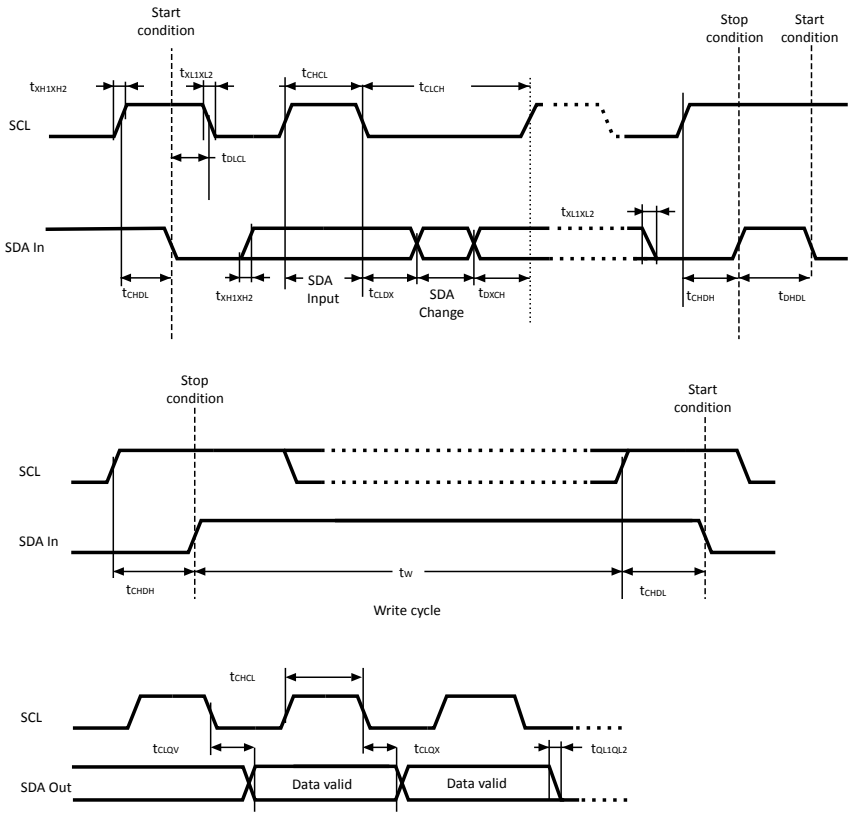


Figure 14. **AC waveforms**



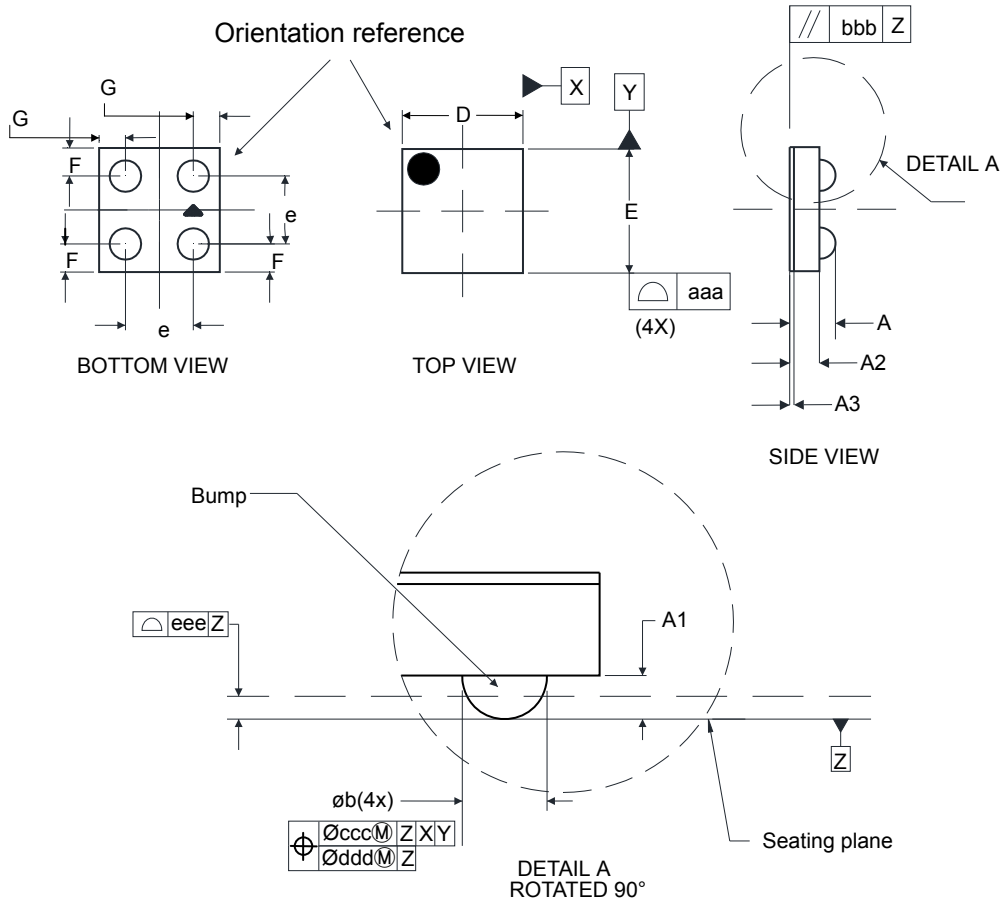
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 WLCSP4 (CP) package information

This WLCSP is a 4 balls, 0.711 x 0.731 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 15. WLCSP4 (CP) - Outline



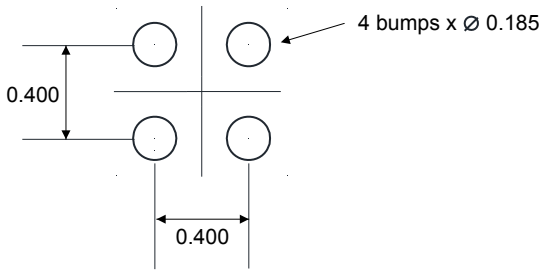
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 18. WLCSP4 (CP) - Mechanical data

Symbol	Milimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	0.200	0.225	0.250	0.0079	0.0091	0.0098
A1	-	0.025	-	-	0.0012	-
A2	-	0.175	-	-	0.0071	-
A3[3]	-	0.025	-	-	0.0012	-
b	-	0.185	-	-	0.0075	-
D	-	0.711	0.731	-	0.028	0.0287
E	-	0.731	0.751	-	0.0287	0.0290
e	-	0.400	-	-	0.0157	-
F	-	0.166	-	-	0.0065	-
G	-	0.156	-	-	0.0061	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The maximum total package height is calculated by the RSS method (root sum square) using nominal and tolerances values of A1 and A2*
3. *Backside coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability*

Figure 16. WLCSP4 (CP) - Recommended footprint

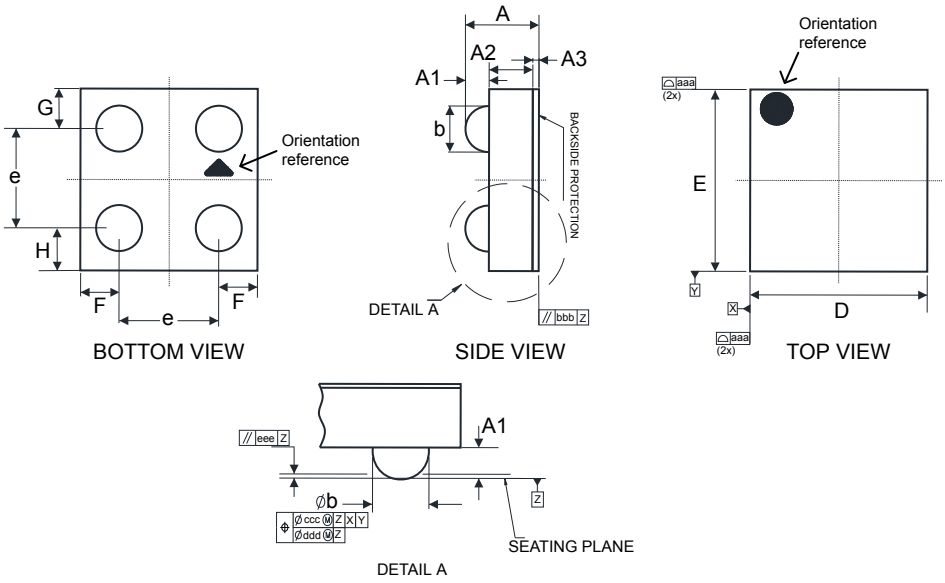


1. Dimensions are expressed in millimetres

10.2 WLCSP4 (CU) ultra thin package information

This WLCSP is a 4 bumps, 0.711 x 0.731 mm, ultra thin wafer level chip scale package.

Figure 17. WLCSP4 (CU) - Outline



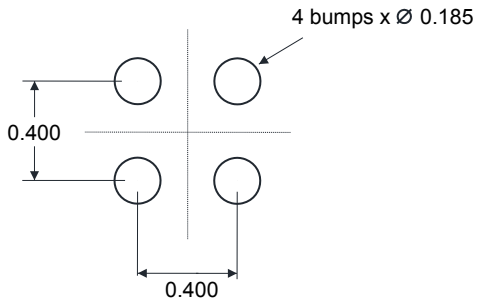
1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
3. Bump position designation per JESD 95-1, SPP-010.

Table 19. WLCSP4 (CU) - Mechanical data

Symbol	millimeters			inches [1]		
	Min	Typ	Max	Min	Typ	Max
A	0.262	0.295	0.328	0.0103	0.0116	0.0129
A1	-	0.095	-	-	0.0037	-
A2	-	0.175	-	-	0.0069	-
A3	-	0.025	-	-	0.0010	-
b[2] [3]	-	0.185	-	-	0.0073	-
D	-	0.711	0.731	-	0.0280	0.0288
E	-	0.731	0.751	-	0.0288	0.0296
e	-	0.400	-	-	0.0157	-
F	-	0.156	-	-	0.0061	-
G	-	0.161	-	-	0.0063	-
H	-	0.171	-	-	0.0067	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.060	-	-	0.0024	-
eee	-	0.060	-	-	0.0024	-

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Primary datum Z and seating plane are defined by the spherical crowns of the bump.*
3. *Dimension is measured at the maximum bump diameter parallel to primary datum Z.*

Figure 18. WLCSP4 (CU) - Recommended footprint



1. Dimensions are expressed in millimeters.

11 Ordering information

Table 20. Ordering information scheme

Example: M24 C64X F CU 6 T / T F

Device type

M24 = I^2C serial access EEPROM

Device function

C64X = 64 Kbit (8192 x 8 bit)

Operating voltage

F = V_{CC} = 1.6 V or 1.7 V to 5.5 V

Package (1)

CP = 4-bump WLCSP

CU = 4-bump WLCSP ultra-thin

Device grade

6 = Industrial: device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

blank = tube packing

Chip enable address(2)

/ = 000

A = 1 to 7 (value of chip enable address)

Process technology(3)

T =Process letter

Option

Blank = No back side coating

F = Back side coating

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*
2. *See Table 4*
3. *The process letter appears on the device package (marking) and on the shipment box. Contact your nearest ST Sales Office for further information.*

Note: Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 21. Document revision history

Date	Revision	Changes
05-Jan-2018	1	Initial release
21-May-2018	2	Updated "Section 1: Description, Figure 1: Logic diagram, Section 6.2: Write operations on chip enable register", title of "Table 14: DC characteristics", "Table 19: Ordering information scheme." Added note 5 in "Figure 15: WLCSP - 4 balls, 0.711x0.731 mm, 0.4 mm pitch, ultra ultra-thin wafer level chip scale grid array package outline", WLCSP4 (CU) package in cover page and "Section 10.3: WLCSP4 ultra thin package information."
21-Jun-2018	3	Updated title in "Table 18. WLCSP -4 balls, 0.711 x 0.731 mm, 0.4 mm pitch, wafer level chip scale mechanical data" and in "Figure 18. WLCSP -4 balls, 0.711 x 0.731 mm, 0.4 mm pitch, wafer level chip scale recommended footprint".
28-Aug-2018	4	Updated "Figure 2: 4-bump WLCSP connections (top view, marking side, with balls on the underside)", "Figure 10: Read on chip enable register" and "Figure 17: Ultra Thin WLCSP- 4-bump, 0.711 x 0.731 mm, wafer level chip scale package outline." Updated "Table 2: Signals vs. bump position."
05-Sep-2018	5	Updated Section 1 Description. Updated Figure 2. 4-bump WLCSP connections.
01-Apr-2019	6	Added device M24C64X-FCP. Removed device M24C64X-FCV, reference to CP package in cover page and in Table 20. Ordering information scheme. Updated Section 10.1 WLCSP4 (CP) package information.
20-Sep-2019	7	Updated Figure 3. Block diagram, Figure 10. Read on chip enable register,
19-Jan-2021	8	Updated: • Features, Section 1 Description, Section 6.3.2 Current address read, Section 7 Initial delivery state • Figure 3. Block diagram • note in Table 3. Chip enable register values • Table 20. Ordering information scheme added Table 4. Commercial product number versus chip enable address at factory delivery

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