





#### P-CHANNEL ENHANCEMENT MODE MOSFET

#### **Features**

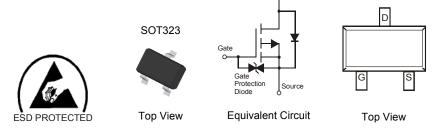
- Low On-Resistance
- Very Low Gate Threshold Voltage V<sub>GS(th)</sub> < 1V</li>
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

#### **Mechanical Data**

Case: SOT323

Drain

- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)



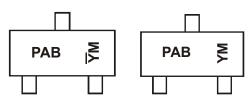
### Ordering Information (Note 4)

I		
Part Number	Case	Packaging
DMP2004WK-7	SOT323	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

# **Marking Information**



Chengdu A/T Site Shanghai A/T Site

PAB = Product Type Marking Code YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)  $\overline{Y}$ M = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or  $\overline{Y}$  = Year (ex: A = 2013) M = Month (ex: 9 = September)

#### Date Code Key

	Date Code Rey												
	Year	2007	2008	2009	2010	201	1 20	)12	2013	2014	2015	2016	2017
	Code	U	V	W	X	Y		Z	Α	В	С	D	Е
Ī	Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ſ	Code	1	2	3	4	5	6	7	8	9	0	N	D



# Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Drain Current (Note 5)	I <sub>D</sub>	-400	mA
Pulsed Drain Current	I <sub>DM</sub>	-1.4	А

# Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	$P_d$	250	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ hetaJA}$	500	°C/W
Operating and Storage Temperature Range	T <sub>j,</sub> T <sub>STG</sub>	-55 to +150	°C

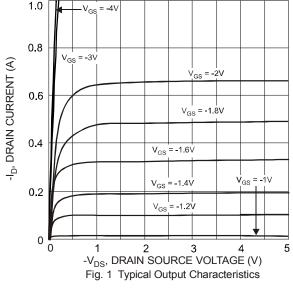
# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

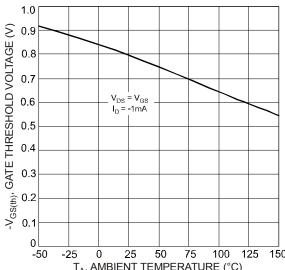
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 6)		•	•		•		
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	_	_	V	$V_{GS} = 0V$ , $I_D = -250\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	-1.0	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±1.0	μΑ	$V_{GS} = \pm 4.5V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 6)			•				
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.5	_	-1.0	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			0.7	0.9		$V_{GS} = -4.5V$ , $I_D = -430$ mA	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	1.1 1.7	1.4 2.0	Ω	$V_{GS} = -2.5V$ , $I_D = -300$ mA	
						$V_{GS} = -1.8V$ , $I_D = -150mA$	
Forward Transfer Admittance	Y <sub>fs</sub>	200	_	_	mS	V <sub>DS</sub> =10V, I <sub>D</sub> = -0.2A	
Diode Forward Voltage (Note 6)	V <sub>SD</sub>	-0.5	_	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -115mA	
DYNAMIC CHARACTERISTICS (Note 7)							
Input Capacitance	C <sub>iss</sub>	_	_	175	pF		
Output Capacitance	Coss	_		30	pF	$V_{DS} = -16V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	_	20	pF	1 - 1.0WII IZ	

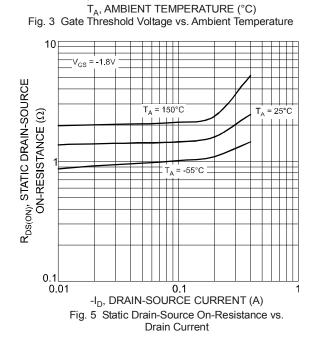
Notes:

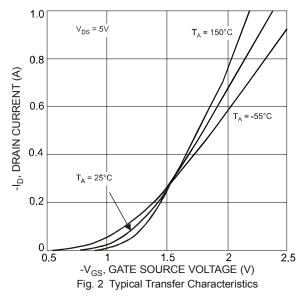
- 5. Device mounted on FR-4 PCB.
- 6. Short duration pulse test used to minimize self-heating effect.7. Guaranteed by design. Not subject to production testing.











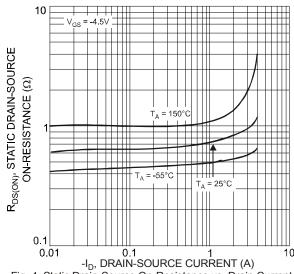


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

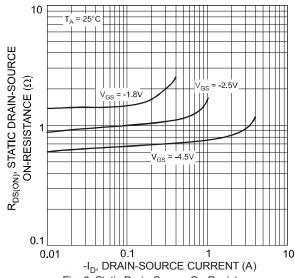


Fig. 6 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

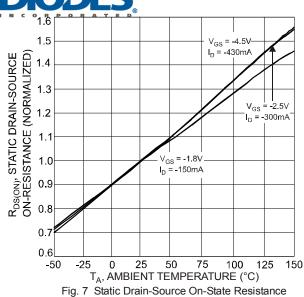


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

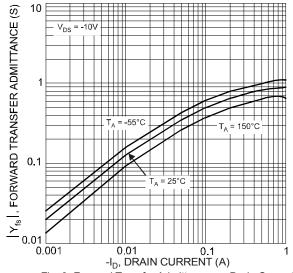


Fig. 9 Forward Transfer Admittance vs. Drain Current

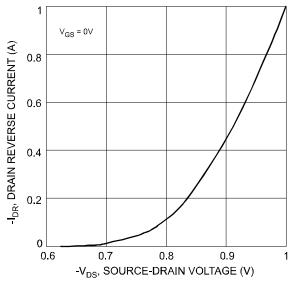
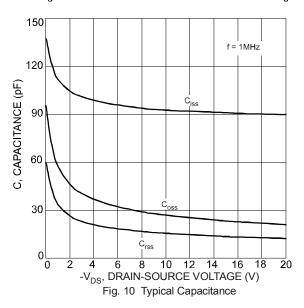
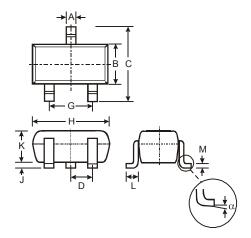


Fig. 8 Drain Reverse Current vs. Source-Drain Voltage



### **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

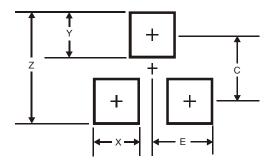


	SOT323							
Dim	Min	Max	Тур					
Α	0.25	0.40	0.30					
В	1.15	1.35	1.30					
С	2.00	2.20	2.10					
D	1	1	0.65					
G	1.20	1.40	1.30					
Н	1.80	2.20	2.15					
J	0.0	0.10	0.05					
K	0.90	1.00	0.95					
L	0.25	0.40	0.30					
М	0.10	0.18	0.11					
α	0°	8°	-					
All	All Dimensions in mm							



# **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.8
Х	0.7
Υ	0.9
С	1.9
E	1.0

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