

## GaAs MMIC SP8T SWITCH NON-REFLECTIVE DC TO 2.5 GHz

FEBRUARY 2001

v02.0101

### Features

- LOW INSERTION LOSS (2 GHz): 1.4dB
- SINGLE POSITIVE SUPPLY: Vdd= +5V
- INTEGRATED 3:8 TTL DECODER
- 24 LEAD QSOP PACKAGE



### General Description

The HMC253QS24 is a low-cost non-reflective SP8T switch in a 24-lead QSOP package featuring wideband operation from DC to 2.5 GHz, covering all cellular/PCS (450 to 2000 MHz), wideband CDMA (2000-2300 MHz), industrial, scientific, and medical (900 and 2400 MHz), and CATV/DBS (50 to 2150 MHz) bands. The switch offers a single positive bias and true TTL/CMOS compatibility. A 3:8 decoder is integrated on the switch requiring only 3 control lines and a positive bias to select each path. The HMC253QS24 SP8T will replace multiple configurations of SP4T and SPDT MMIC switches.

### Guaranteed Performance

*For TTL Control and Vdd = +5V in a 50 Ohm system, -40 to +85 deg C*

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz		1.1	1.5	dB
	DC - 2.0 GHz		1.3	1.7	dB
	DC - 2.5 GHz		1.8	2.4	dB
Isolation	DC - 1.0 GHz	32	36		dB
	DC - 2.0 GHz	26	30		dB
	DC - 2.5 GHz	24	28		dB
Return Loss "On State"	DC - 1.0 GHz	14	18		dB
	DC - 2.0 GHz	9	12		dB
	DC - 2.5 GHz	6	8		dB
Return Loss RF1-8 "Off State"	0.3 - 2.5 GHz	7	10		dB
	0.5 - 2.5 GHz	10	13		dB
Input Power for 1dB Compression	0.3 - 2.5 GHz	20	23		dBm
Input Third Order Intercept (Two-Tone Input Power = +7 dBm each tone)	0.3 - 2.5 GHz	40	43		dBm
Switching Characteristics	0.3 - 2.5 GHz				
tRISE, tFALL (10/90% RF)			30		ns
tON, tOFF (50% CTL to 10/90% RF)			100		ns

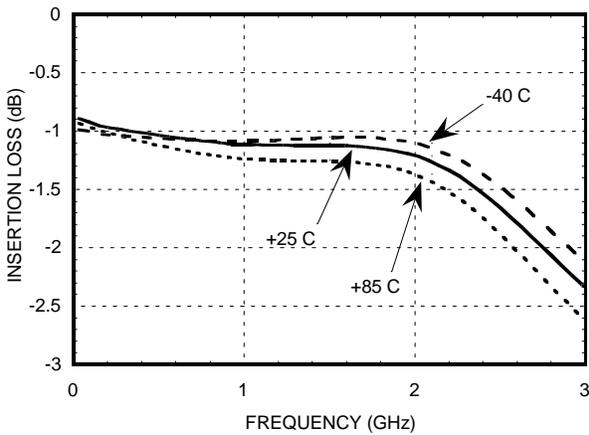


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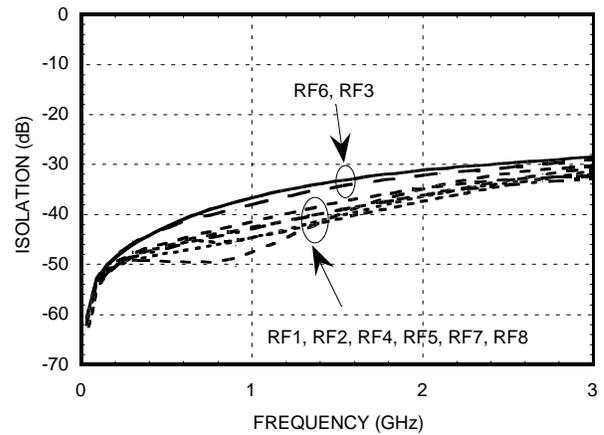
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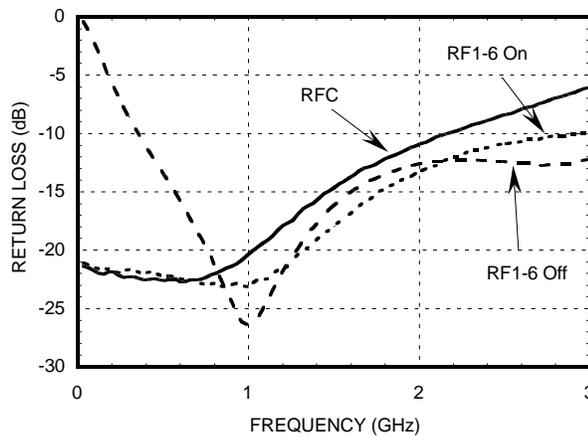
### Insertion Loss



### Isolation



### Return Loss

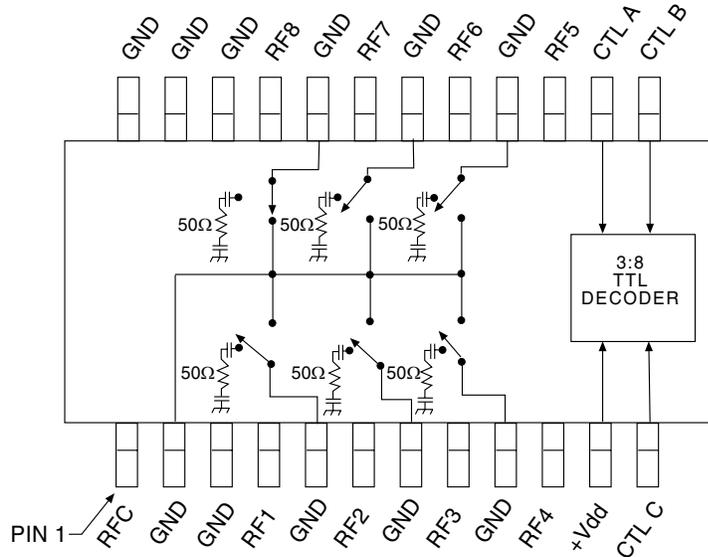


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### Functional Diagram



### Absolute Maximum Ratings

Bias Voltage Range (Port Vdd)	+7.0 Vdc
Control Voltage Range (A, B, C)	-0.5V to Vdd +1Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C
Maximum Input Power Vdd = +5V	+20dBm (0.05-0.5GHz) +24dBm (0.5-2.5GHz)

**NOTE:**

- 1) DC blocking capacitors are required at ports RFC and RF1, 2, 3, 4, 5, 6, 7, 8.

### Truth Table

Control Input			Signal Path State
A	B	C	RFCOM to:
Low	Low	Low	RF1
High	Low	Low	RF2
Low	High	Low	RF3
High	High	Low	RF4
Low	Low	High	RF5
High	Low	High	RF6
Low	High	High	RF7
High	High	High	RF8

### Bias Voltage & Current

Vdd Range = +5.0 Vdc ± 10%		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5.0	6.0	9.0

### TTL/CMOS Control Voltages

State	Bias Condition
Low	0 to +0.8 Vdc @ 5 uA Typ.
High	+2.0 to +5.0 Vdc @ 70 uA Typ..

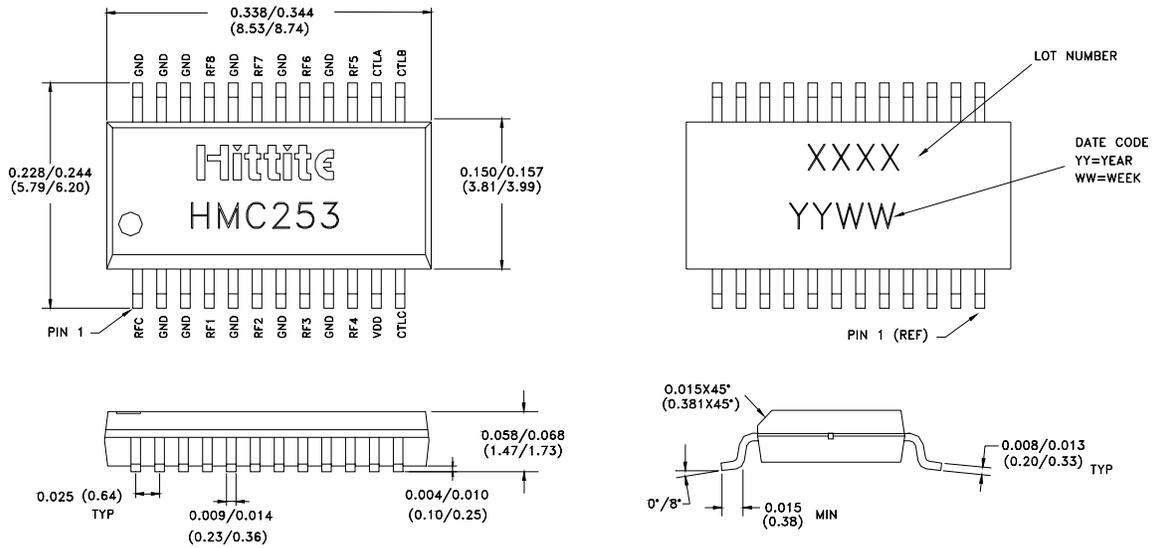


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### Outline Drawing



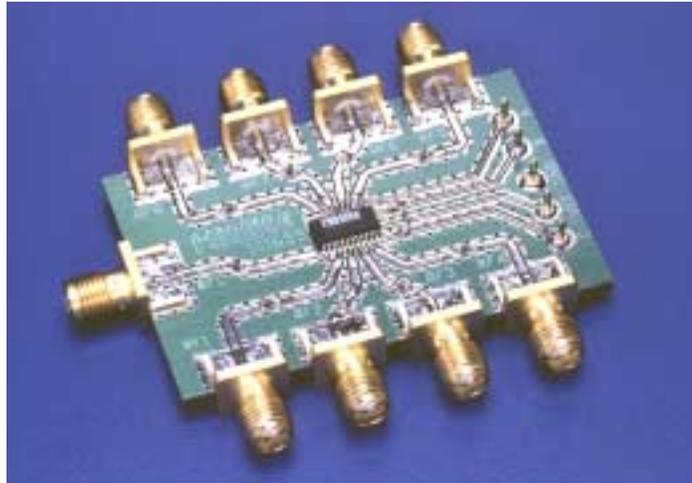
- 1) MATERIAL:
  - A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
  - B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TINSOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)

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### *Evaluation Circuit Board*

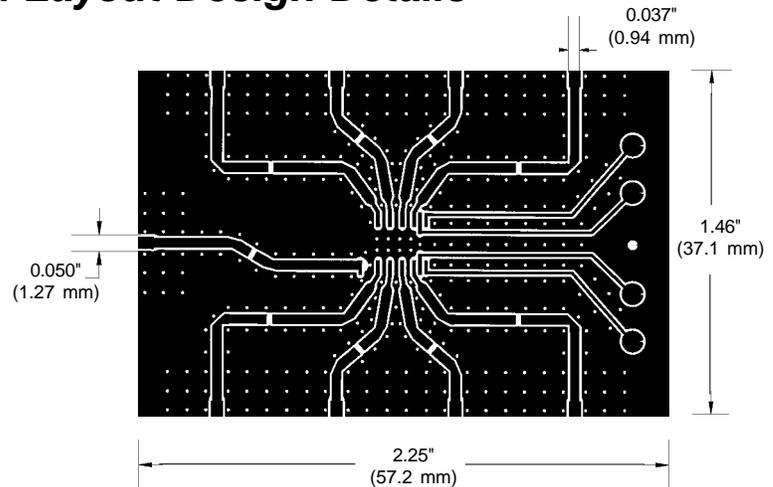


7  
SWITCHES  
SP8T  
SMT

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

### *Evaluation Circuit Board Layout Design Details*

Layout Technique	Grounded Coplanar Waveguide (CPWG)
Material	FR4
Dielectric Thickness	0.028" (0.71 mm)
50 Ohm Line Width	0.037" (0.94 mm)
Gap to Ground Edge	0.010" (0.25 mm)
Ground VIA Hole Diameter	0.014" (0.36 mm)
Connectors	SMA-F ( EF - Johnson P/N 142-0701-806)



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**NOTES:**