

MOSFET – Dual, P-Channel, ChipFET

-20 V, -4.1 A

NTHD4102P

Features

- Offers an Ultra Low $R_{DS(ON)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, and PDAs
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

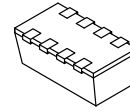
Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			-20	V
V _{GS}	Gate-to-Source Voltage			± 8.0	V
I _D	Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	-2.9	A
			T _A = 85°C	-2.1	
		t ≤ 10 s	T _A = 25°C	-4.1	
P _D	Power Dissipation (Note 1)	Steady State	T _A = 25°C	1.1	W
		t ≤ 10 s		2.1	
I _{DM}	Pulsed Drain Current	t _p = 10 μs		-16	A
T _J , T _{STG}	Operating Junction and Storage Temperature			-55 to 150	°C
I _S	Source Current (Body Diode)			-1.1	A
T _L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	°C

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Junction-to-Ambient, Steady State (Note 1)	113	$^\circ\text{C/W}$
	Junction-to-Ambient, $t \leq 10\text{ s}$ (Note 1)	60	

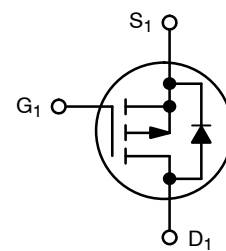
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)

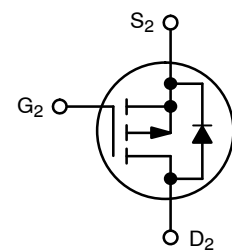


ChipFET
CASE 1206A
STYLE 2

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
-20 V	64 m Ω @ -4.5 V	-4.1 A
	85 m Ω @ -2.5 V	
	120 m Ω @ -1.8 V	

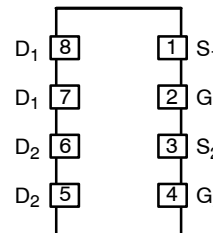


P-Channel MOSFET

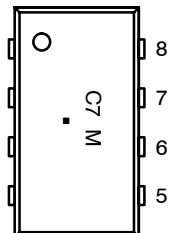


P-Channel MOSFET

PIN CONNECTIONS



MARKING DIAGRAM



C7 = Specific Device Code
M = Month Code
■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4102PT1	ChipFET	3,000 / Tape & Reel
NTHD4102PT1G	ChipFET (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://www.onsemi.com/BRD8011/D).

NTHD4102P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(Br)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{(Br)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			-15		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 85^\circ\text{C}$		-5.0	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.45		-1.5	V
$V_{GS(TH)}/T_J$	Gate Threshold Temperature Coefficient			2.7		mV/ $^\circ\text{C}$
$R_{DS(ON)}$	Drain-to-Source On Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2.9\text{ A}$		64	80	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$		85	110	
		$V_{DS} = -1.8\text{ V}, I_D = -1.0\text{ A}$		120	170	
g_{FS}	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -2.9\text{ A}$		7.0		S

CHARGES, CAPACITANCES, AND GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -16\text{ V}$		750		pF
C_{OSS}	Output Capacitance			100		
C_{RSS}	Reverse Transfer Capacitance			45		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = -4.5\text{ V}, V_{DS} = -16\text{ V},$ $I_D = -2.6\text{ A}$		7.6	8.6	nC
Q_{GS}	Gate-to-Source Charge			1.3		
Q_{GD}	Gate-to-Drain Charge			2.6		

SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = -4.5\text{ V}, V_{DD} = -16\text{ V},$ $I_D = -2.6\text{ A}, R_G = 2.0\text{ }\Omega$		5.5	10	ns
t_r	Rise Time			12	25	
$t_{d(OFF)}$	Turn-Off Delay Time			32	40	
t_f	Fall Time			23	35	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = -1.1\text{ A}$		-0.8	-1.2	V
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 1.0\text{ A}$		20	40	ns
t_a	Charge Time			15		
t_b	Discharge Time			5		
Q_{RR}	Reverse Recovery Charge			0.01		μC

- Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

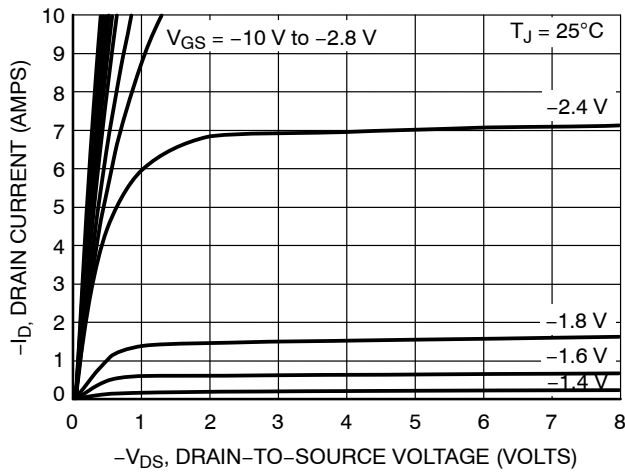


Figure 1. On-Region Characteristics

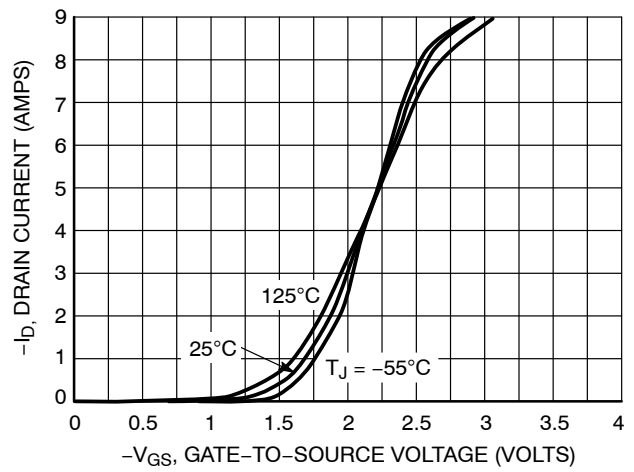


Figure 2. Transfer Characteristics

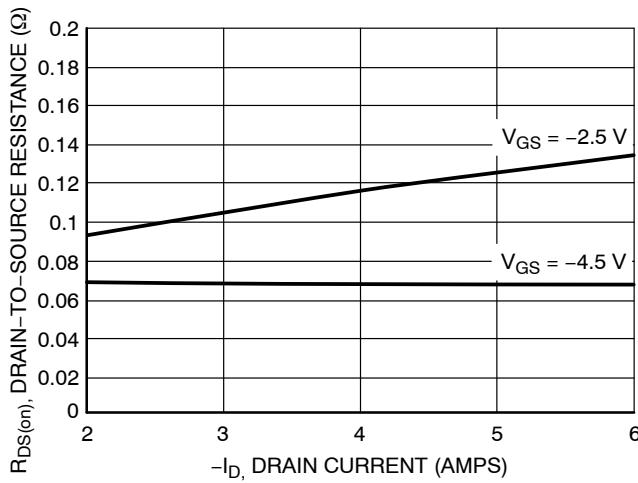


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

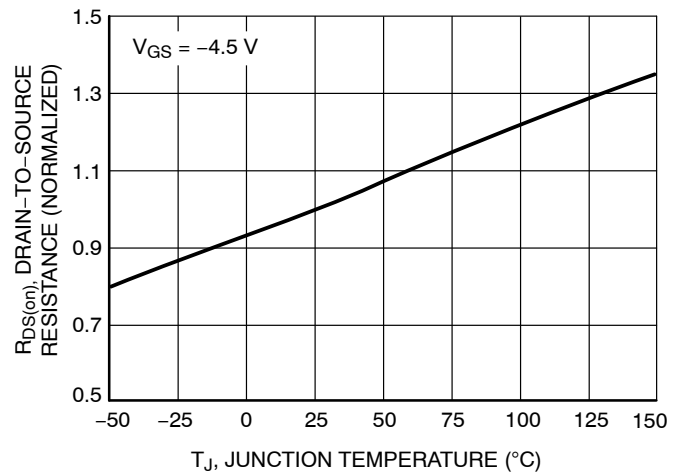


Figure 4. On-Resistance Variation with Temperature

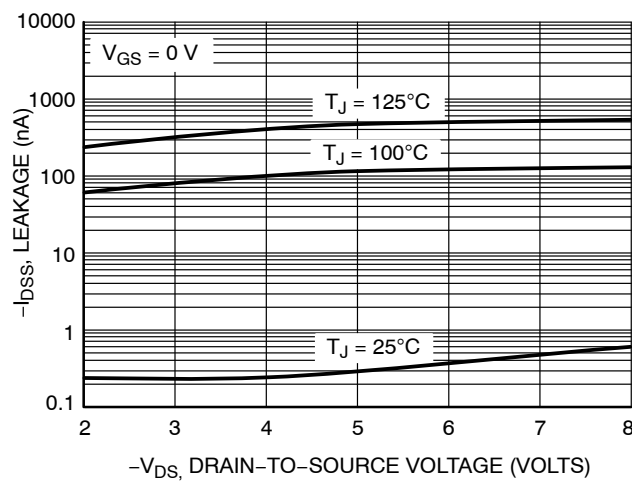


Figure 5. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

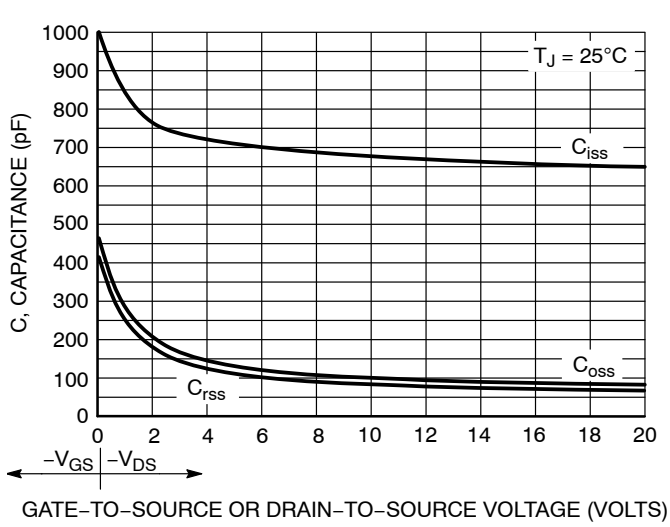


Figure 6. Capacitance Variation

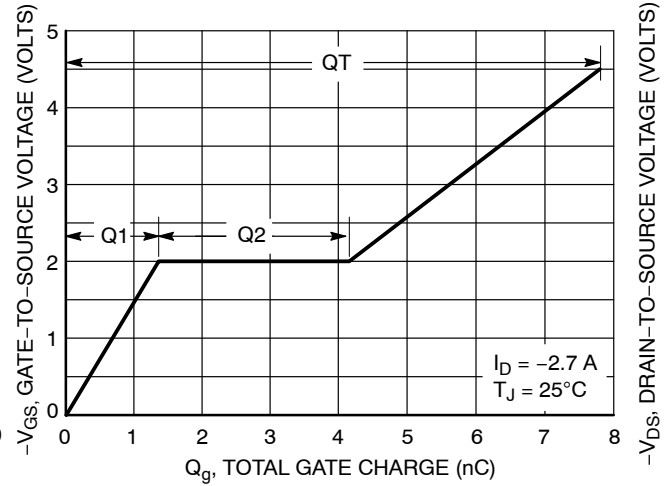


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

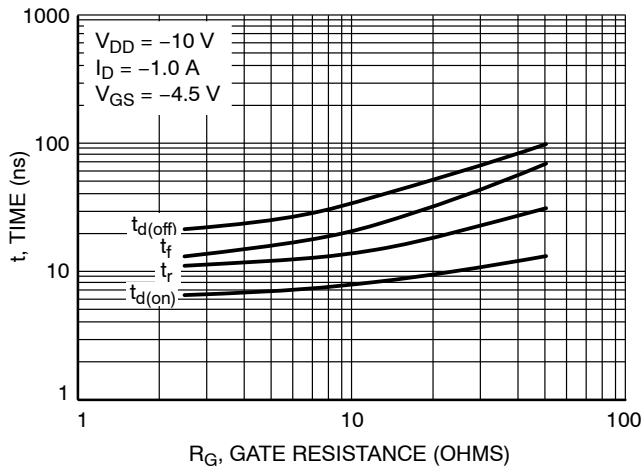


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

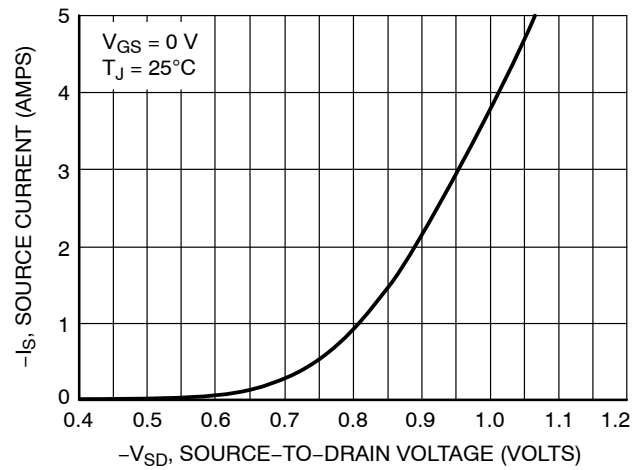


Figure 9. Diode Forward Voltage vs. Current

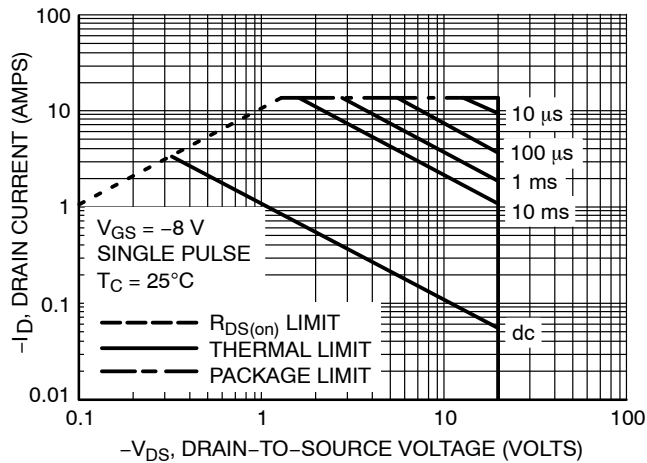
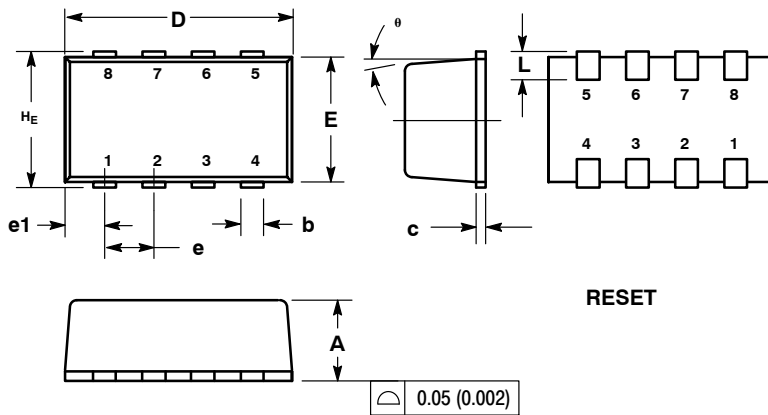


Figure 10. Maximum Rated Forward Biased Safe Operating Area



SCALE 1:1



ChipFET™
CASE1206A-03
ISSUE K

DATE 19 MAY 2009

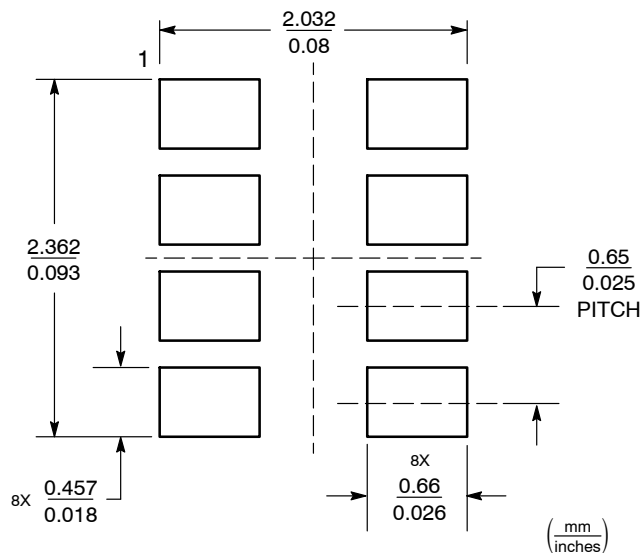
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

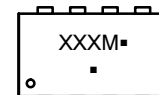
STYLE 1: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 2: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 3: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. COLLECTOR 4. BASE 5. EMITTER 6. COLLECTOR 7. COLLECTOR 8. COLLECTOR	STYLE 5: PIN 1. ANODE 2. ANODE 3. DRAIN 4. DRAIN 5. SOURCE 6. GATE 7. CATHODE 8. CATHODE	STYLE 6: PIN 1. ANODE 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. CATHODE / DRAIN
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SOLDERING FOOTPRINT



Basic Style

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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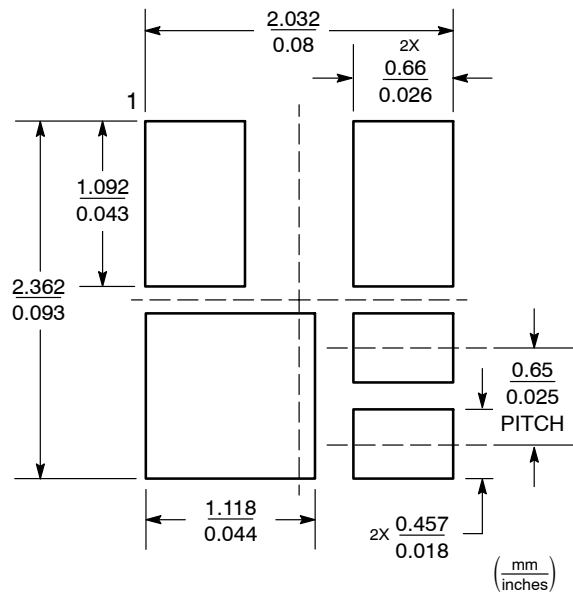
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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