
HN29W51214S Series

512M AND type Flash Memory
More than 16,057-sector (271,299,072-bit) \times 2

HITACHI

ADE-203-1155C (Z)

Rev. 3.0

Mar. 8, 2001

Description

The Hitachi HN29W51214S Series is stacked 2 chips Hitachi 256-Mbit Flash memory (HN29W25611S) that are CMOS Flash Memory with AND type memory cells. It has fully automatic programming and erase capabilities with a single 3.3 V power supply. The functions are compatible with HN29W25611S Series and controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (2048 + 64) bytes. Initial available sectors of HN29W51214S are more than 32,114 (98% of all sector address).

Features

- On-board single power supply (V_{CC}): $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
- Organization
 - AND Flash Memory: (2048 + 64) bytes \times (More than 16,057 sectors) \times 2
 - Data register: (2048 + 64) bytes \times 2
- Multi-level memory cell
 - 2 bit/per memory cell
- Automatic programming
 - Sector program time: 3.0 ms (typ)
 - System bus free
 - Address, data latch function
 - Internal automatic program verify function
 - Status data polling function
- Automatic erase
 - Single sector erase time: 1.5 ms (typ)
 - System bus free
 - Internal automatic erase verify function
 - Status data polling function

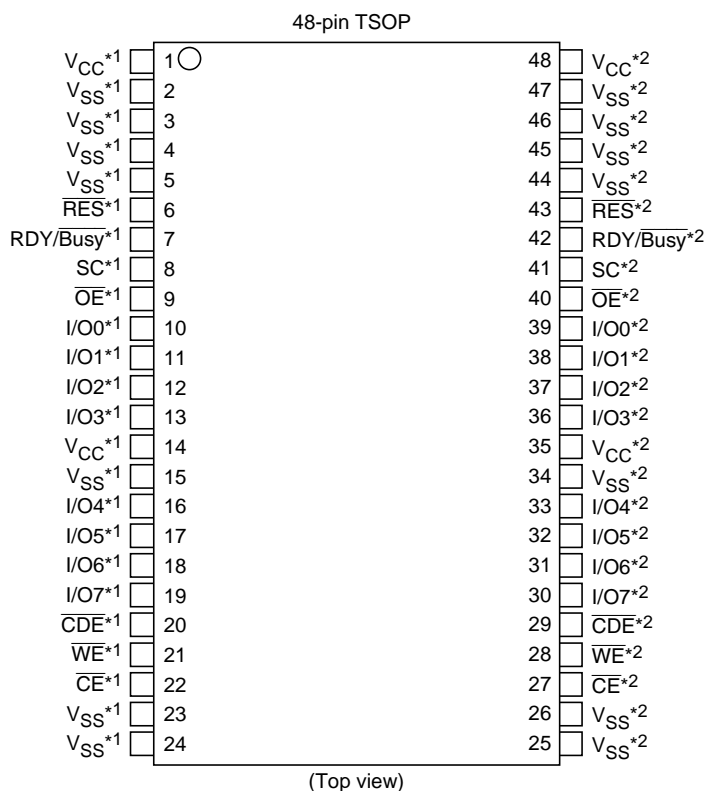
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- Erase mode
 - Single sector erase ((2048 + 64) byte unit)
- Fast serial read access time:
 - First access time: 50 μ s (max)
 - Serial access time : 80 ns (max) ($V_{CC} = 2.7$ V to 3.6 V)
: 60 ns (max) ($V_{CC} = 3.0$ V to 3.6 V)
- Low power dissipation:
 - $I_{CC2} = 50$ mA (max) (Read) (1-chip operation)
 $I_{CC2} = 100$ mA (max) (Read) (2-chip operation)
 - $I_{SB2} = 50$ μ A (max) (Standby) (1-chip operation)
 $I_{SB2} = 100$ μ A (max) (Standby) (2-chip operation)
 - $I_{CC3}/I_{CC4} = 40$ mA (max) (Erase/Program) (1-chip operation)
 $I_{CC3}/I_{CC4} = 80$ mA (max) (Erase/Program) (2-chip operation)
 - $I_{SB3} = 5$ μ A (max) (Deep standby) (1-chip operation)
 $I_{SB3} = 10$ μ A (max) (Deep standby) (2-chip operation)
- The following architecture is required for data reliability.
 - Error correction: more than 3-bit error correction per each sector read
 - Spare sectors: 1.8% (290 sectors)/chip within usable sectors

Ordering Information

Type No.	Available sector	Package
HN29W51214ST-80	More than 32,114 sectors	12.0 \times 18.40 mm ² 0.5 mm pitch 48-pin plastic TSOP I (TFP-48DA)

Pin Arrangement

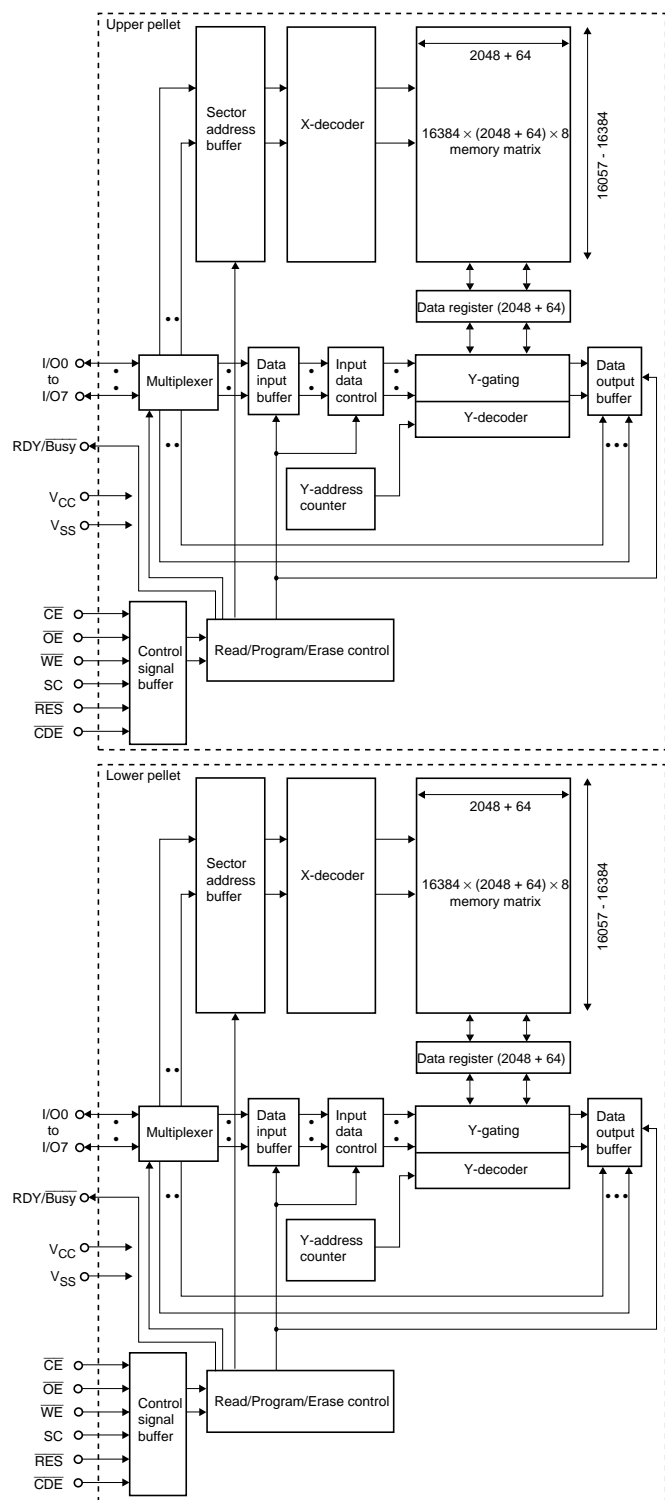


Notes: 1. Upper chip.
2. Lower chip.

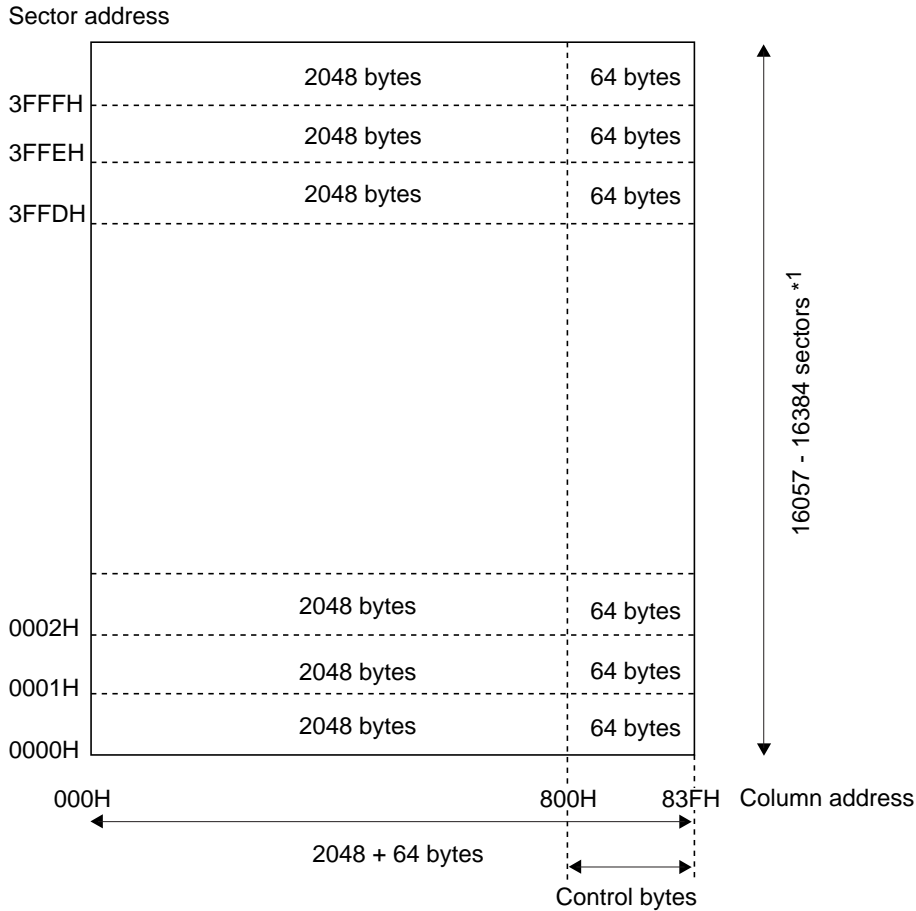
Pin Description

Pin name	Function
I/O0 to I/O7	Input/output
\overline{CE}	Chip enable
\overline{OE}	Output enable
\overline{WE}	Write enable
\overline{CDE}	Command data enable
V_{CC}	Power supply
V_{SS}	Ground
$\overline{RDY/Busy}$	Ready/ \overline{Busy}
\overline{RES}	Reset
SC	Serial clock

Block Diagram



Memory Map and Address



Address	Cycles	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Sector address	SA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	SA (2): Second cycle	A8	A9	A10	A11	A12	A13	×*2	×
Column address	CA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	CA (2): Second cycle	A8	A9	A10	A11	×	×	×	×

- Notes: 1. Some failed sectors may exist in the device. The failed sectors can be recognized by reading the sector valid data written in a part of the column address 800 to 83F (The specific address is TBD.). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.
2. An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH} , referred to DC characteristics.

Pin Function

$\overline{\text{CE}}$: $\overline{\text{CE}}$ is used to select the device. The status returns to the standby at the rising edge of $\overline{\text{CE}}$ in the reading operation. However, the status does not return to the standby at the rising edge of $\overline{\text{CE}}$ in the busy state in programming and erase operation.

$\overline{\text{OE}}$: Memory data and status register data can be read, when $\overline{\text{OE}}$ is V_{IL} .

$\overline{\text{WE}}$: Commands and address are latched at the rising edge of $\overline{\text{WE}}$.

SC: Programming and reading data is latched at the rising edge of SC.

$\overline{\text{RES}}$: $\overline{\text{RES}}$ pin must be kept at the V_{ILR} ($V_{\text{SS}} \pm 0.2 \text{ V}$) level when V_{CC} is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. $\overline{\text{RES}}$ must be kept at the V_{IHR} ($V_{\text{CC}} \pm 0.2 \text{ V}$) level during any operations such as programming, erase and read.

$\overline{\text{CDE}}$: Commands and data are latched when $\overline{\text{CDE}}$ is V_{IL} and address is latched when $\overline{\text{CDE}}$ is V_{IH} .

RDY/ $\overline{\text{Busy}}$: The RDY/ $\overline{\text{Busy}}$ indicates the program/erase status of the flash memory. The RDY/ $\overline{\text{Busy}}$ signal is initially at a high impedance state. It turns to a V_{OL} level after the (40H) command in programming operation or the (B0H) command in erase operation. After the erase or programming operation finishes, the RDY/ $\overline{\text{Busy}}$ signal turns back to the high impedance state.

I/O0 to I/O7: The I/O pins are used to input data, address and command, and are used to output memory data and status register data.

Mode Selection

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	SC	$\overline{\text{RES}}$	$\overline{\text{CDE}}$	RDY/ $\overline{\text{Busy}}$ * ³	I/O0 to I/O7
Deep standby	\times * ⁴	\times	\times	\times	V_{ILR}	\times	V_{OH}	High-Z
Standby	V_{IH}	\times	\times	\times	V_{IHR}	\times	V_{OH}	High-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	\times	V_{IHR}	\times	V_{OH}	High-Z
Status register read* ¹	V_{IL}	V_{IL}	V_{IH}	\times	V_{IHR}	\times	V_{OH}	Status register outputs
Command write* ²	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IHR}	V_{IL}	V_{OH}	Din

- Notes: 1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when $\overline{\text{CE}} = V_{\text{IL}}$ and $\overline{\text{OE}} = V_{\text{IL}}$ (conventional read operation condition).
2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.
3. The RDY/ $\overline{\text{Busy}}$ bus should be pulled up to V_{CC} to maintain the V_{OH} level while the RDY/ $\overline{\text{Busy}}$ pin outputs a high impedance.
4. An \times means "Don't care". The pin level can be set to either V_{IL} or V_{IH} referred to DC characteristics.

Command Definition*1, 2

Command		Bus cycles	First bus cycle		Second bus cycle		
			Operation mode*3	Data in	Operation mode	Data in	Data out
Read	Serial read (1)	(Without CA)	3	Write	00H	Write	SA (1)*4
		(With CA)	3 + 2h*6	Write	00H	Write	SA (1)*4
	Serial read (2)		3	Write	F0H	Write	SA (1)*4
	Read identifier codes		1	Write	90H	Read	ID*8, 9
	Data recovery read		1	Write	01H	Read	Recovery data
Auto erase	Single sector		4	Write	20H	Write	SA (1)*4
Auto program	Program (1)	(Without CA*7)	4	Write	10H	Write	SA (1)*4
		(With CA*7)	4 + 2h*6	Write	10H	Write	SA (1)*4
	Program (2)*10		4	Write	1FH	Write	SA (1)*4
	Program (3) (Control bytes)*7		4	Write	0FH	Write	SA (1)*4
	Program (4)	(Without CA*7)	4	Write	11H	Write	SA (1)*4
		(With CA*7)	4 + 2h*6	Write	11H	Write	SA (1)*4
Reset			1	Write	FFH		
Clear status register		1	Write	50H			

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Command			Bus cycles	Third bus cycle		Fourth bus cycle	
				Operation mode	Data in	Operation mode	Data in
Read	Serial read (1) (Without CA)	3	Write	SA (2) ^{**4}			
	(With CA)	3 + 2h ^{*6}	Write	SA (2) ^{**4}	Write	CA (1) ^{*5}	
	Serial read (2)	3	Write	SA (2) ^{**4}			
	Read identifier codes	1					
	Data recovery read	1					
Auto erase	Single sector	4	Write	SA (2) ^{**4}	Write	B0H ^{*11}	
Auto program	Program (1) (Without CA ^{*7})	4	Write	SA (2) ^{**4}	Write	40H ^{*11, 12}	
	(With CA ^{*7})	4 + 2h ^{*6}	Write	SA (2) ^{**4}	Write	CA (1)	
	Program (2) ^{*10}	4	Write	SA (2) ^{**4}	Write	40H ^{*11, 12}	
	Program (3) (Control bytes) ^{*7}	4	Write	SA (2) ^{**4}	Write	40H ^{*11, 12}	
	Program (4) (WithoutCA ^{*7})	4	Write	SA (2) ^{**4}	Write	40H ^{*11, 12}	
	(With CA ^{*7})	4 + 2h ^{*6}	Write	SA (2) ^{**4}	Write	CA (1)	
Reset		1					
Clear status register		1					

Command		Bus cycles	Fifth bus cycle		Sixth bus cycle	
			Operation mode	Data in	Operation mode	Data in
Read	Serial read (1) (Without CA)	3				
	(With CA)	3 + 2h* ⁶	Write	CA (2)* ⁵		
	Serial read (2)	3				
	Read identifier codes	1				
	Data recovery read	1				
Auto erase	Single sector	4				
Auto program	Program (1) (Without CA* ⁷)	4				
	(With CA* ⁷)	4 + 2h* ⁶	Write	CA (2)* ⁵	Write	40H* ^{11, 12}
	Program (2)* ¹⁰	4				
	Program (3) (Control bytes)* ⁷	4				
	Program (4) (Without CA* ⁷)	4				
	(With CA* ⁷)	4 + 2h* ⁶	Write	CA (2)	Write	40H* ^{11, 12}
Reset		1				
Clear status register		1				

- Notes: 1. Commands and sector address are latched at rising edge of \overline{WE} pulses. Program data is latched at rising edge of SC pulses.
2. The chip is in the read status register mode when \overline{RES} is set to V_{IHR} first time after the power up.
3. Refer to the command read and write mode in mode selection.
4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A13).
5. CA (1) = Column address (A0 to A7), CA (2) = Column address (A8 to A11).
(0 A11 to A0 83FH)
6. The variable h is the input number of times of set of CA (1) and CA (2) (1 h 2048 + 64).
Set of CA (1) and CA (2) can be input without limitation.
7. By using program (1) and (3), data can additionally be programmed for each sector before erase.
8. ID = Identifier code; Manufacturer code (07H), Device code (99H).
9. The manufacturer identifier code is output when \overline{CDE} is low and the device identifier code is output when \overline{CDE} is high.
10. Before program (2) operations, data in the programmed sector must be erased.
11. No commands can be written during auto program and erase (when the RDY/Busy pin outputs a V_{OL}).
12. The fourth or sixth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

Serial Read (1): Memory data D0 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 2112. When CA is input, memory data D (m) to D (m + j) in the sector of address SA is sequentially read. Then output data is not valid after the number of the SC pulse exceeds (2112 to m). The mode turns back to the standby mode at any time when \overline{CE} is V_{IH} .

Serial Read (2): Memory data D2048 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 64. The mode turns back to the standby mode at any time when \overline{CE} is V_{IH} .

Automatic Erase

Single Sector Erase: Memory data D0 to D2111 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the RDY/\overline{Busy} signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D2048 to D2111 must be read and kept outside of the sector before the sector erase.

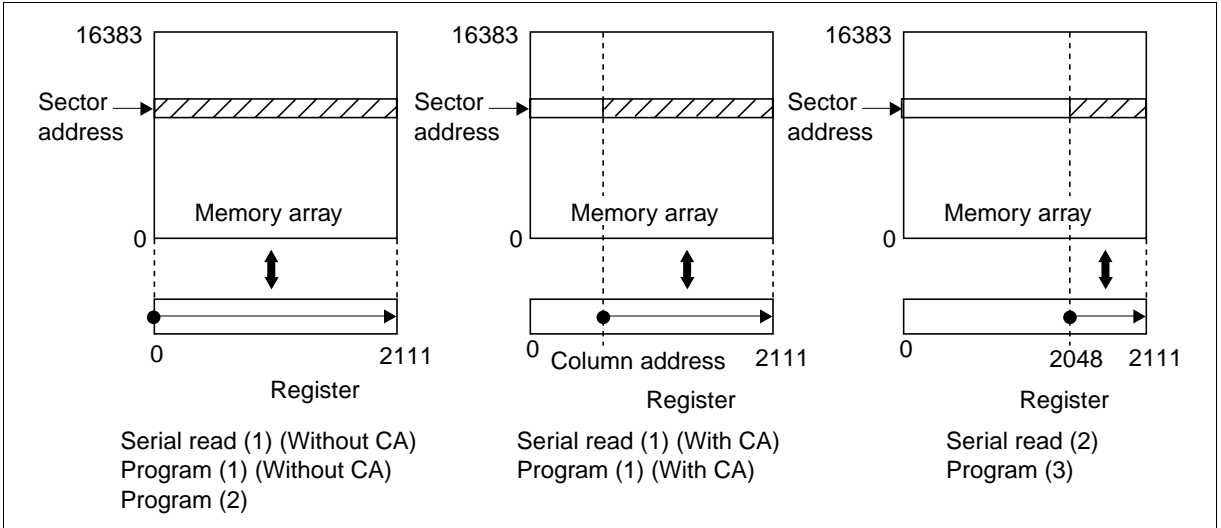
Automatic Program

Program (1): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD2048 to PD2111.

Program (2): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD2048 to PD2111.

Program (3): Program data PD2048 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.

Program (4): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (4), data can be rewritten for each sector before the following erase. So the column data before programming operation are either "1" or "0". In this mode, E/W number of times must be counted whenever program (4) execute. After the programming starts, the program completion can be checked through the RDY/Busy signal and status data polling. The sector valid data should be included in the program data PD2048 to PD2111.



Status Register Read

The status returns to the status register read mode from standby mode, when $\overline{\text{CE}}$ and $\overline{\text{OE}}$ is V_{IL} . In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description.

Identifier Read

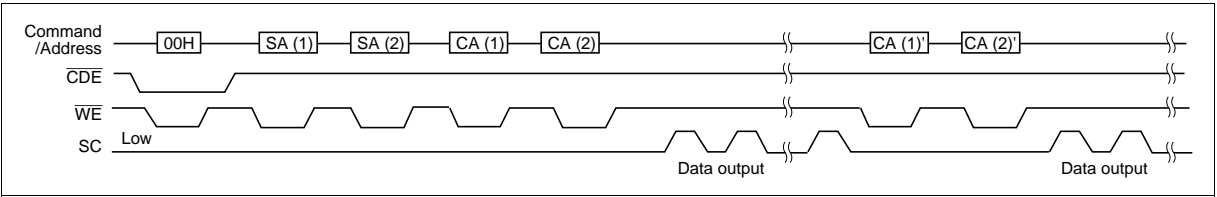
The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{\text{CDE}} V_{\text{IL}}$ and V_{IH} , respectively.

Data Recovery Read

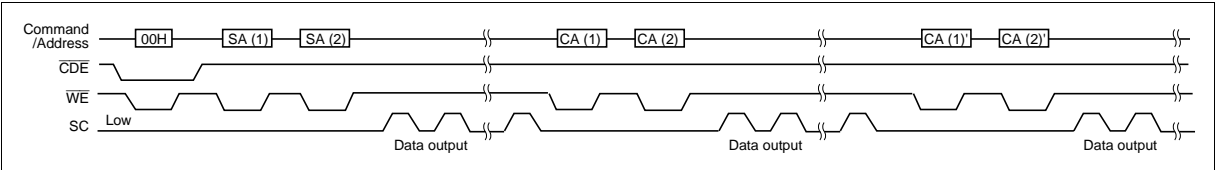
When the programming was an error, the program data can be read by using data recovery read. When an additional programming was an error, the data compounded of the program data and the origin data in the sector address SA can be read. Output data are not valid after the number of SA pulse exceeds 2112. The mode turns back to the standby mode at any time when $\overline{\text{CE}}$ is V_{IH} . The read data are invalid when addresses are latched at a rising edge of $\overline{\text{WE}}$ pulse after the data recovery read command is written.

Command/Address/Data Input Sequence

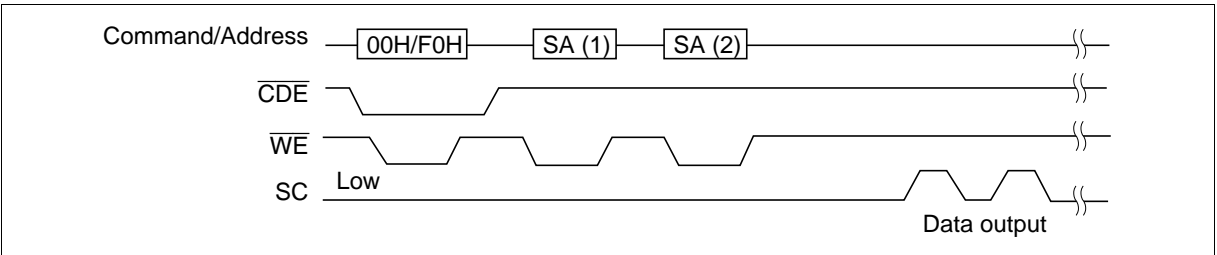
Serial Read (1) (With CA before SC)



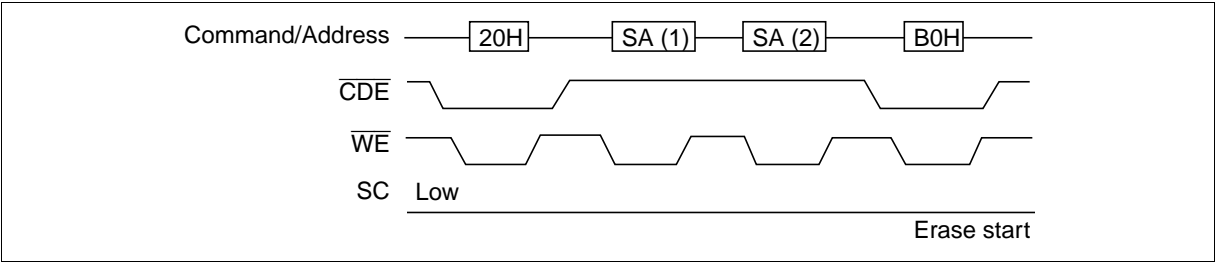
Serial Read (1) (With CA after SC)



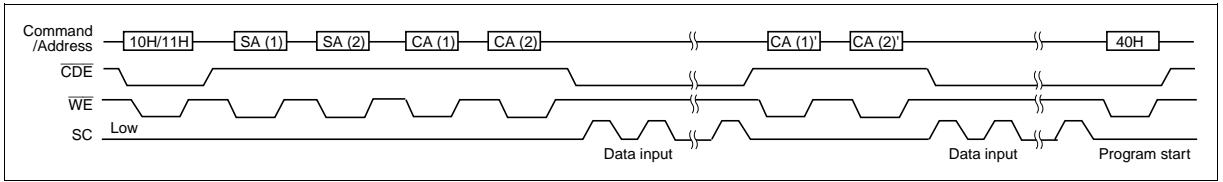
Serial Read (1) (Without CA), (2)



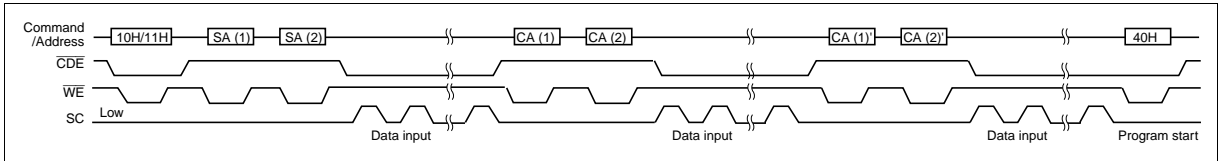
Single Sector Erase



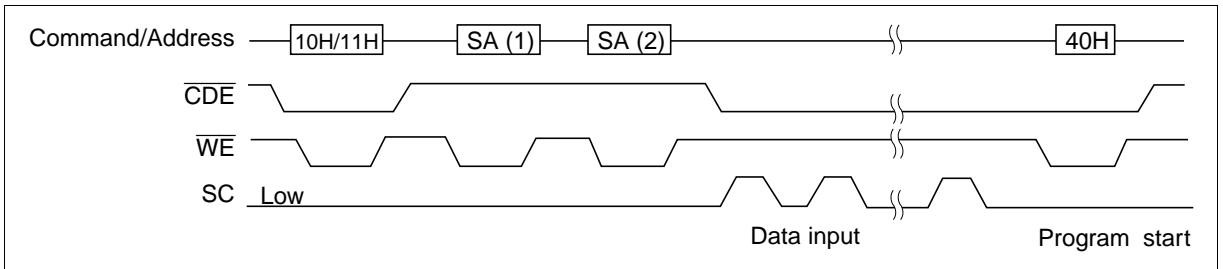
Program (1), (4) (With CA before SC)



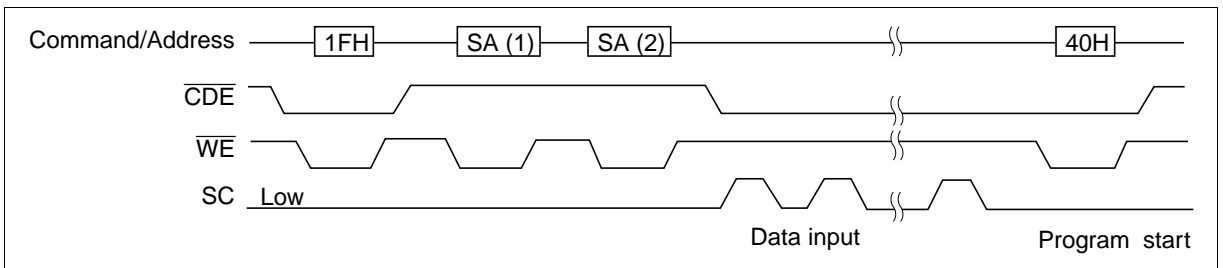
Program (1), (4) (With CA after SC)



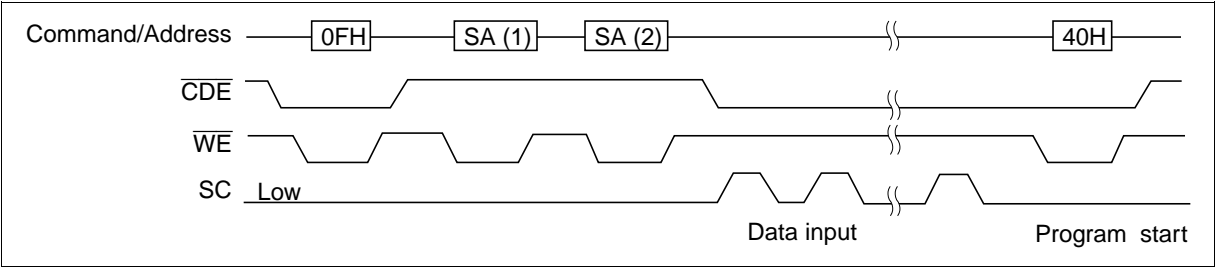
Program (1), (4) (Without CA)



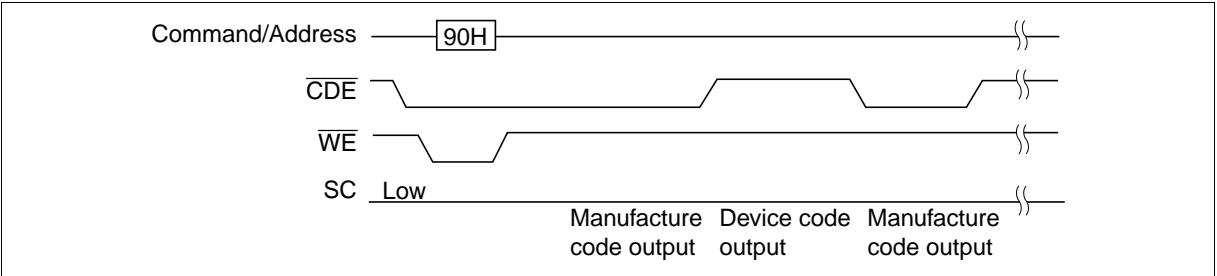
Program (2)



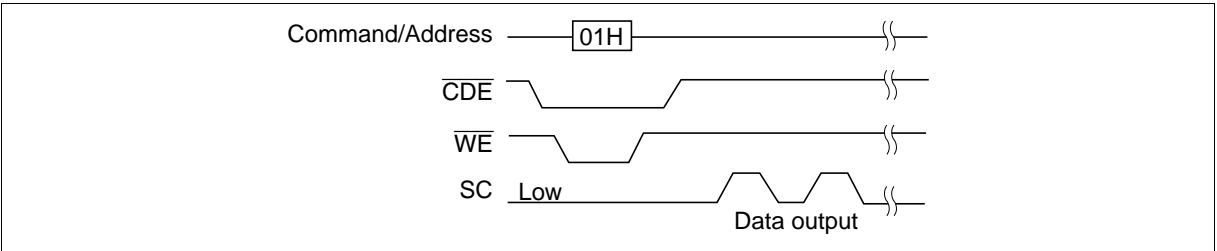
Program (3)



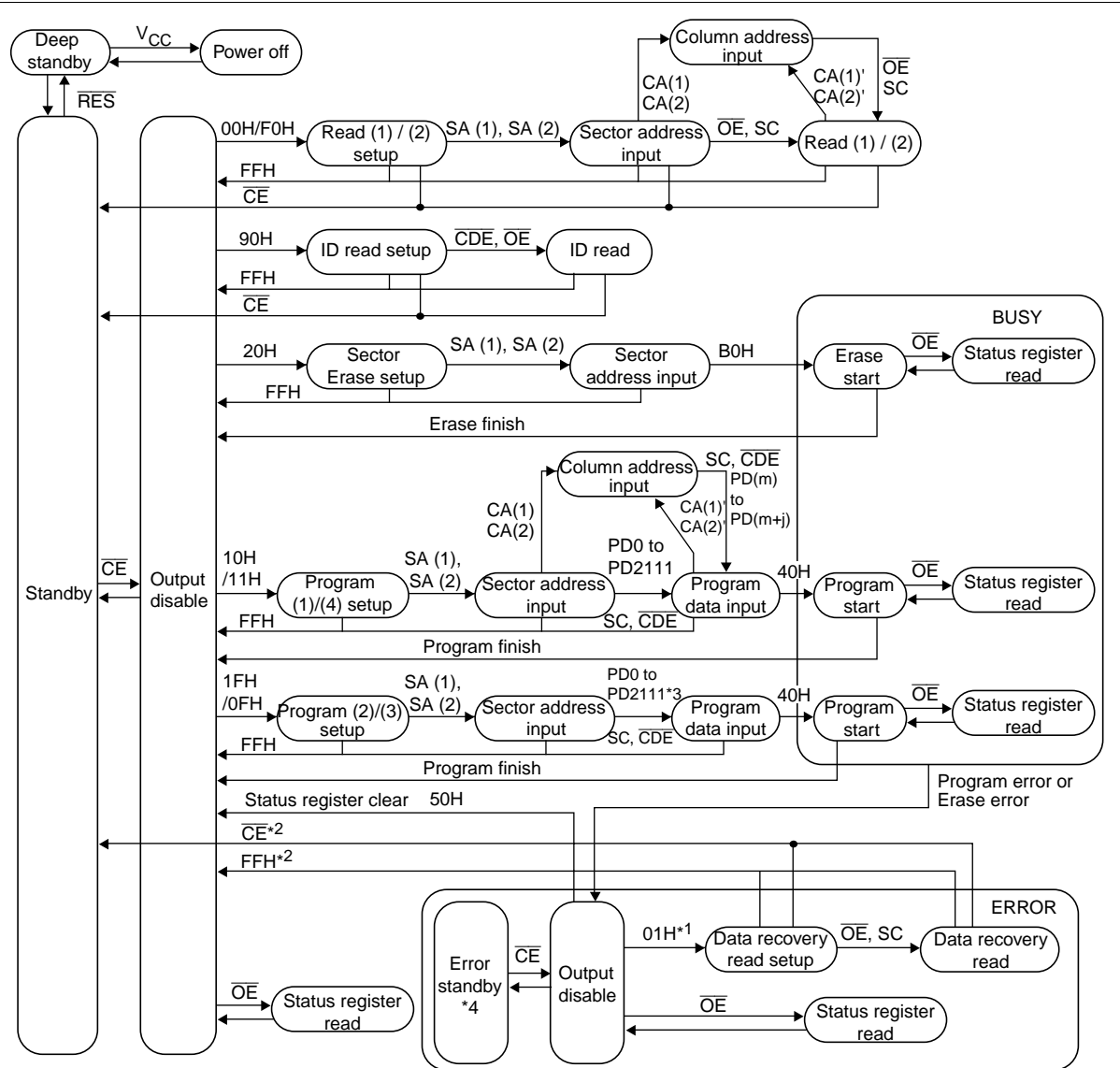
ID Read Mode



Data Recovery Read Mode



Status Transition



- Notes:
1. (01H) Data recovery read can be used only for Program (1), (2), (3), (4) errors.
 2. When reset is done by \overline{CE} or FFH, error status flag is cleared.
 3. When Program (3) mode, input data is PD2048 to PD2111.
 4. When Error standby, I_{CC3} level is current.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V _{CC} voltage	V _{CC}	−0.6 to +4.5	V	1
V _{SS} voltage	V _{SS}	0	V	
All input and output voltages	V _{in} , V _{out}	−0.6 to V _{CC} + 0.3	V	1, 2
Operating temperature range	T _{opr}	0 to +70	°C	
Storage temperature range	T _{stg}	−65 to +125	°C	3
Storage temperature under bias	T _{bias}	−10 to +80	°C	

Notes: 1. Relative to V_{SS}.
2. V_{in}, V_{out} = −2.0 V for pulse width 20 ns.
3. Device storage temperature range before programming.

Capacitance (T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C _{in}	—	—	6	pF	V _{in} = 0 V
Output capacitance	C _{out}	—	—	12	pF	V _{out} = 0 V

DC Characteristics ($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	I_{LO}	—	—	2	μA	$V_{out} = V_{SS} \text{ to } V_{CC}$
Standby V_{CC} current (1-chip operation)	I_{SB1}	—	0.3	1	mA	$\overline{CE} = V_{IH}$
(2-chip operation)	I_{SB1}	—	0.6	2	mA	
(1-chip operation)	I_{SB2}	—	30	50	μA	$\overline{CE} = V_{CC} \pm 0.2 \text{ V}$, $\overline{RES} = V_{CC} \pm 0.2 \text{ V}$
(2-chip operation)	I_{SB2}	—	60	100	μA	
Deep standby V_{CC} current (1-chip operation)	I_{SB3}	—	1	5	μA	$\overline{RES} = V_{SS} \pm 0.2 \text{ V}$
(2-chip operation)	I_{SB3}	—	2	10	μA	
Operating V_{CC} current (1-chip operation)	I_{CC1}	—	20	25	mA	$I_{out} = 0 \text{ mA}$, $f = 0.2 \text{ MHz}$
(2-chip operation)	I_{CC1}	—	40	50	mA	
(1-chip operation)	I_{CC2}	—	30	50	mA	$I_{out} = 0 \text{ mA}$, $f = 20 \text{ MHz}$
(2-chip operation)	I_{CC2}	—	60	100	mA	
Operating V_{CC} current (Program) (1-chip operation)	I_{CC3}	—	20	40	mA	In programming
(2-chip operation)	I_{CC3}	—	40	80	mA	
Operating V_{CC} current (Erase) (1-chip operation)	I_{CC4}	—	20	40	mA	In erase
(2-chip operation)	I_{CC4}	—	40	80		
Input voltage	V_{IL}	$-0.3^{*1, 2}$	—	$V_{CC} \times 0.3$	V	
	V_{IH}	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage (\overline{RES} pin)	V_{ILR}	-0.2	—	0.2	V	
	V_{IHR}	$V_{CC} - 0.2$	—	$V_{CC} + 0.2$	V	
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$)	V_{OH}	$V_{CC} \times 0.8$	—	—	V	$I_{OH} = -2 \text{ mA}$
($V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$)	V_{OH}	2.4	—	—	V	$I_{OH} = -2 \text{ mA}$

- Notes: 1. V_{IL} min = -1.0 V for pulse width 50 ns in the read operation. V_{IL} min = -2.0 V for pulse width 20 ns in the read operation.
2. V_{IL} min = -0.6 V for pulse width 20 ns in the erase/data programming operation.
3. V_{IH} max = $V_{CC} + 1.5 \text{ V}$ for pulse width 20 ns. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

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AC Characteristics ($V_{CC} = 2.7\text{ V}$ to 3.6 V , $T_a = 0$ to $+70^\circ\text{C}$)

Test Conditions

- Input pulse levels: $0.7\text{ V}/2.7\text{ V}$
- Input pulse levels for $\overline{\text{RES}}$: $0.2\text{ V}/V_{CC} - 0.2\text{ V}$
- Input rise and fall time: 5 ns
- Output load: $1\text{ TTL gate} + 100\text{ pF}$ (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V , 1.8 V

Power on and off, Serial Read Mode

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Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Write cycle time	t_{CWC}	120	—	—	ns		
Serial clock cycle time ($V_{CC} = 2.7\text{ V}$ to 3.6 V)	t_{SCC}	80	—	—	ns		
Serial clock cycle time ($V_{CC} = 3.0\text{ V}$ to 3.6 V)	t_{SCC}	60	—	—	ns		
$\overline{\text{CE}}$ setup time	t_{CES}	0	—	—	ns		
$\overline{\text{CE}}$ hold time	t_{CEH}	0	—	—	ns		
Write pulse time	t_{WP}	60	—	—	ns	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$	
Write pulse high time	t_{WPH}	40	—	—	ns		
Address setup time	t_{AS}	50	—	—	ns		
Address hold time	t_{AH}	10	—	—	ns		
Data setup time	t_{DS}	50	—	—	ns		
Data hold time	t_{DH}	10	—	—	ns		
SC to output delay ($V_{CC} = 2.7\text{ V}$ to 3.6 V)	t_{SAC}	—	—	80	ns	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$	
SC to output delay ($V_{CC} = 3.0\text{ V}$ to 3.6 V)	t_{SAC}	—	—	60	ns		
$\overline{\text{OE}}$ setup time for SC	t_{OES}	0	—	—	ns		
$\overline{\text{OE}}$ low to output low-Z	t_{OEL}	0	—	40	ns		
$\overline{\text{OE}}$ setup time before read	t_{OER}	250	—	—	ns		
$\overline{\text{OE}}$ setup time before command write	t_{OEWs}	0	—	—	ns		

		HN29W51214S					
		-80					
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
SC to output hold	t _{SH}	15	—	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
\overline{OE} high to output float	t _{DF}	—	—	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	1
\overline{WE} to SC delay time	t _{WSD}	50	—	—	μs		2
\overline{RES} to \overline{CE} setup time	t _{RP}	1	—	—	ms		
SC to \overline{OE} hold time	t _{SOH}	50	—	—	ns		
SC pulse width (V _{CC} = 2.7 V to 3.6 V)	t _{SP}	35	—	—	ns		
SC pulse width (V _{CC} = 3.0 V to 3.6 V)	t _{SP}	25	—	—	ns		
SC pulse low time (V _{CC} = 2.7 V to 3.6 V)	t _{SPL}	35	—	—	ns		
SC pulse low time (V _{CC} = 3.0 V to 3.6 V)	t _{SPL}	25	—	—	ns		
SC setup time for \overline{CE}	t _{SCS}	0	—	—	ns		
\overline{CDE} setup time for \overline{WE}	t _{CDS}	0	—	—	ns		
\overline{CDE} hold time for \overline{WE}	t _{CDH}	20	—	—	ns		
V _{CC} setup time for \overline{RES}	t _{VRS}	1	—	—	μs	$\overline{CE} = V_{IH}$	
\overline{RES} to V _{CC} hold time	t _{VRH}	1	—	—	μs	$\overline{CE} = V_{IH}$	
\overline{CE} setup time for \overline{RES}	t _{CESR}	1	—	—	μs		
RDY/ \overline{Busy} undefined for V _{CC} off	t _{DFP}	0	—	—	ns		
\overline{RES} high to device ready	t _{BSY}	—	—	1	ms		
\overline{CE} pulse high time	t _{CPH}	200	—	—	ns		
\overline{CE} , \overline{WE} setup time for \overline{RES}	t _{CWRS}	0	—	—	ns		
\overline{RES} to \overline{CE} , \overline{WE} hold time	t _{CWRH}	0	—	—	ns		
SC setup for \overline{WE}	t _{SW}	50	—	—	ns		
\overline{CE} hold time for \overline{OE}	t _{COH}	0	—	—	ns		
SA (2) to CA (2) delay time	t _{SCD}	—	—	30	μs		
RDY/ \overline{Busy} setup for SC	t _{RS}	200	—	—	ns		
Time to device busy on read mode	t _{DBR}	—	—	1	μs		
Busy time on reset mode	t _{RBSY}	—	45	—	μs		

Notes: 1. t_{DF} is a time after which the I/O pins become open.

2. t_{WSD} (min) is specified as a reference point only for SC, if t_{WSD} is greater than the specified t_{WSD} (min) limit, then access time is controlled exclusively by t_{SAC} .

HN29W51214S Series

Program, Erase and Erase Verify

		HN29W51214S					
		-80					
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Write cycle time	t _{CWC}	120	—	—	ns		
Serial clock cycle time (V _{CC} = 2.7 V to 3.6 V)	t _{SCC}	80	—	—	ns		
Serial clock cycle time (V _{CC} = 3.0 V to 3.6 V)	t _{SCC}	60	—	—	ns		
\overline{CE} setup time	t _{CES}	0	—	—	ns		
\overline{CE} hold time	t _{CEH}	0	—	—	ns		
Write pulse time	t _{WP}	60	—	—	ns		
Write pulse high time	t _{WPH}	40	—	—	ns		
Address setup time	t _{AS}	50	—	—	ns		
Address hold time	t _{AH}	10	—	—	ns		
Data setup time	t _{DS}	50	—	—	ns		
Data hold time	t _{DH}	10	—	—	ns		
\overline{OE} setup time before command write	t _{OEWS}	0	—	—	ns		
\overline{OE} setup time before status polling	t _{OEPS}	40	—	—	ns		
\overline{OE} setup time before read	t _{OER}	250	—	—	ns		
Time to device busy	t _{DB}	—	—	150	ns		
Time to device busy on read mode	t _{DBR}	—	—	1	μs		
Auto erase time	t _{ASE}	—	1.5	10.0	ms		
Auto program time Program(1), (3)	t _{ASP}	—	3.0	20.0	ms		
Program(2)	t _{ASP}	—	2.5	20.0	ms		
Program(4)	t _{ASP}	—	3.5	30.0	ms		
\overline{WE} to SC delay time	t _{WSD}	50	—	—	μs		
\overline{WE} to SC delay time on recovery read mode	t _{WSDR}	2	—	—	μs		
\overline{CE} pulse high time	t _{CPH}	200	—	—	ns		

		HN29W51214S					
		-80					
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
SC pulse width (V _{CC} = 2.7 V to 3.6 V)	t _{SP}	35	—	—	ns		
SC pulse width (V _{CC} = 3.0 V to 3.6 V)	t _{SP}	25	—	—	ns		
SC pulse low time (V _{CC} = 2.7 V to 3.6 V)	t _{SPL}	35	—	—	ns		
SC pulse low time (V _{CC} = 3.0 V to 3.6 V)	t _{SPL}	25	—	—	ns		
Data setup time for SC	t _{SDS}	0	—	—	ns		
Data hold time for SC	t _{SDH}	30	—	—	ns	CDE = V _{IL}	
SC setup for WE	t _{SW}	50	—	—	ns		
SC setup for CE	t _{SCS}	0	—	—	ns		
SC hold time for WE	t _{SCHW}	20	—	—	ns		
CE to output delay	t _{CE}	—	—	120	ns		
OE to output delay	t _{OE}	—	—	60	ns		
OE high to output float	t _{DF}	—	—	40	ns		1
RES to CE setup time	t _{RP}	1	—	—	ms		
CDE setup time for WE	t _{CDS}	0	—	—	ns		
CDE hold time for WE	t _{CDH}	20	—	—	ns		
CDE setup time for SC	t _{CDSS}	1.5	—	—	μs		
CDE hold time for SC	t _{CDSH}	30	—	—	ns		
Next cycle ready time	t _{RDY}	0	—	—	ns		
CDE to OE hold time	t _{CDOH}	50	—	—	ns		
CDE to output delay (V _{CC} = 2.7 V to 3.6 V)	t _{CDAC}	—	—	80	ns		
CDE to output delay (V _{CC} = 3.0 V to 3.6 V)	t _{CDAC}	—	—	60	ns		
CDE to output invalid	t _{CDF}	—	—	100	ns		
CE setup time for OE	t _{COS}	0	—	—	ns		
CE hold time for OE	t _{COH}	0	—	—	ns		
CDE to OE setup time	t _{CDOS}	20	—	—	ns		
OE setup time for SC	t _{OES}	0	—	—	ns		
OE low to output low-Z	t _{OEL}	0	—	40	ns		

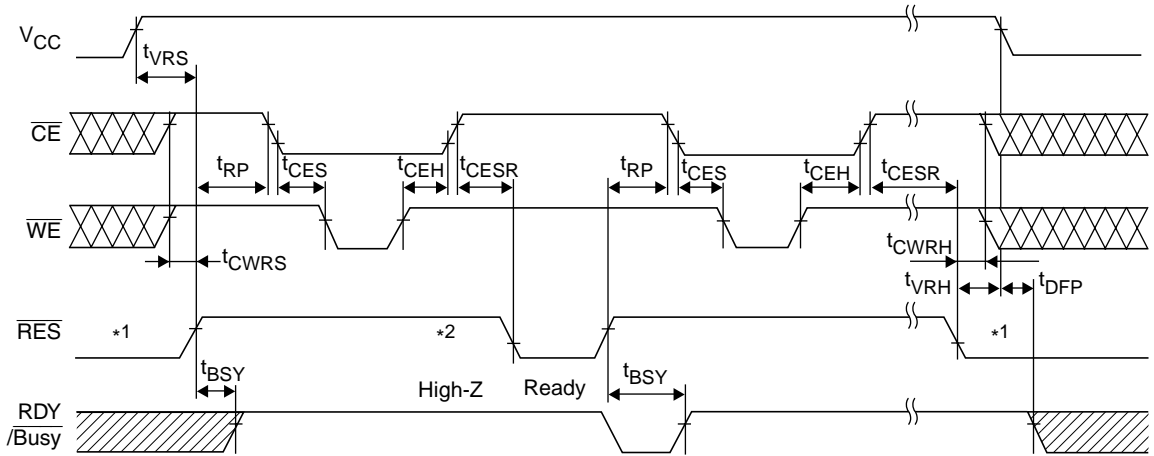
HN29W51214S Series


		HN29W51214S				Test conditions	Notes
		-80			Unit		
Parameter	Symbol	Min	Typ	Max			
SC to output delay (V _{CC} = 2.7 V to 3.6 V)	t _{SAC}	—	—	80	ns		
SC to output delay (V _{CC} = 3.0 V to 3.6 V)	t _{SAC}	—	—	60	ns		
SC to output hold	t _{SH}	15	—	—	ns		
RDY/ $\overline{\text{Busy}}$ setup for SC	t _{RS}	200	—	—	ns		
$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$	t _{CWH}	1.0	—	—	μs		
$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$ on recovery read mode	t _{CWHR}	2	—	—	μs		
$\overline{\text{WE}}$ hold time for $\overline{\text{WE}}$	t _{WWH}	1	—	—	μs		
Busy time on read mode	t _{RBSY}	—	45	—	μs		

Note: 1. t_{DF} is a time after which the I/O pins become open.

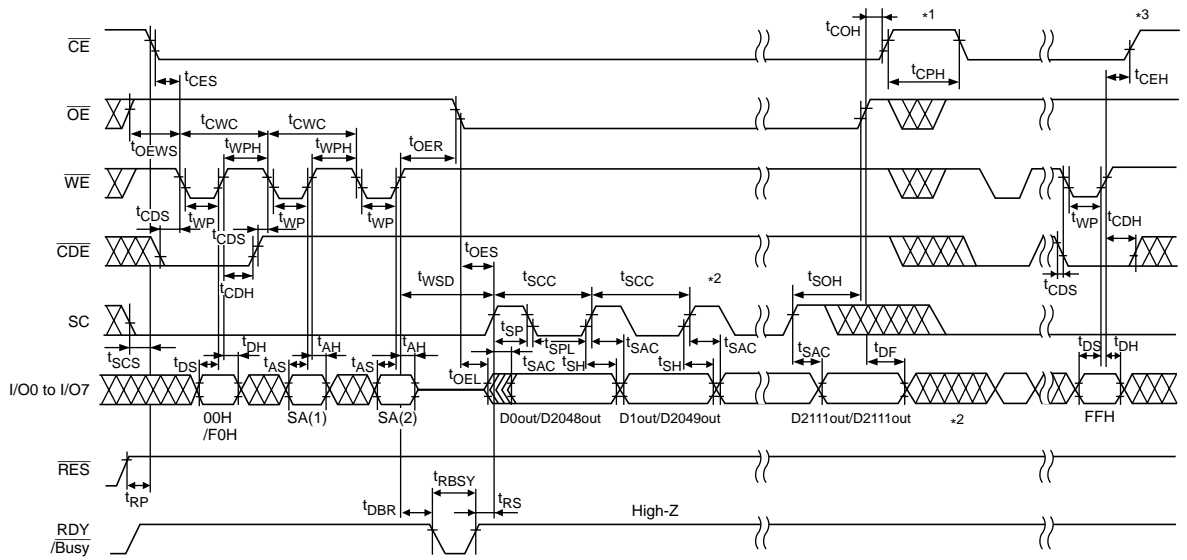
Timing Waveforms

Power on and off Sequence



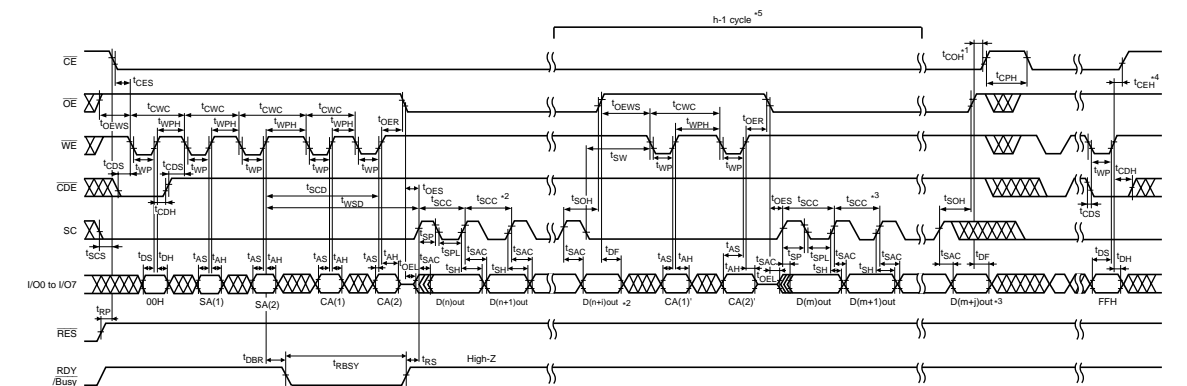
- Notes:
1. \overline{RES} must be kept at the V_{ILR} level referred to DC characteristics at the rising and falling edges of V_{CC} to guarantee data stored in the chip.
 2. \overline{RES} must be kept at the V_{IHR} level referred to DC characteristics while I/O7 outputs the V_{OL} level in the status data polling and $\overline{RDY}/\text{Busy}$ outputs the V_{OL} level.
 3.  : Undefined

Serial Read (1) (2) Timing Waveform



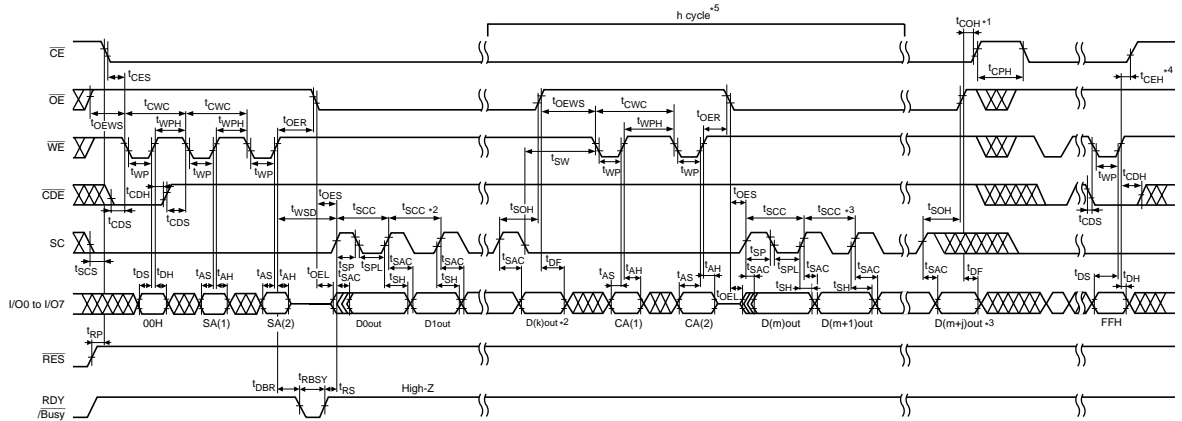
- Notes: 1. The status returns to the standby at the rising edge of \overline{CE} .
 2. Output data is not valid after the number of the SC pulse exceeds 2112 and 64 in the serial read mode (1) and (2), respectively.
 3. After any commands are written, the status can return to the standby after the command FFH is input and \overline{CE} turns to the V_{IH} level.

Serial Read (1) with CA before SC Timing Waveform



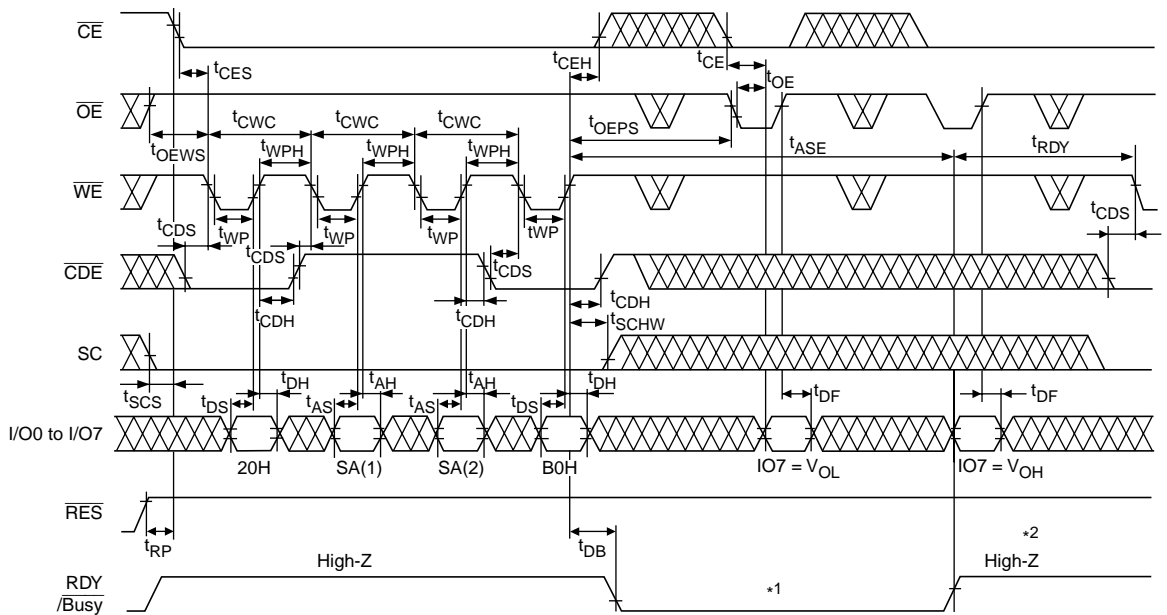
- Notes: 1. The status returns to the Standby at the rising edge of \overline{CE} .
 2. Output data is not valid after the number of the SC pulse exceeds $(2112-n)$. ($i \leq 2111-n$, $0 \leq n \leq 2111$)
 3. Output data is not valid after the number of the SC pulse exceeds $(2112-m)$. ($j \leq 2111-m$, $0 \leq m \leq 2111$)
 4. After any commands are written, the status can return to the standby after the command FFH is input and \overline{CE} turns to the V_{IH} level.
 5. This interval can be repeated (h-1) cycle. ($1 \leq h \leq 2048 + 64$)

Serial Read (1) with CA after SC Timing Waveform

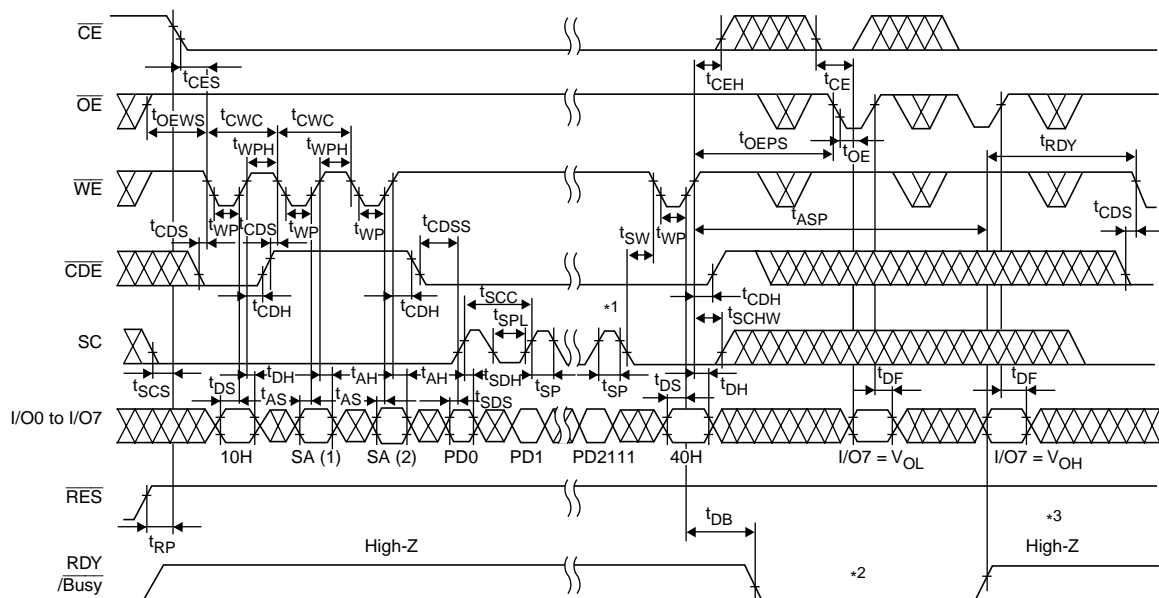


- Notes:
1. The status returns to the Standby at the rising edge of \overline{CE} .
 2. Output data is not valid after the number of the SC pulse exceeds 2112. ($0 \leq k \leq 2111$)
 3. Output data is not valid after the number of the SC pulse exceeds $(2112-m)$. ($j \leq 2111-m, 0 \leq m \leq 2111$)
 4. After any commands are written, the status can return to the standby after the command FFH is input and \overline{CE} turns to the V_{IH} level.
 5. This interval can be repeated h cycle. ($1 \leq h \leq 2048 + 64$)

Erase and Status Data Polling Timing Waveform (Sector Erase)

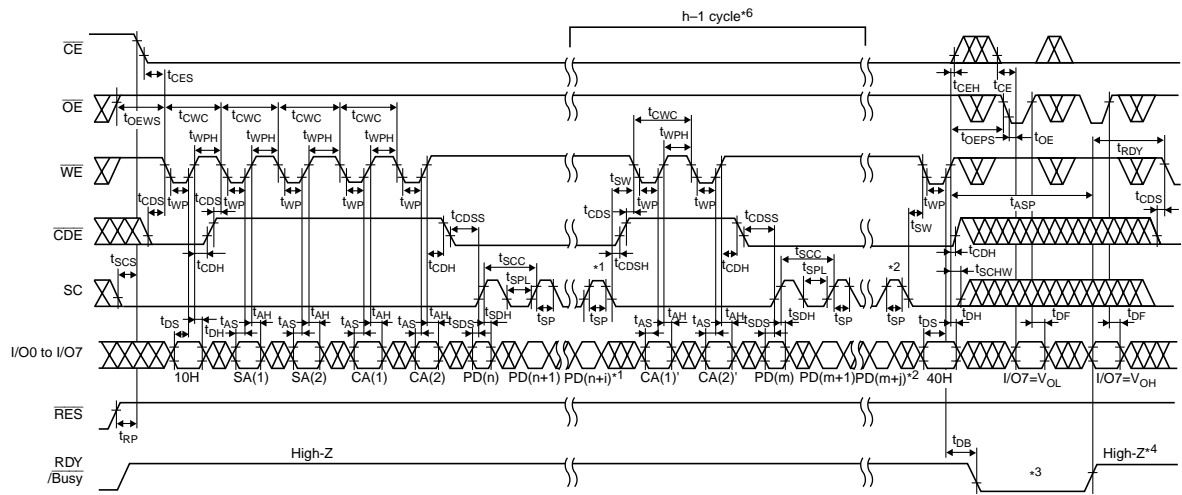


- Notes:
1. Any commands, including reset command FFH, cannot be input while RDY/Busy outputs a V_{OL} .
 2. The status returns to the standby status after RDY/Busy returns to High-Z.



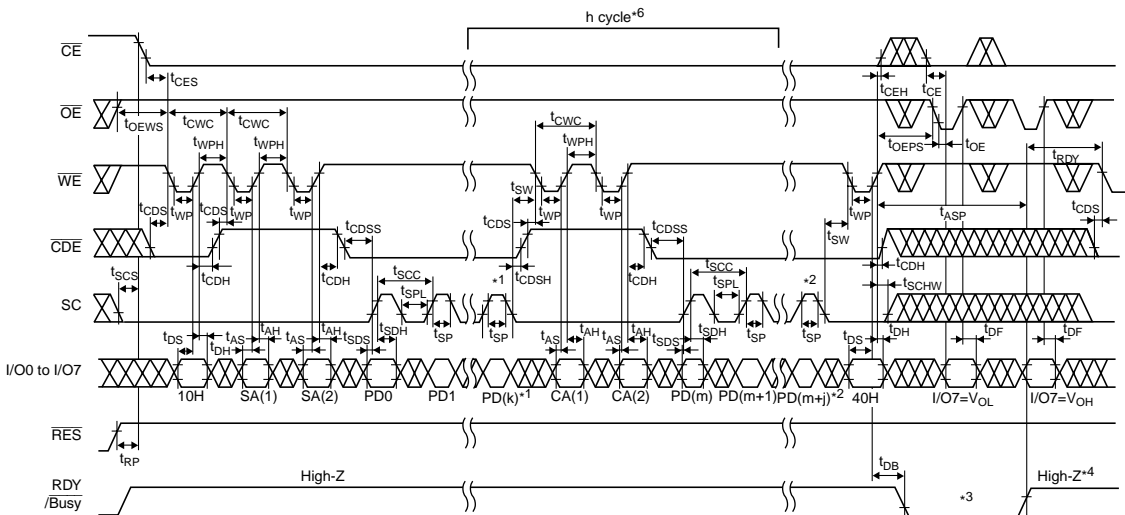
- Notes:
1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.
 2. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 3. The status returns to the standby status after RDY/Busy returns to High-Z.
 4. By using program (1), data can be programmed additionally for each sector before erase.

Program (1) with CA before SC and Status Data Polling Timing Waveform



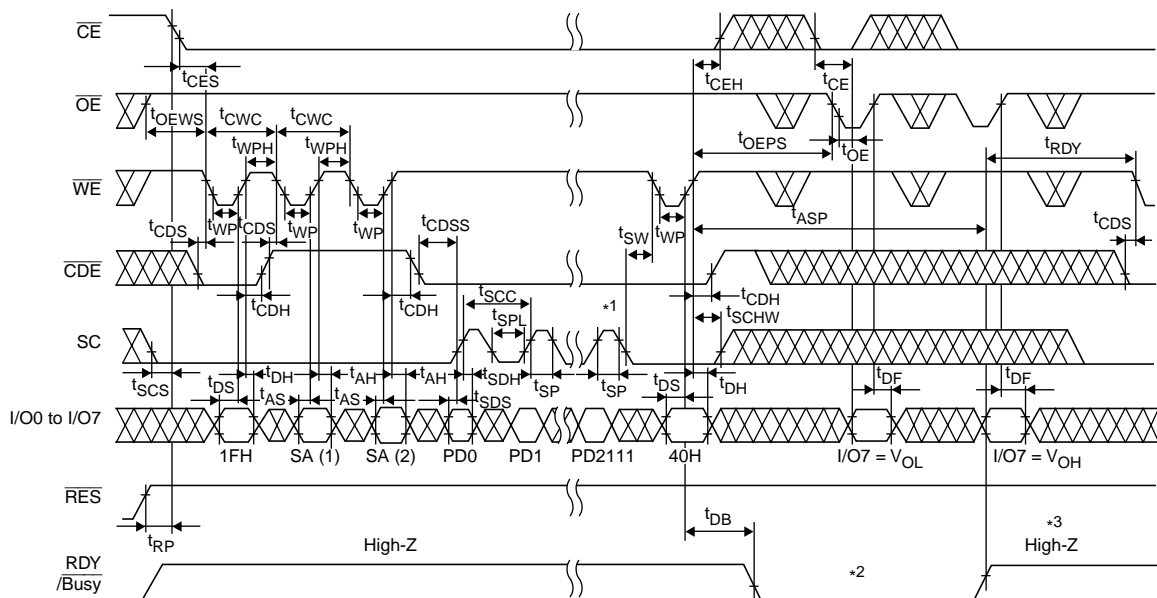
- Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - n)$, $(i \leq 2111 - n, 0 \leq n \leq 2111)$
 2. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - m)$, $(j \leq 2111 - m, 0 \leq m \leq 2111)$
 3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 4. The status returns to the standby status after RDY/Busy returns to High-Z.
 5. By using program (1), data can be programmed additionally for each sector before erase.
 6. This interval can be repeated $(h - 1)$ cycle, $(1 \leq h \leq 2048 + 64)$

Program (1) with CA after SC and Status Data Polling Timing Waveform



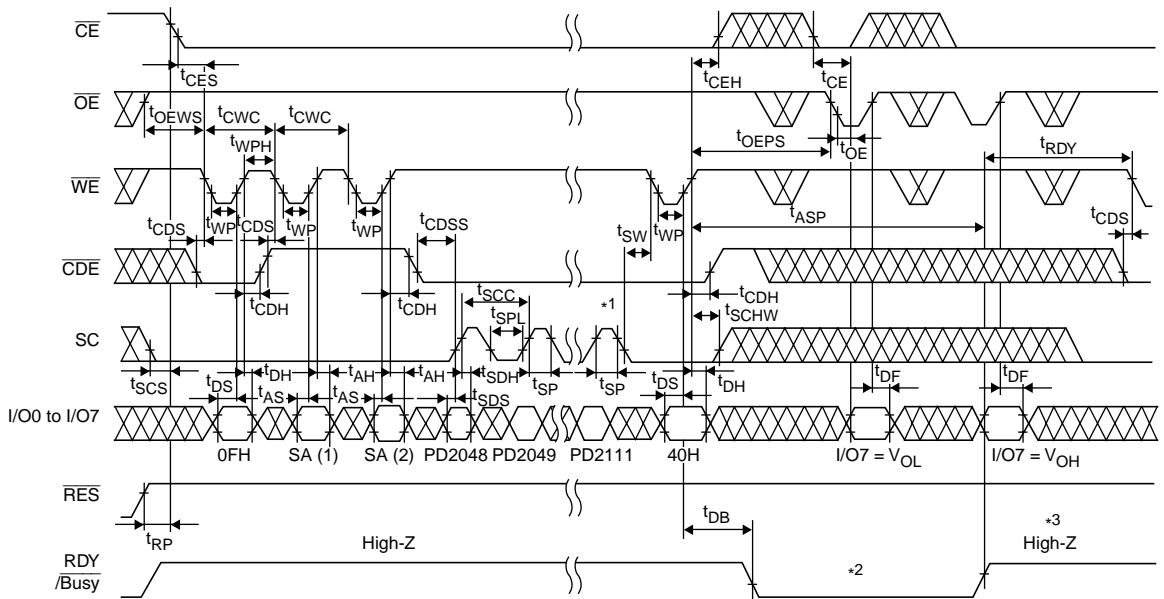
- Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112, $(0 \leq k \leq 2111)$
 2. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - m)$, $(j \leq 2111 - m, 0 \leq m \leq 2111)$
 3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 4. The status returns to the standby status after RDY/Busy returns to High-Z.
 5. By using program (1), data can be programmed additionally for each sector before erase.
 6. This interval can be repeated h cycle, $(1 \leq h \leq 2048 + 64)$

Program (2) and Status Data Polling Timing Waveform

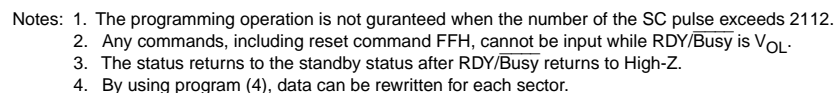


- Notes:
1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.
 2. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL}.
 3. The status returns to the standby status after RDY/Busy returns to High-Z.
 4. By using program (2), the programmed data of each sector must be erased before programming next data.

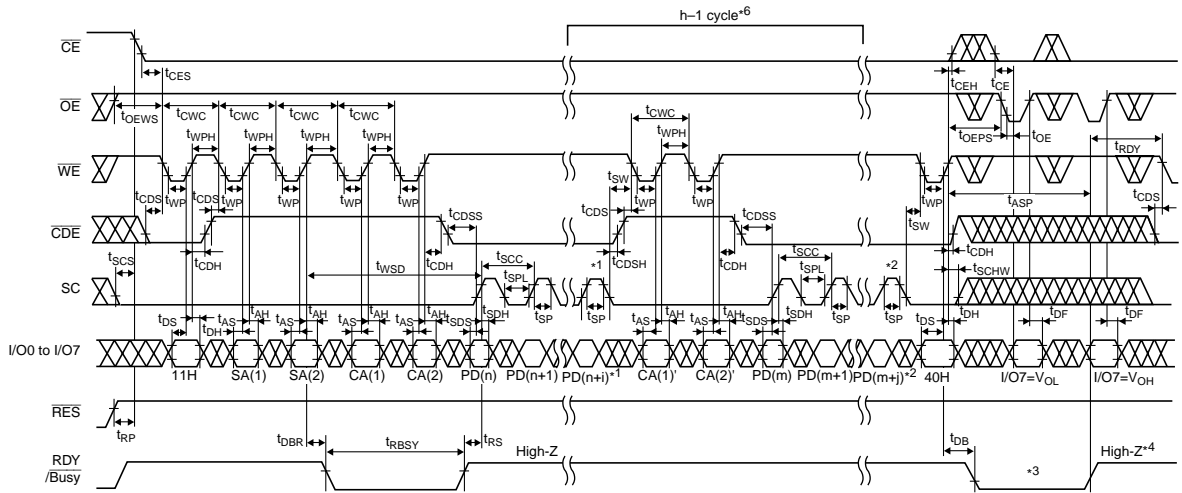
Program (3) and Status Data Polling Timing Waveform



- Notes:
1. The programming operation is not guaranteed when the number of the SC pulse exceeds 64.
 2. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 3. The status returns to the standby status after RDY/Busy returns to High-Z.
 4. By using program (3), the data can be programmed additionally for each sector before erase.

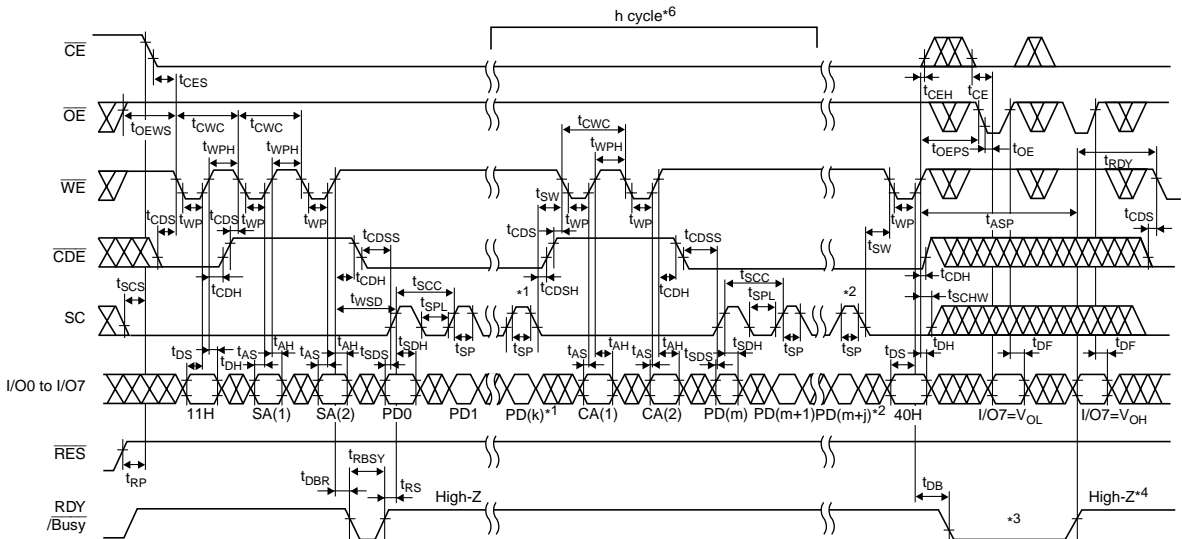


Program (4) with CA before SC and Status Data Polling Timing Waveform



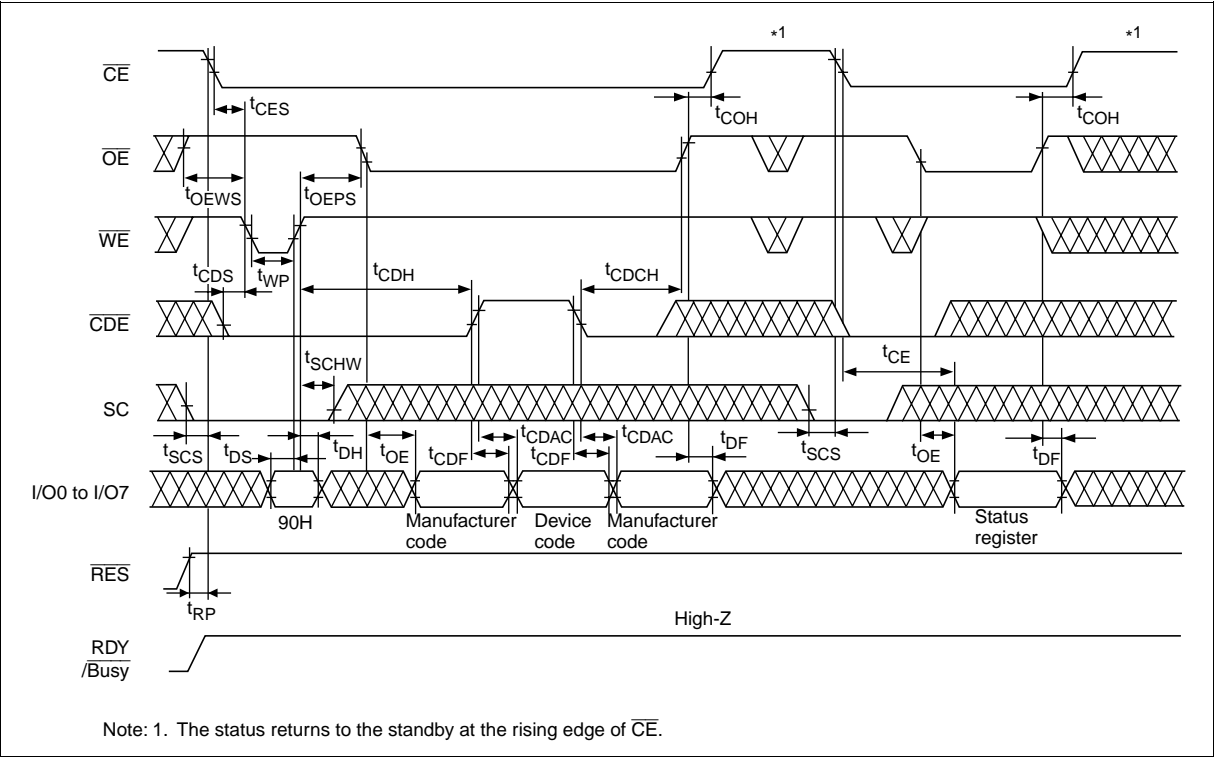
- Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - n)$, $(i \leq 2111 - n, 0 \leq n \leq 2111)$
 2. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - m)$, $(j \leq 2111 - m, 0 \leq m \leq 2111)$
 3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 4. The status returns to the standby status after RDY/Busy returns to High-Z.
 5. By using program (4), data can be rewritten for each sector.
 6. This interval can be repeated $(h - 1)$ cycle, $(1 \leq h \leq 2048 + 64)$

Program (4) with CA after SC and Status Data Polling Timing Waveform

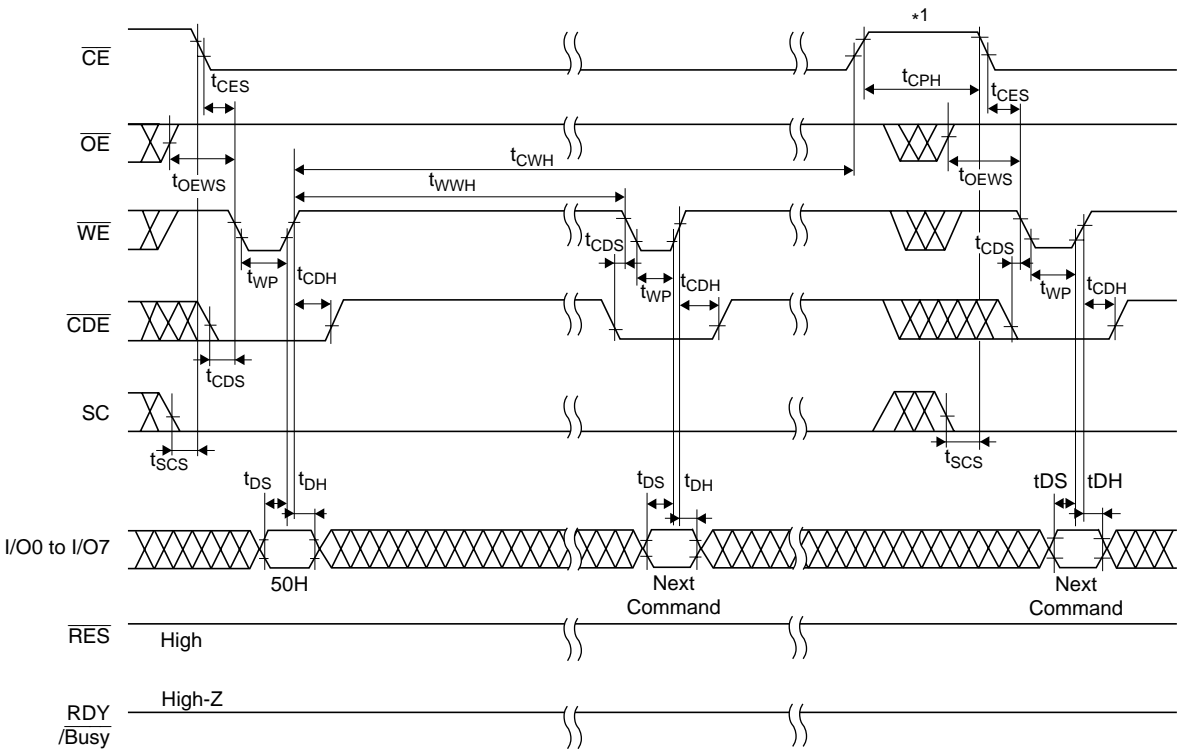


- Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112, $(0 \leq k \leq 2111)$
 2. The programming operation is not guaranteed when the number of the SC pulse exceeds $(2112 - m)$, $(j \leq 2111 - m, 0 \leq m \leq 2111)$
 3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 4. The status returns to the standby status after RDY/Busy returns to High-Z.
 5. By using program (4), data can be rewritten for each sector.
 6. This interval can be repeated h cycle, $(1 \leq h \leq 2048 + 64)$

ID and Status Register Read Timing Waveform



Clear Status Register Timing Waveform



Note 1. The status returns to the standby at the rising edge of \overline{CE} .

Function Description

Status Register: The HN29W51214S outputs the operation status data as follows: I/O7 pin outputs a V_{OL} to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a V_{OH} when the operation finishes. I/O5 and I/O4 pins output V_{OL} s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output V_{OH} s, it indicates that these operations have timed out. When these pins monitor, I/O7 pin must turn to a V_{OH} . To execute other erase and program operation, the status data must be cleared after a time out occurs. From I/O0 to I/O3 pins are reserved for future use. The pins output V_{OL} s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

I/O	Flag definition	Definition
I/O7	Ready/ $\overline{\text{Busy}}$	V_{OH} = Ready, V_{OL} = Busy
I/O6	Reserved	Outputs a V_{OL} and should be masked out during the status data polling mode.
I/O5	Erase check	V_{OH} = Fail, V_{OL} = Pass
I/O4	Program check	V_{OH} = Fail, V_{OL} = Pass
I/O3	Reserved	Outputs a V_{OL} and should be masked out during the status data polling mode.
I/O2	Reserved	
I/O1	Reserved	
I/O0	Reserved	

Requirement for System

Specifications

Item	Min	Typ	Max	Unit
Usable sectors (initially)	32,114	—	32,768	sector
Spare sectors (1-chip operation)	290	—	—	sector
(2-chip operation)	580	—	—	sector
ECC (Error Correction Code)	3	—	—	bit/sector
Program/Erase endurance	—	—	3×10^5	cycle

Unusable Sector

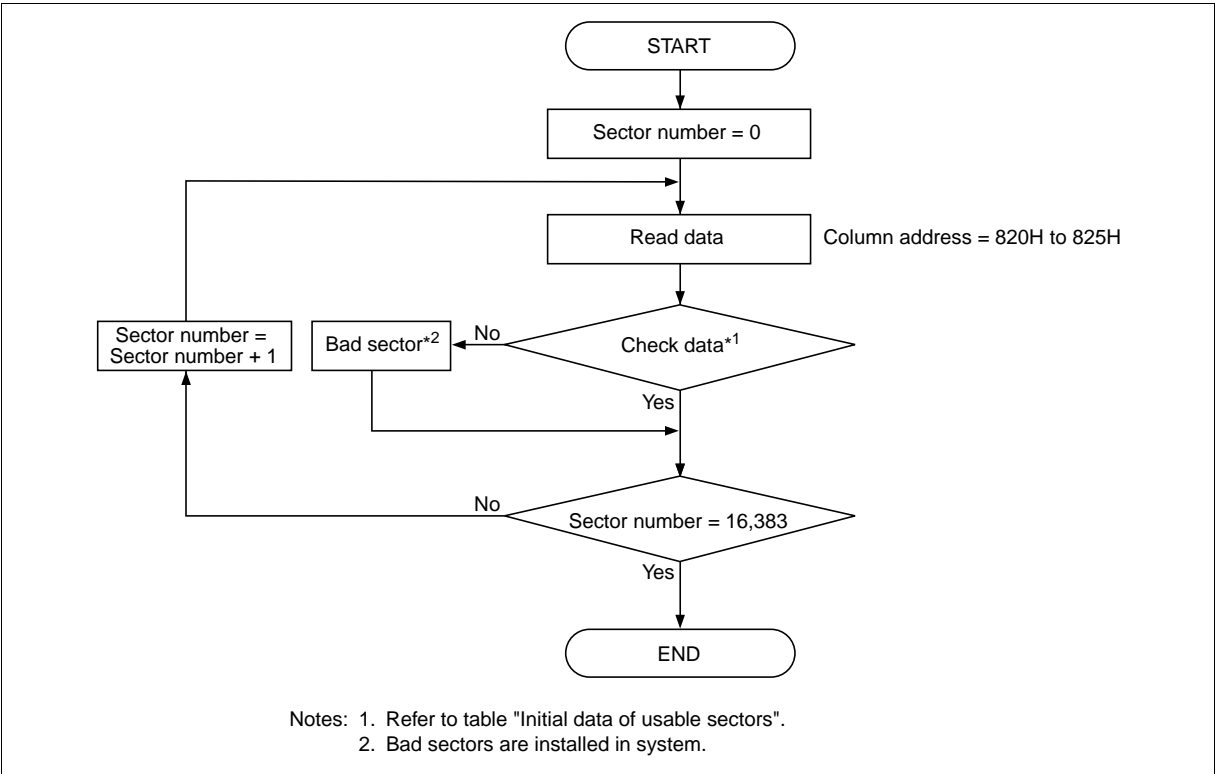
Initially, the HN29W51214S includes unusable sectors. The unusable sectors must be distinguished from the usable sectors by the system as follows.

1. Check the partial invalid sectors in the devices on the system. The usable sectors were programmed the following data. Refer to the flowchart “The Unusable Sector Indication Flow”.

Initial Data of Usable Sectors

Column address	0H to 81FH	820H	821H	822H	823H	824H	825H	826H to 83FH
Data	FFH	1CH	71H	C7H	1CH	71H	C7H	FFH

2. Do not erase and program to the partial invalid sectors by the system.

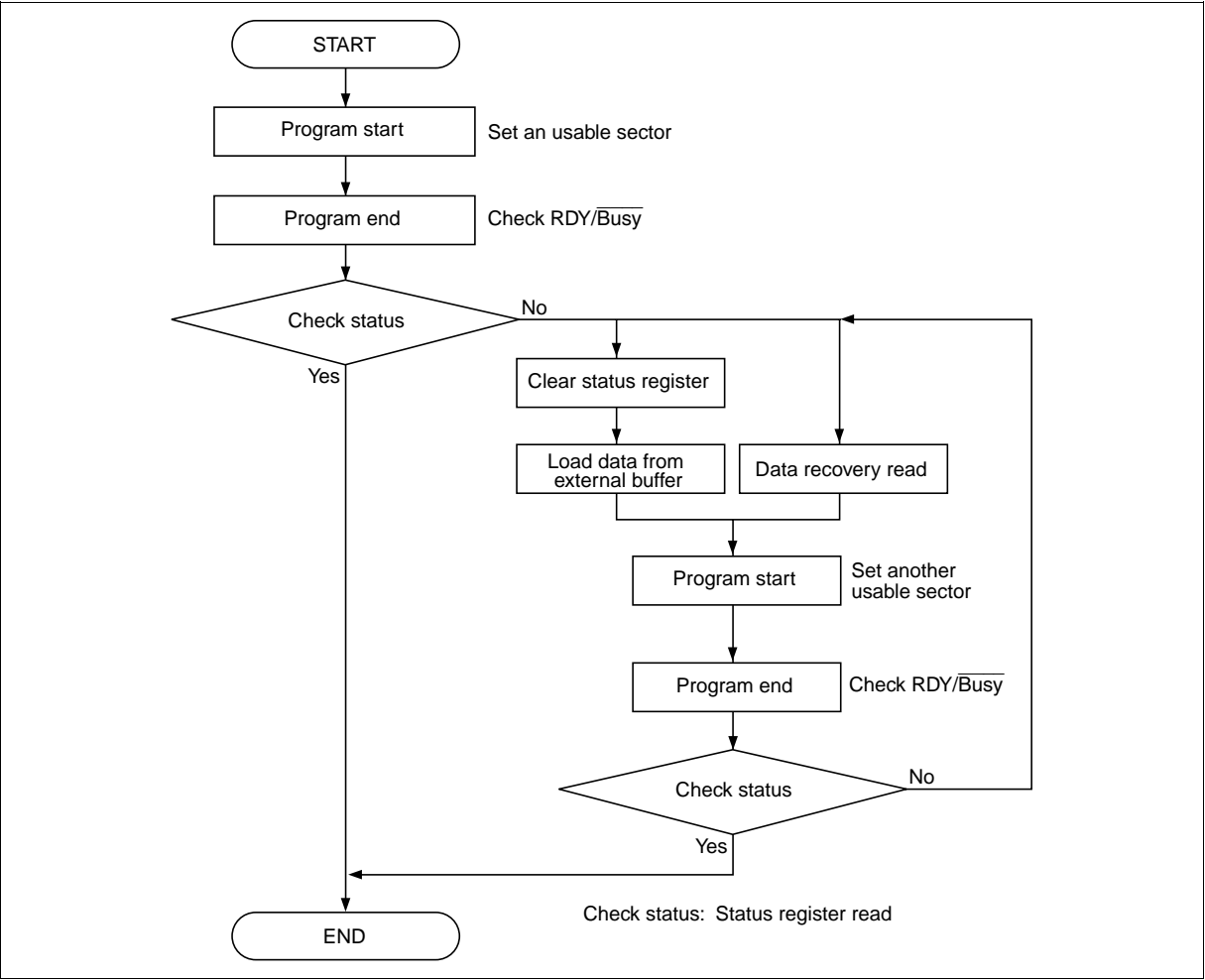


The Unusable Sector Indication Flow (1-chip)

Requirements for High System Reliability

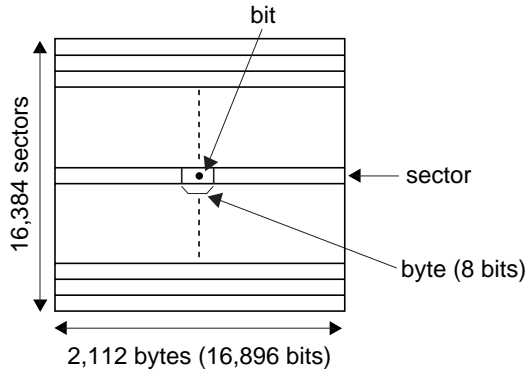
The device may fail during a program, erase or read operation due to write or erase cycles. The following architecture will enable high system reliability if a failure occurs.

1. For an error in read operation: An error correction more than 3-bit error correction per each sector read is required for data reliability.
2. For errors in program or erase operations: The device may fail during a program or erase operation due to write or erase cycles. The status register indicates if the erase and program operation complete in a finite time. When an error occurred in the sector, try to reprogram the data into another sector. Avoid further system access to the sector that error happens. Typically, recommended number of a spare sectors are 1.8% of initial usable 32,114 sectors by each device. If the number of failed sectors exceeds the number of the spare sectors, usable data area in the device decreases. For the reprogramming, do not use the data from the failed sectors, because the data from the failed sectors are not fixed. So the reprogram data must be the data reloaded from external buffer, or use the Data recovery read mode (see the “Mode Description” and under figure “Spare Sector Replacement Flow after Program Error”). To avoid consecutive sector failures, choose addresses of spare sectors as far as possible from the failed sectors.



Spare Sector Replacement Flow after Program Error

Memory Structure



Bit: Minimum unit of data.

Byte: Input/output data unit in programming and reading. (1 byte = 8 bits)

Sector: Page unit in erase, programming and reading. (1 sector = 2,112 bytes = 16,896 bits)

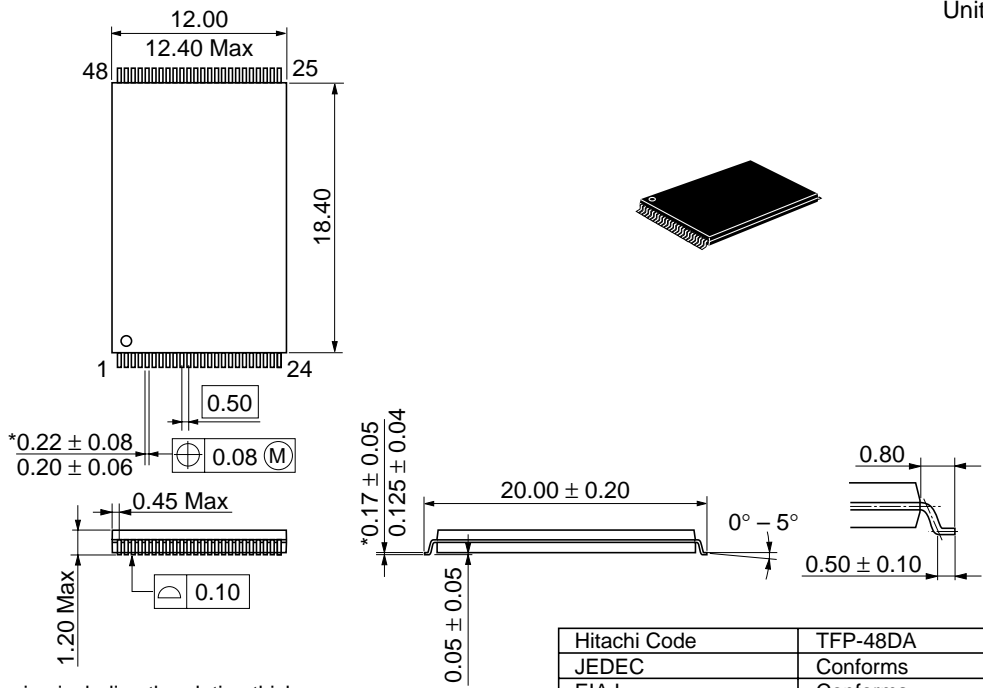
Device: 1 device = 16,384 sectors.

HN29W51214S Series

Package Dimensions

HN29W51214ST Series (TFP-48DA)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-48DA
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.52 g

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