

Micropower Precision, Dual/Quad CMOS Rail-to-Rail Input/Output Amplifiers

FEATURES

- **Maximum Offset Voltage of 25 μ V (25°C)**
- **Maximum Offset Drift of 0.7 μ V/°C**
- **Maximum Input Bias:**
1pA (25°C)
50pA ($\leq$ 85°C)
- Micropower: 54 μ A per Amp
- 95dB CMRR (Min)
- 100dB PSRR (Min)
- Input Noise Voltage Density: 16nV/ $\sqrt{\text{Hz}}$
- Rail-to-Rail Inputs and Outputs
- 2.7V to 5.5V Operation Voltage
- LTC6078 Available in 8-Lead MSOP and 10-Lead DFN Packages; LTC6079 Available in 16-Lead SSOP and DFN Packages

APPLICATIONS

- Photodiode Amplifier
- High Impedance Sensor Amplifier
- Microvolt Accuracy Threshold Detection
- Instrumentation Amplifiers
- Battery Powered Applications

DESCRIPTION

The LTC®6078/LTC6079 are dual/quad, low offset, low noise operational amplifiers with low power consumption and rail-to-rail input/output swing.

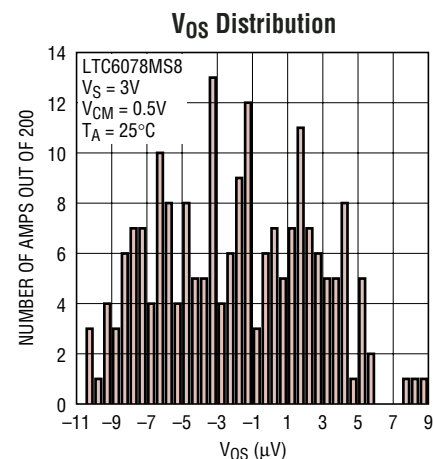
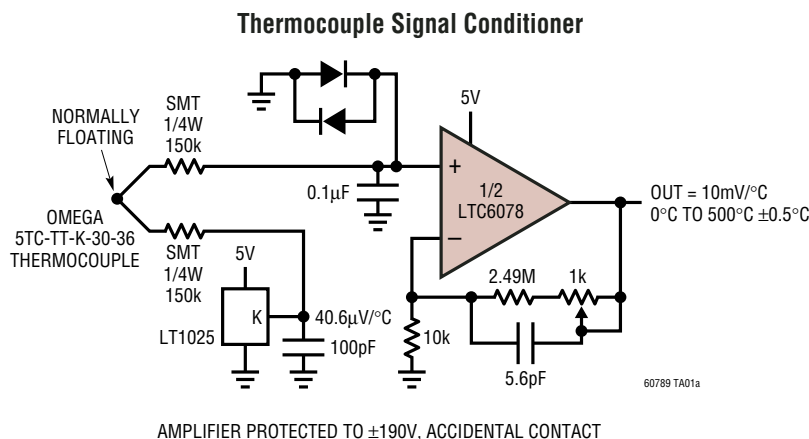
Input offset voltage is trimmed to less than 25 μ V and the CMOS inputs draw less than 50pA of bias current. The low offset drift, excellent CMRR, and high voltage gain make it a good choice for precision signal conditioning.

Each amplifier draws only 54 μ A current on a 3V supply. The micropower, rail-to-rail operation of the LTC6078/LTC6079 is well suited for portable instruments and single supply applications.

The LTC6078/LTC6079 are specified on power supply voltages of 3V and 5V from –40 to 125°C. The dual amplifier LTC6078 is available in 8-lead MSOP and 10-lead DFN packages. The quad amplifier LTC6079 is available in 16-lead SSOP and DFN packages.

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TYPICAL APPLICATION



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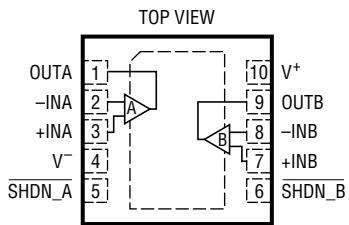
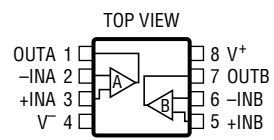
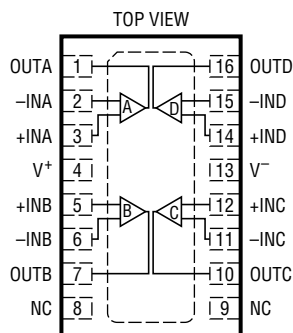
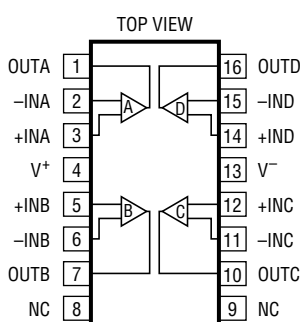
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)	6V
Input Voltage	V^- to V^+
Output Short Circuit Duration (Note 2)	Indefinite
Operating Temperature Range (Note 3)	
LTC6078C, LTC6079C	-40°C to 85°C
LTC6078I, LTC6079I	-40°C to 85°C
LTC6078H, LTC6079H	-40°C to 125°C
(Not Available in DFN Package)	

Specified Temperature Range (Note 4)	
LTC6078C, LTC6079C	0°C to 70°C
LTC6078I, LTC6079I	-40°C to 85°C
LTC6078H, LTC6079H	-40°C to 125°C
Junction Temperature	
DFN Packages	125°C
All Other Packages	150°C
Storage Temperature Range	
DFN Packages	-65°C to 125°C
All Other Packages	-65°C to 150°C
Lead Temperature (Soldering, 10 Sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW  DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 43^{\circ}\text{C/W}$ UNDERSIDE METAL CONNECTED TO V^{-}	TOP VIEW  MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 200^{\circ}\text{C/W}$	ORDER PART NUMBER	DD PART MARKING*
		LTC6078CDD LTC6078IDD	LBBB LBBB
TOP VIEW  DHC PACKAGE 16-LEAD (5mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 43^{\circ}\text{C/W}$ UNDERSIDE METAL CONNECTED TO V^{-}	TOP VIEW  GN PACKAGE 16-LEAD PLASTIC SSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 110^{\circ}\text{C/W}$	ORDER PART NUMBER	MS8 PART MARKING*
		LTC6078ACMS8 LTC6078CMS8 LTC6078AIMS8 LTC6078IMS8 LTC6078AHMS8 LTC6078HMS8	LTAJZ LTAJZ LTAJZ LTAJZ LTAJZ LTAJZ
		ORDER PART NUMBER	DHC PART MARKING*
		LTC6079CDHC LTC6079IDHC	6079 6079
		ORDER PART NUMBER	GN PART MARKING
		LTC6079CGN LTC6079IGN LTC6079HGN	6079 6079I 6079H

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

*The temperature grades and parametric grades are identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Offset Voltage (Note 5)	LTC6078MS8, LTC6078AMS8, LTC6079GN							μV
		$V_{\text{CM}} = 0.5\text{V}, 2.5\text{V}$		± 7	± 25		± 7	± 25	μV
		LTC6078DD, LTC6079DHC		± 7	± 30				μV
		LTC6078AMS8	●	± 20	± 70		± 25	± 95	μV
		LTC6078MS8	●	± 25	± 97		± 30	± 135	μV
		LTC6079GN	●	± 30	± 115		± 35	± 165	μV
		LTC6078DD	●	± 30	± 120				μV
		LTC6079DHC	●	± 35	± 150				μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 5)	LTC6078AMS8	●	± 0.2	± 0.7		± 0.2	± 0.7	$\mu\text{V}/^\circ\text{C}$
		LTC6078MS8	●		± 1.1			± 1.1	$\mu\text{V}/^\circ\text{C}$
		LTC6078DD, LTC6079GN	●	± 0.3	± 1.4		± 0.3	± 1.4	$\mu\text{V}/^\circ\text{C}$
		LTC6079DHC	●	± 0.3	± 1.8				$\mu\text{V}/^\circ\text{C}$
I_{B}	Input Bias Current (Note 6)	$V_{\text{CM}} = V^+/2$		0.2	1		0.2	1	pA
		$V_{\text{CM}} = V^+/2$	●	10	50		150	350	pA
I_{OS}	Input Offset Current (Note 6)	$V_{\text{CM}} = V^+/2$		0.1			0.1		pA
		$V_{\text{CM}} = V^+/2$	●	0.5	25		10	100	pA
e_{n}	Input Noise Voltage	0.1Hz to 10Hz		1			1		$\mu\text{V}_{\text{P-P}}$
	Input Noise Voltage Density	$f = 1\text{kHz}$		18			18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$		16			16		$\text{nV}/\sqrt{\text{Hz}}$
i_{n}	Input Noise Current Density (Note 8)			0.56			0.56		$\text{fA}/\sqrt{\text{Hz}}$
	Input Common Mode Range		●	V^-	V^+	V^-	V^+		V
C_{DIFF}	Differential Input Capacitance			10			10		pF
C_{CM}	Common Mode Input Capacitance			18			18		pF
CMRR	Common Mode Rejection Ratio	All Packages		95	110		95	110	dB
		LTC6078AMS8	●	87	105		87	103	dB
		LTC6078AMS8	●	91	103		91	103	dB
		LTC6078MS8	●	85	102		85	100	dB
		LTC6078MS8	●	89	102		89	102	dB
		LTC6079GN	●	84	102		84	100	dB
		LTC6079GN	●	88	102		88	102	dB
		LTC6078DD, LTC6079DHC	●	83	100				dB
		LTC6078DD, LTC6079DHC	●	87	102				dB
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = 2.7\text{V to } 5.5\text{V}$		100	120		100	120	dB
			●	97			97		dB
V_{OUT}	Output Voltage, High (Referred to V^+)	No Load			1			1	mV
		$I_{\text{SOURCE}} = 0.2\text{mA}$	●	35	15		40	15	mV
		$I_{\text{SOURCE}} = 2\text{mA}$	●	350	150		400	150	mV
	Output Voltage, Low (Referred to V^-)	No Load			1			1	mV
		$I_{\text{SINK}} = 0.2\text{mA}$	●		10			10	mV
		$I_{\text{SINK}} = 2\text{mA}$	●		100			100	mV
A_{VOL}	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}, 0.5\text{V} \leq V_{\text{OUT}} \leq 2.5\text{V}$	●	115	130		110	125	dB
I_{SC}	Output Short-Circuit Current	Source	●	5	10		4	10	mA
		Sink	●	7	14		6	14	mA
SR	Slew Rate	$A_{\text{V}} = 1$			0.05			0.05	V/ μs
GBW	Gain-Bandwidth Product ($f_{\text{TEST}} = 10\text{kHz}$)	$R_{\text{L}} = 100\text{k}$		420	750		420	750	kHz
			●	360			320		kHz
Φ_0	Phase Margin	$R_{\text{L}} = 10\text{k}, C_{\text{L}} = 200\text{pF}$			66			66	Deg
t_{S}	Settling Time 0.1%	$A_{\text{V}} = 1, 1\text{V Step}$			24			24	μs

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current (per Amplifier)	No Load	●		54	72 78		54	72 80	μA μA
	Shutdown Current (per Amplifier)	Shutdown, $V_{SHDN} \leq 0.8\text{V}$, LTC6078DD	●		0.3	1				μA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7		5.5	2.7		5.5	V
	Channel Separation	$f_s = 10\text{kHz}$, $R_L = 10\text{k}$			-110			-110		dB
	Shutdown Logic	$\overline{\text{SHDN}}$ High, LTC6078DD $\overline{\text{SHDN}}$ Low, LTC6078DD	● ●	2		0.8	2		0.8	V V
t_{ON}	Turn on Time	$V_{SHDN} = 0.8\text{V}$ to 2V , LTC6078DD			50			50		μs
t_{OFF}	Turn off Time	$V_{SHDN} = 2\text{V}$ to 0.8V , LTC6078DD			2			2		μs
	Leakage of $\overline{\text{SHDN}}$ Pin	$V_{SHDN} = 0\text{V}$, LTC6078DD			0.6					μA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C, I SUFFIXES			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Offset Voltage	LTC6078MS8, LTC6078AMS8, LTC6079GN $V_{CM} = 0.5\text{V}$			± 10	± 30		± 10	± 30	μV
		LTC6078DD, LTC6079DHC $V_{CM} = 0.5\text{V}$			± 10	± 35				μV
		LTC6078AMS8 $V_{CM} = 0.5\text{V}$	●		± 20	± 75		± 25	± 100	μV
		LTC6078MS8 $V_{CM} = 0.5\text{V}$	●		± 25	± 102		± 30	± 140	μV
		LTC6079GN $V_{CM} = 0.5\text{V}$	●		± 30	± 120		± 35	± 170	μV
		LTC6078DD $V_{CM} = 0.5\text{V}$	●		± 30	± 125				μV
		LTC6079DHC $V_{CM} = 0.5\text{V}$	●		± 35	± 155				μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 7)	LTC6078AMS8	●		± 0.2	± 0.7		± 0.2	± 0.7	$\mu\text{V}/^\circ\text{C}$
		LTC6078MS8	●			± 1.1			± 1.1	$\mu\text{V}/^\circ\text{C}$
		LTC6078DD, LTC6079GN	●		± 0.3	± 1.4		± 0.3	± 1.4	$\mu\text{V}/^\circ\text{C}$
		LTC6079DHC	●		± 0.3	± 1.8				$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = V^+/2$			0.2	1		0.2	1	pA
		$V_{CM} = V^+/2$	●		10	50		150	350	pA
I_{OS}	Input Offset Current	$V_{CM} = V^+/2$			0.1			0.1		pA
		$V_{CM} = V^+/2$	●		0.5	25		10	100	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz			1			1		μV_{P-P}
	Input Noise Voltage Density	$f = 1\text{kHz}$			18			18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$			16			16		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density (Note 8)				0.56			0.56		$\text{fA}/\sqrt{\text{Hz}}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{DIFF}	Differential Input Capacitance				10			10		pF
C_{CM}	Common Mode Input Capacitance				18			18		pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	C, I SUFFIXES			H SUFFIX			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common Mode Rejection Ratio	All Packages $V_{\text{CM}} = 0\text{V to } 5\text{V}$	●	91	105	91	105		dB
		LTC6078AMS8 $V_{\text{CM}} = 0\text{V to } 5\text{V}$	●	90	105	90	105		dB
		LTC6078AMS8 $V_{\text{CM}} = 0\text{V to } 3.7\text{V}$	●	94	105	94	105		dB
		LTC6078MS8 $V_{\text{CM}} = 0\text{V to } 5\text{V}$	●	88	100	88	100		dB
		LTC6078MS8 $V_{\text{CM}} = 0\text{V to } 3.7\text{V}$	●	90	105	90	105		dB
		LTC6079GN $V_{\text{CM}} = 0\text{V to } 5\text{V}$	●	86	100	86	100		dB
		LTC6079GN $V_{\text{CM}} = 0\text{V to } 3.7\text{V}$	●	90	105	90	105		dB
		LTC6078DD, LTC6079DHC $V_{\text{CM}} = 0\text{V to } 5\text{V}$	●	86	100				dB
		LTC6078DD, LTC6079DHC $V_{\text{CM}} = 0\text{V to } 3.7\text{V}$	●	90	105				dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.7\text{V to } 5.5\text{V}$	●	100	120				dB
				97		97	120		dB
V_{OUT}	Output Voltage, High (Referred to V^+)	No Load	●		2		2		mV
		$I_{\text{SOURCE}} = 0.5\text{mA}$	●	50	20	55	20		mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	500	200	550	200		mV
	Output Voltage, Low (Referred to V^-)	No Load	●		1		1		mV
		$I_{\text{SINK}} = 0.5\text{mA}$	●		15	40	15	45	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		150	400	150	450	mV
A_{VOL}	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}$, $0.5\text{V} \leq V_{\text{OUT}} \leq 4.5\text{V}$	●	115	130	110	125		dB
I_{SC}	Output Short-Circuit Current	Source	●	14	25	12	25		mA
		Sink	●	14	25	12	25		mA
SR	Slew Rate	$A_V = 1$			0.05		0.05		V/ μs
GBW	Gain-Bandwidth Product ($f_{\text{TEST}} = 10\text{kHz}$)	$R_L = 100\text{k}$	●	420	750	420	750		kHz
				360		320			kHz
Φ_0	Phase Margin	$R_L = 10\text{k}$, $C_L = 200\text{pF}$			66		66		Deg
t_S	Settling Time 0.1%	$A_V = 1$, 1V Step			24		24		μs
I_S	Supply Current (per Amplifier)	No Load	●		55	74	55	74	μA
						82		84	μA
	Shutdown Current (per Amplifier)	Shutdown, $V_{\text{SHDN}} \leq 1.2\text{V}$, LTC6078DD	●		1.5	5	1.5	5	μA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.7	5.5	2.7	5.5		V
	Channel Separation	$f_S = 10\text{kHz}$, $R_L = 10\text{k}$			-110		-110		dB
	Shutdown Logic	SHDN High , LTC6078DD SHDN Low , LTC6078DD	● ●	3.5		3.5		1.2	V V
t_{ON}	Turn on Time	$V_{\text{SHDN}} = 1.2\text{V to } 3.5\text{V}$, LTC6078DD			50		50		μs
t_{OFF}	Turn off Time	$V_{\text{SHDN}} = 1.2\text{V to } 3.5\text{V}$, LTC6078DD			2		2		μs
	Leakage of SHDN Pin	$V_{\text{SHDN}} = 0\text{V}$, LTC6078DD			0.6				μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

Note 3: The LTC6078C/LTC6079C and LTC6078I/LTC6079I are guaranteed functional over the operating temperature range of -40°C to 85°C . The LTC6078H/LTC6079H are guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 4: The LTC6078C/LTC6079C are guaranteed to meet specified

performance from 0°C to 70°C . The LTC6078C/LTC6079C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6078I/LTC6079I are guaranteed to meet specified performance from -40°C to 85°C . The LTC6078H/LTC6079H are guaranteed to meet specified performance from -40°C to 125°C .

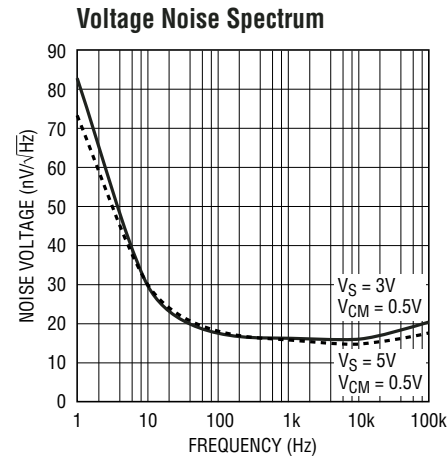
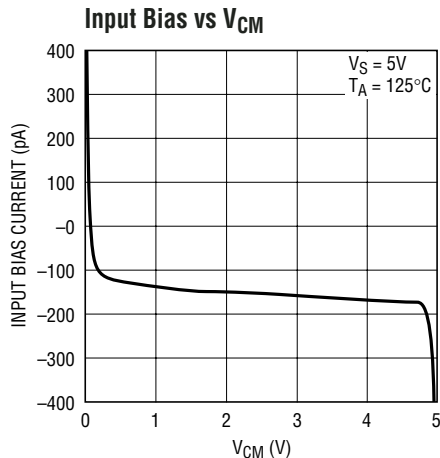
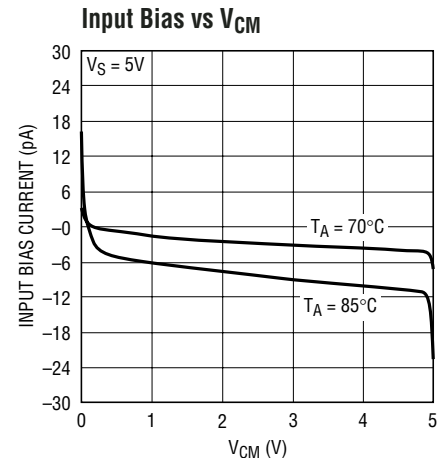
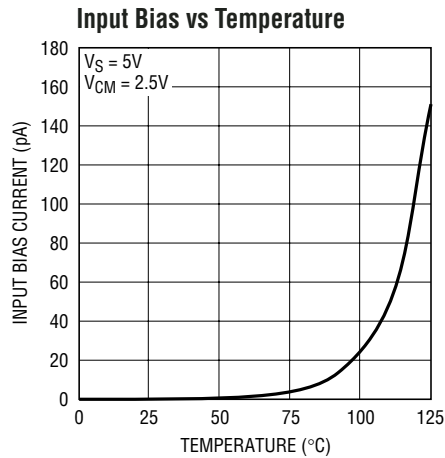
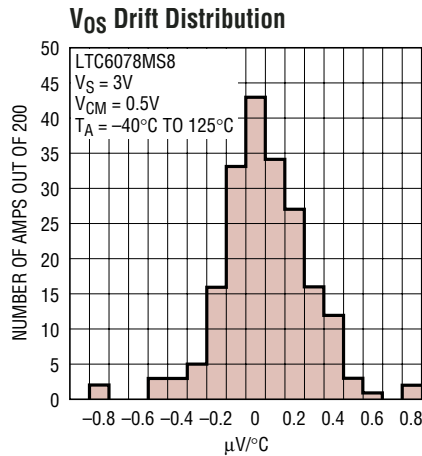
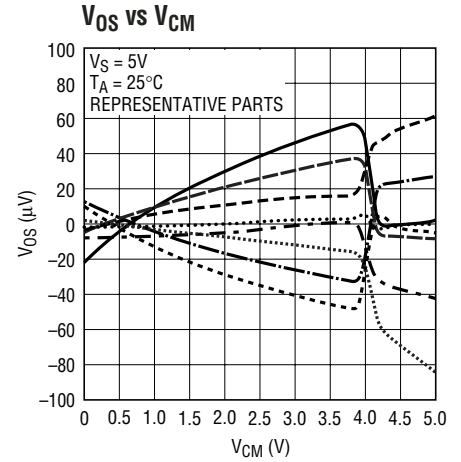
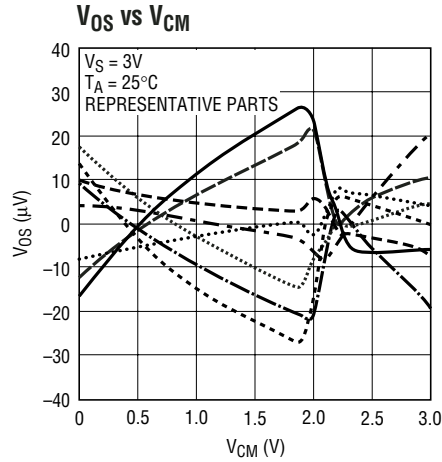
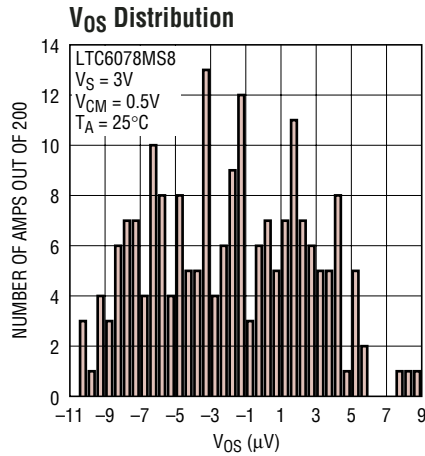
Note 5: V_{OS} and V_{OS} drift are 100% tested at 25°C and 125°C .

Note 6: I_B and I_{OS} are guaranteed by the $V_S = 5\text{V}$ test.

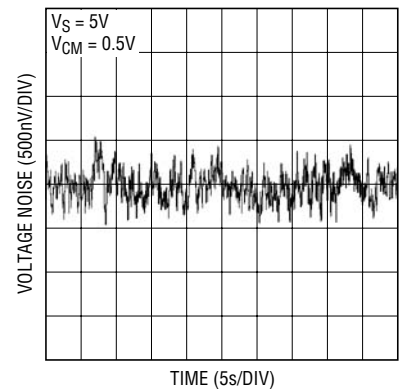
Note 7: V_{OS} drift is guaranteed by the $V_S = 3\text{V}$ test.

Note 8: Current noise is calculated from $i_n = \sqrt{2qI_B}$, where $q = 1.6 \cdot 10^{-19}$ coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

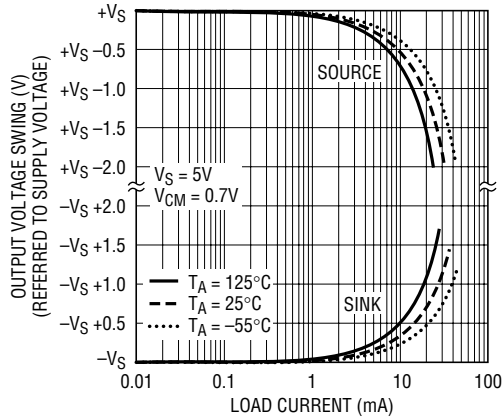


0.1Hz to 10Hz Output Voltage Noise



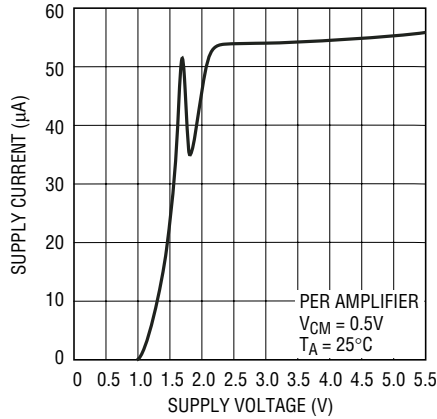
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Current



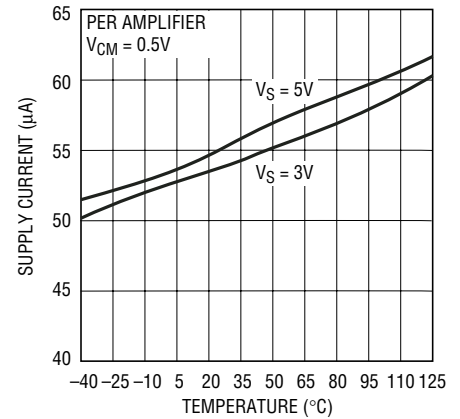
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Supply Current vs Supply Voltage



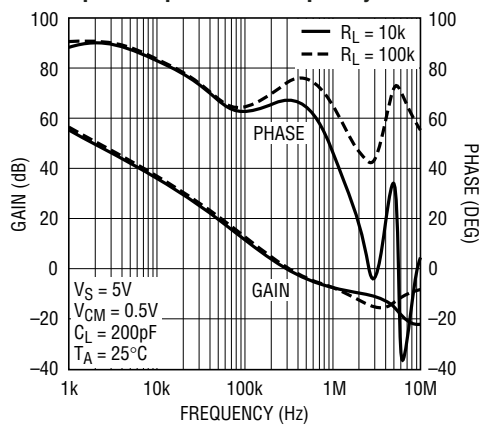
60789 G11

Supply Current vs Temperature



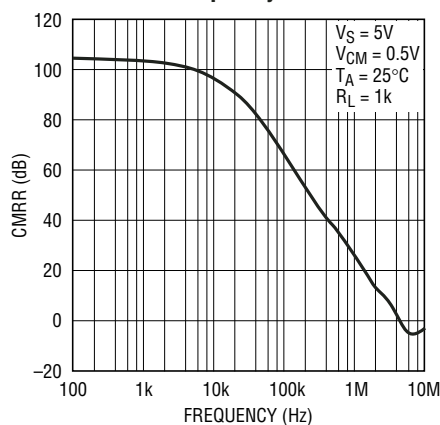
60789 G12

Open Loop Gain vs Frequency



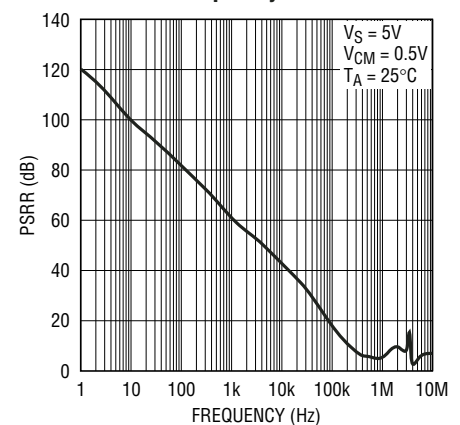
60789 G13

CMRR vs Frequency



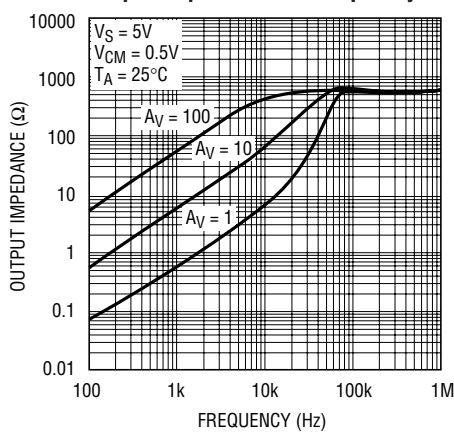
60789 G14

PSRR vs Frequency



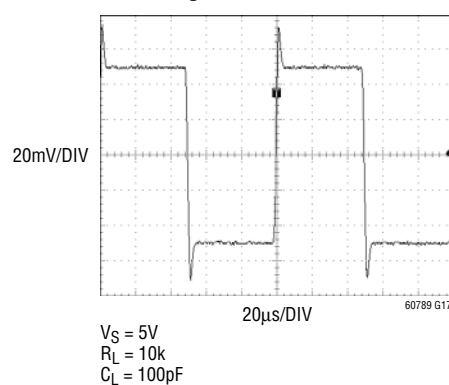
60789 G15

Output Impedance vs Frequency



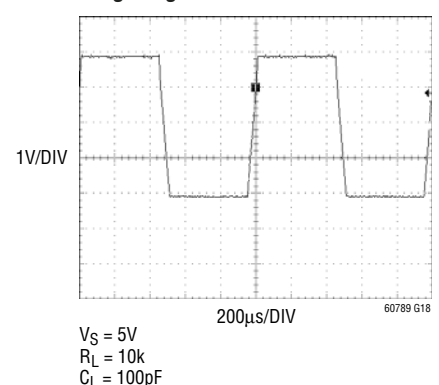
60789 G16

Small Signal Transient



60789 G17

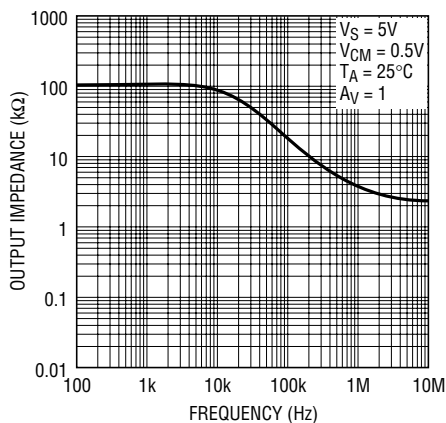
Large Signal Transient



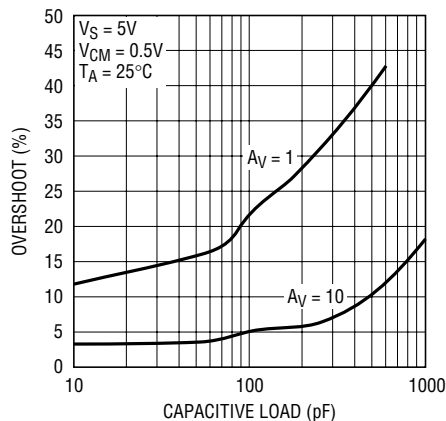
60789 G18

TYPICAL PERFORMANCE CHARACTERISTICS

Disabled Output Impedance vs Frequency

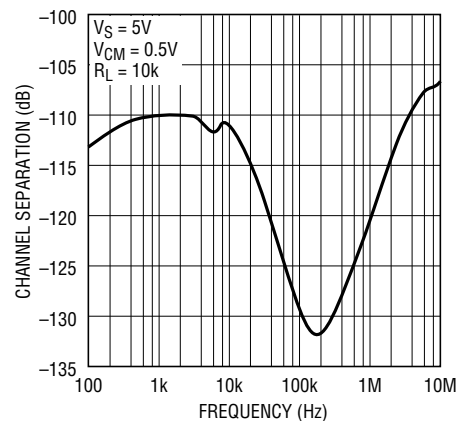


60789 G19

Overshoot vs C_L 

60789 G20

Channel Separation vs Frequency



60789 G21

PIN FUNCTIONS

OUT: Amplifier Output**-IN:** Inverting Input**+IN:** Noninverting Input**V+:** Positive Supply**V-:** Negative Supply

SHDN_A: Shutdown Pin of Amplifier A, active low and only valid for LTC6078DD. An internal current source pulls the pin to V^+ when floating.

SHDN_B: Shutdown Pin of Amplifier B, active low and only valid for LTC6078DD. An internal current source pulls the pin to V^+ when floating.

NC: Not internally connected.

Exposed Pad: Connected to V^- .

APPLICATIONS INFORMATION

Preserving Input Precision

Preserving input accuracy of the LTC6078/LTC6079 requires that the application circuit and PC board layout do not introduce errors comparable or greater than the $10\mu\text{V}$ typical offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of 10's of microvolts so the connections to the input leads should be short, close together and away from heat dissipating components. Air current across the board can also generate temperature differentials.

The extremely low input bias currents (0.2pA typical) allow high accuracy to be maintained with high impedance sources and feedback resistors. Leakage currents on the PC board can be higher than the input bias current. For example, $10\text{G}\Omega$ of leakage between a 5V supply lead and an input lead will generate 500pA ! Surround the input leads with a guard ring driven to the same potential as the input common mode to avoid excessive leakage in high impedance applications.

Input Clamps

Large differential voltages across the inputs over very long time periods can impact the precisely trimmed input offset voltage of the LTC6078/LTC6079. As an example, a 2V differential voltage between the inputs over a period of 100 hours can shift the input offset voltage by tens of microvolts. If the amplifier is to be subjected to large differential input voltages, adding back-to-back diodes between the two inputs will minimize this shift and retain the DC precision. If necessary, current-limiting series resistors can be added in front of the diodes, as shown in Figure 1. These diodes are not necessary for normal closed loop applications.

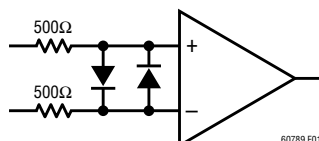


Figure 1. Op Amp with Input Voltage Clamp

Capacitive Load

LTC6078/LTC6079 can drive capacitive load up to 200pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

SHDN Pins

Pins 5 and 6 are used for power shutdown on the LTC6078 in the DD package. If they are floating, internal current sources pull Pins 5 and 6 to $V+$ and the amplifiers operate normally. In shutdown, the amplifier output is high impedance, and each amplifier draws less than $2\mu\text{A}$ current.

When the chip is turned on, the supply current per amplifier is about $35\mu\text{A}$ larger than its normal values for $50\mu\text{s}$.

Rail-to-Rail Input

The input stage of LTC6078/LTC6079 combines both PMOS and NMOS differential pairs, extending its input common mode voltage range to both positive and negative supply voltages. At high input common mode range, the NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3V and 0.9V below the positive supply.

Thermal Hysteresis

Figure 2 shows the input offset hysteresis of LTC6078MS8 for 3 thermal cycles from -45°C to 90°C . The typical offset shift after the 3 cycles is only $1\mu\text{V}$.

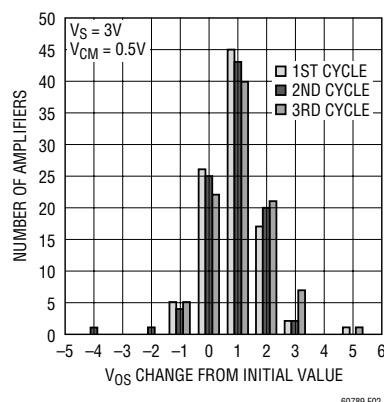


Figure 2. V_{OS} Thermal Hysteresis of LTC6078MS8

APPLICATIONS INFORMATION

PC Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the V_{OS} and V_{OS} drift to shift. The DD and DHC packages are more sensitive to stress. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should always be mounted so that the leads absorb the stress and not the package. The package is generally aligned with the leads parallel to the long side of the PC board.

The most effective technique to relieve the PC board stress is to cut slots in the board around the op amp. These slots can be cut on three sides of the IC and the leads can exit on

the fourth side. Figure 3 shows the layout of a LTC6078DD with slots at three sides.

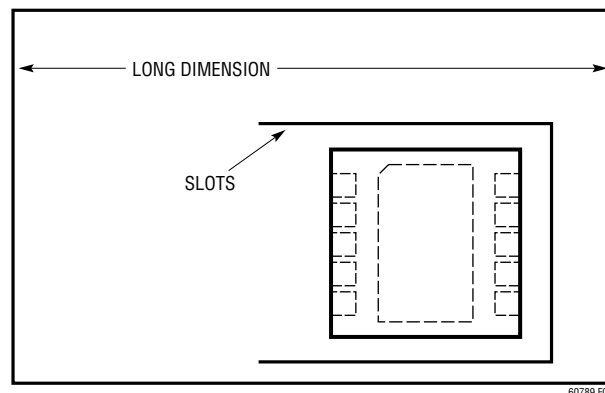
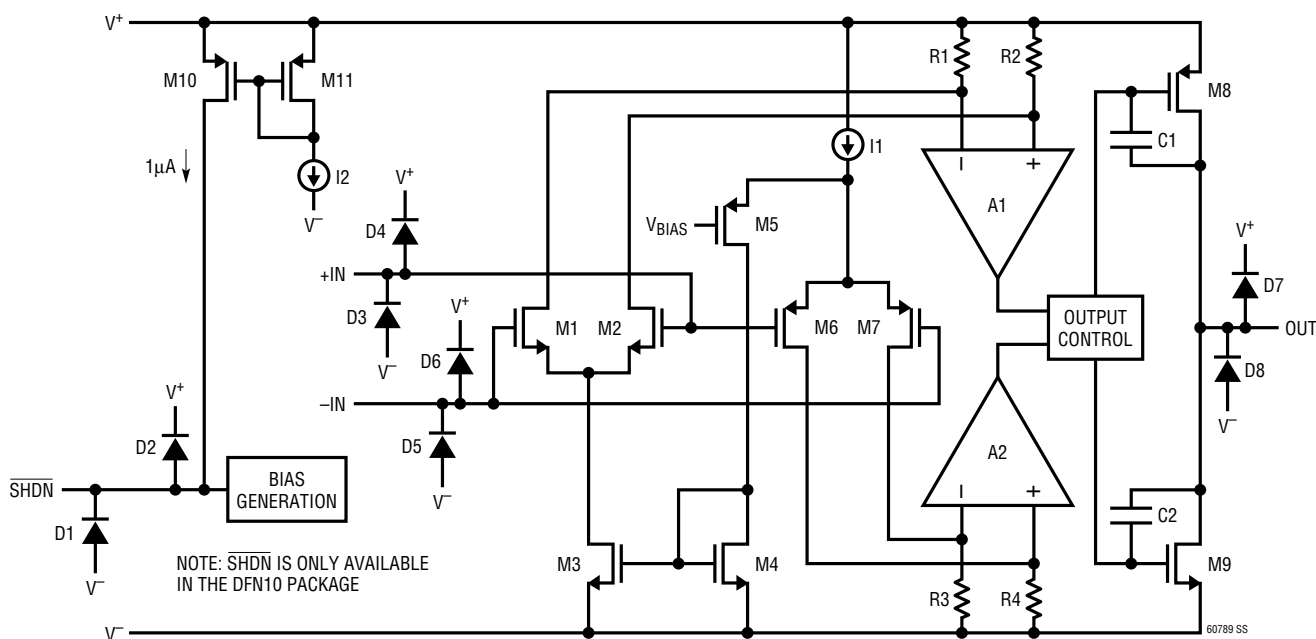


Figure 3. Vertical Orientation of LTC6078DD with Slots

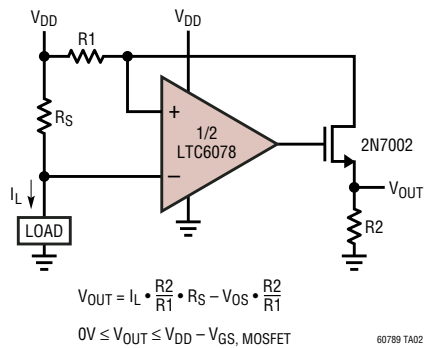
SIMPLIFIED SCHEMATIC



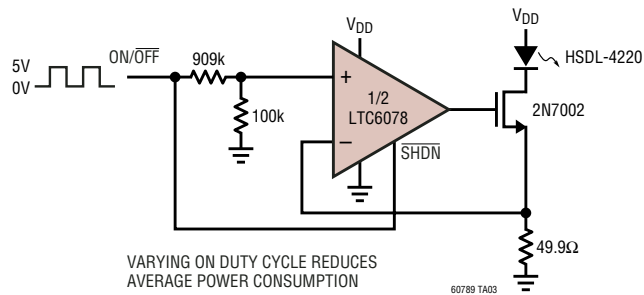
Simplified Schematic of the Amplifier

TYPICAL APPLICATIONS

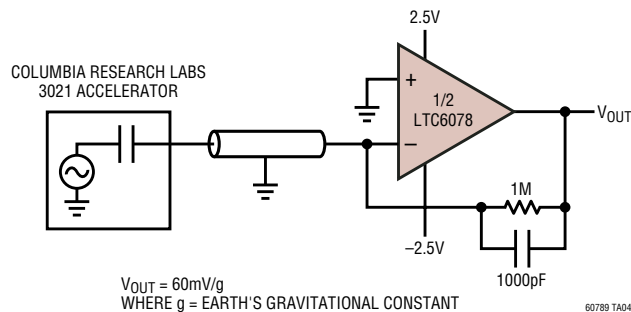
2.7V High Side Current Sense



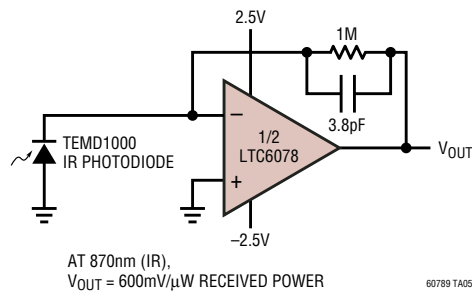
Low Average Power IR LED Driver



Accelerometer Signal Conditioner

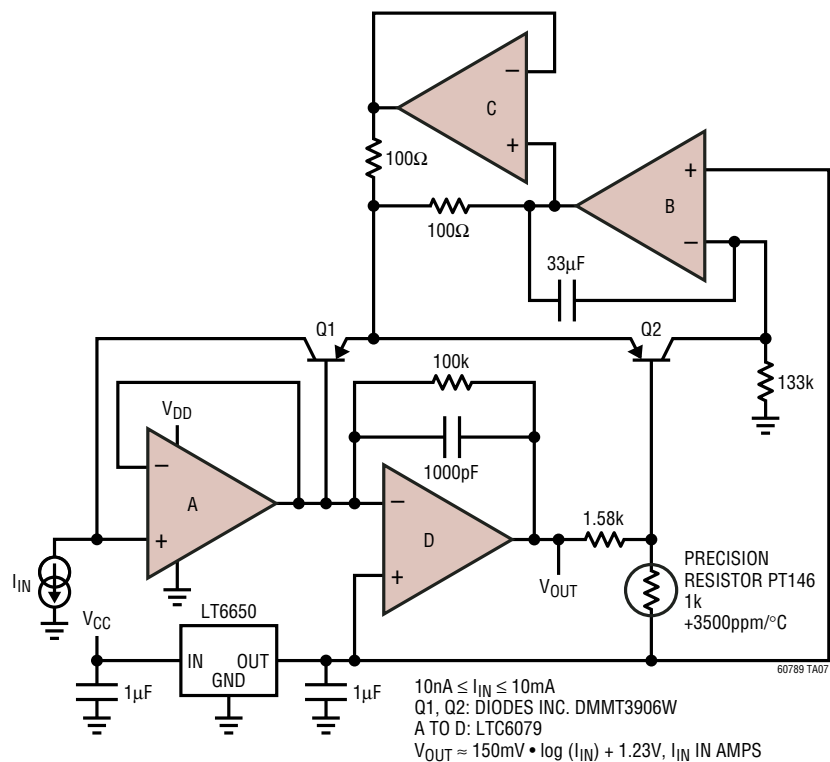


Photodiode Amplifier

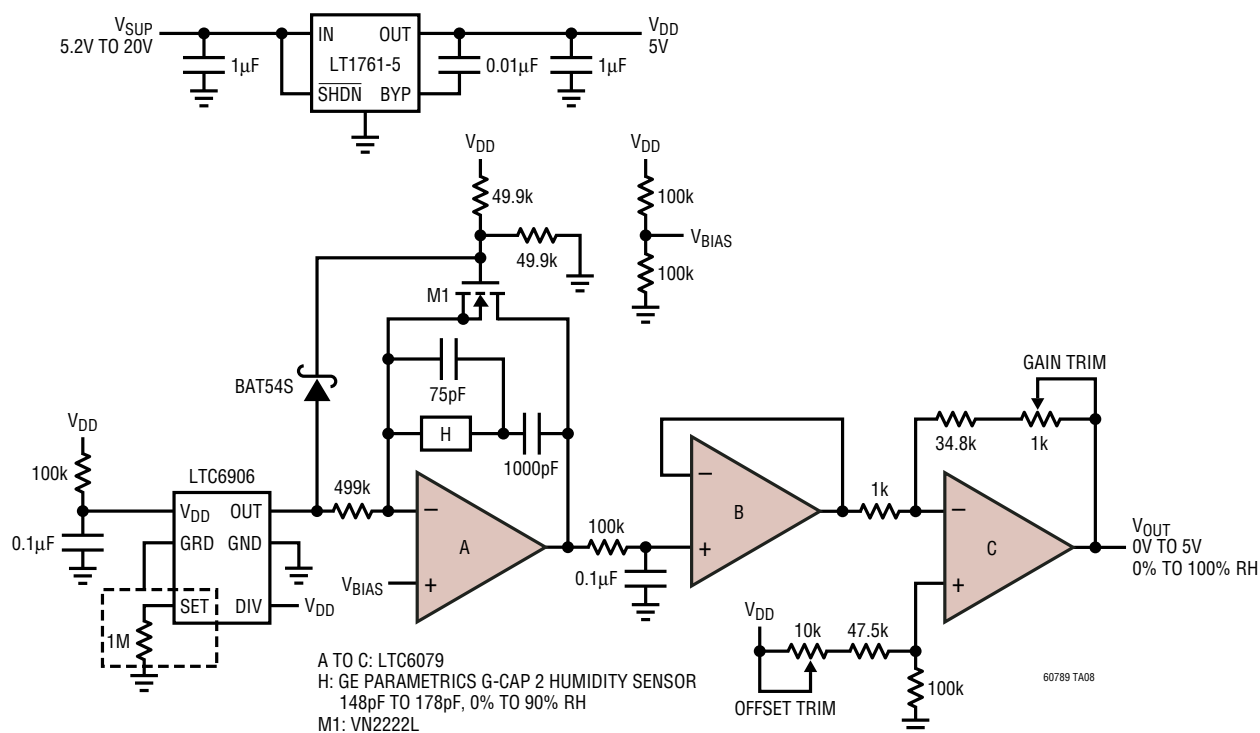


TYPICAL APPLICATIONS

6 Decade Current Log Amplifier



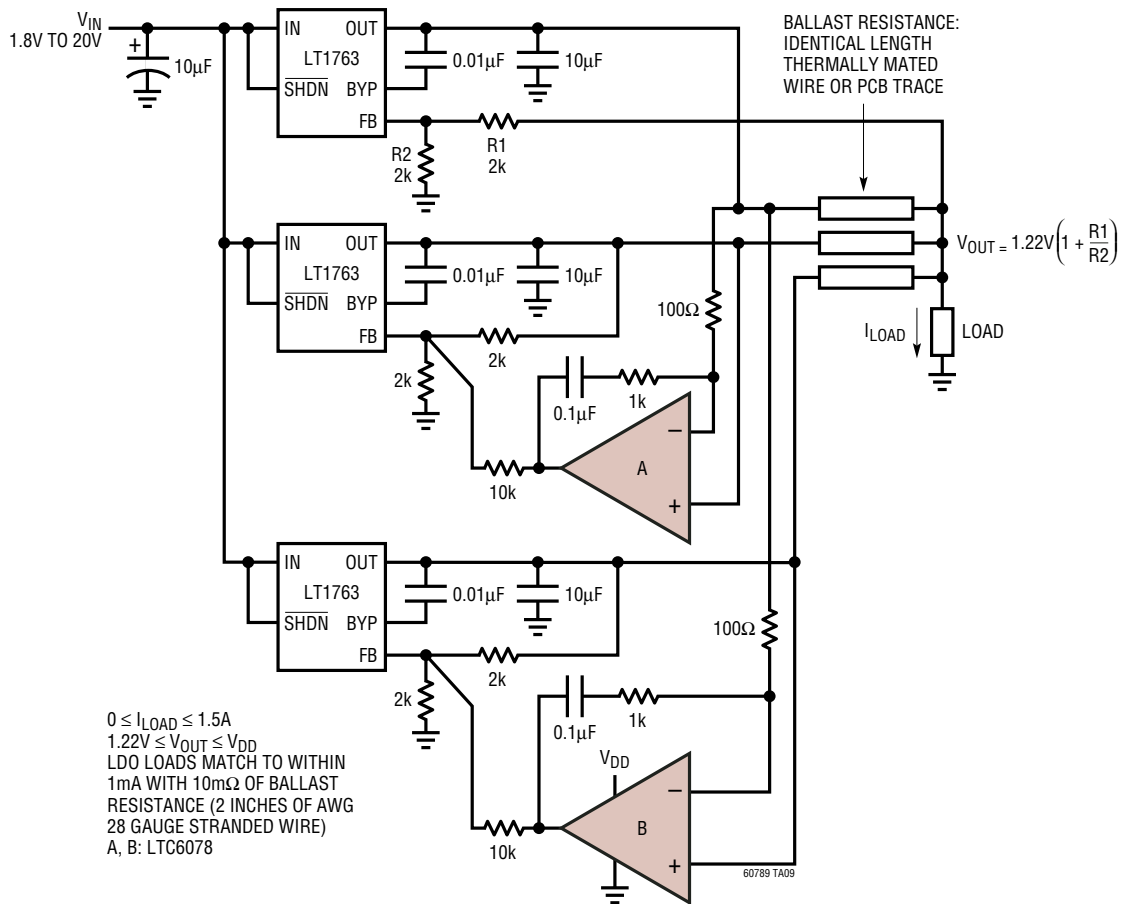
Humidity Sensor Signal Conditioner



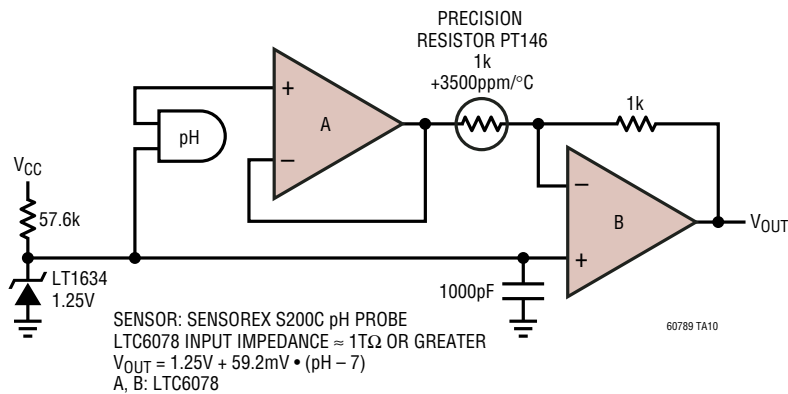
60789fa

TYPICAL APPLICATIONS

LDO Load Balancing

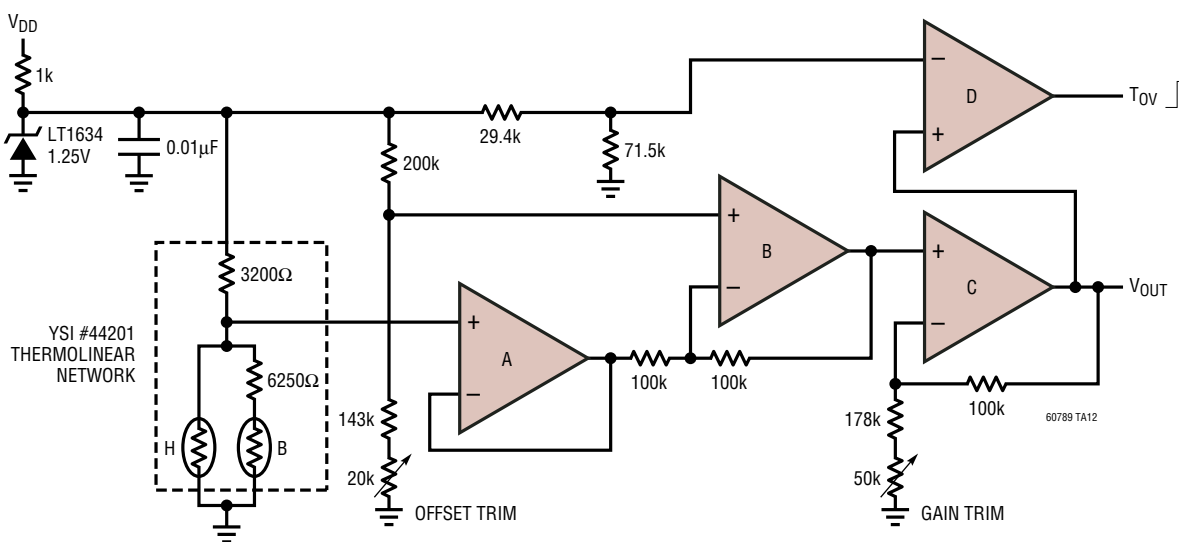


pH Probe Amplifier



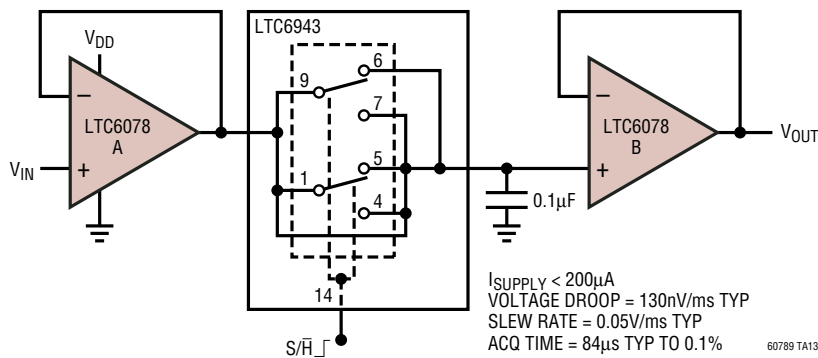
TYPICAL APPLICATIONS

Thermistor Amplifier with Overtemperature Alarm



A TO D: LTC6079, $V_{DD} = 2.7V$ TO $5.5V$, $V_{SS} = GND$
 $V_{OUT} = 0 \rightarrow 1V$ FOR $0^{\circ}C$ TO $100^{\circ}C$, LINEAR
 $T_{OV} \rightarrow HIGH$ WHEN $T \geq 90^{\circ}C$

Precision Sample-and-Hold



$I_{OUT} = \frac{V_{IN}}{R_{SET}}$
 $I_{ERROR} < 0.1\% \text{ AT } I_{OUT} = 1\mu A$

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{IN}$$

NOTCH DEPTH = -60dB AT 60Hz, RTI

60789 TA15

Top view of the package showing dimensions and tolerances:

- Overall width: 3.50 ± 0.05
- Distance from top edge to centerline: 2.15 ± 0.05
- Distance from centerline to top edge of package outline: 1.65 ± 0.05 (2 SIDES)
- Distance from centerline to bottom edge of package outline: 1.65 ± 0.05 (2 SIDES)
- Distance from centerline to edge of package outline: 0.25 ± 0.05
- Distance from centerline to edge of package outline: 0.50 BSC
- Distance from centerline to edge of package outline: 2.38 ± 0.05 (2 SIDES)
- Distance from centerline to edge of package outline: 0.675 ± 0.05
- Package outline is indicated by a dashed line.

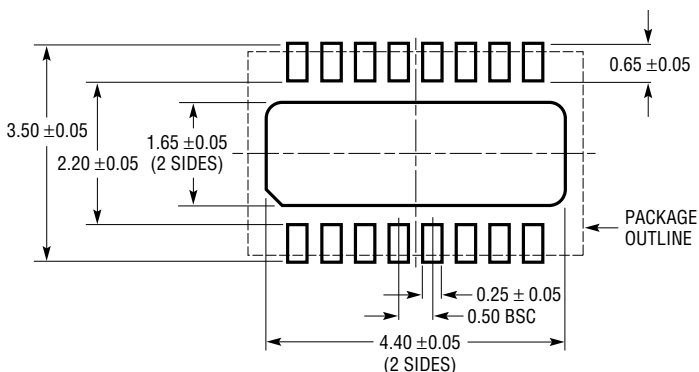
The image contains two mechanical drawings of the 0805 package:

- Top View:** A square package with a side length of 3.00 ± 0.10 (4 SIDES). A circular feature is labeled "PIN 1 TOP MARK (SEE NOTE 6)".
- Bottom View—EXPOSED PAD:** Shows the underside of the package with dimensions:
 - Overall width: 0.75 ± 0.05
 - Overall length: $0.00 - 0.05$
 - Distance from left edge to first pad: 0.200 REF
 - Distance between pads: 0.25 ± 0.05
 - Distance from last pad to right edge: 0.50 BSC
 - Radius of curved sections: $R = 0.115$ TYP
 - Distance from top edge to first curved section: 1.65 ± 0.10 (2 SIDES)
 - Distance from bottom edge to first curved section: 0.38 ± 0.10
 - Distance from left edge to first curved section: 2.38 ± 0.10 (2 SIDES)
 - Reference to standard: (0805) DFN 1103

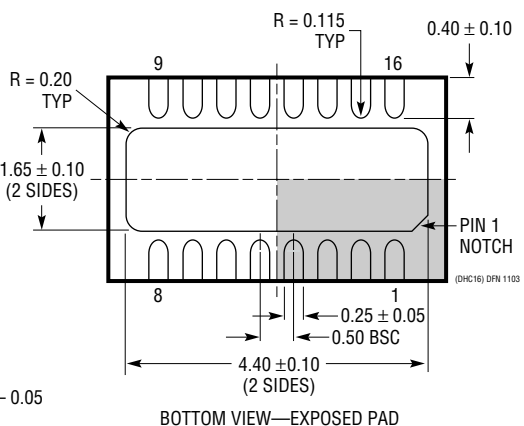
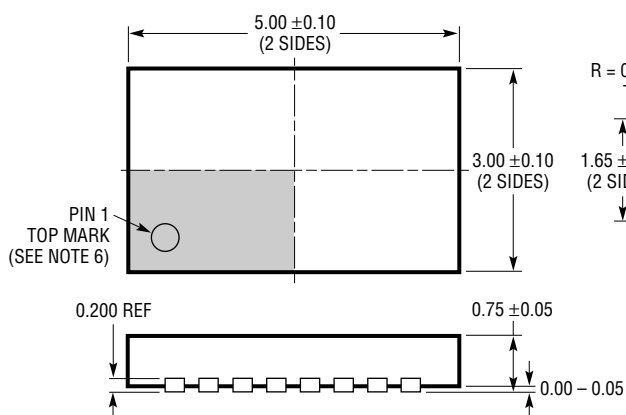
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
 (Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



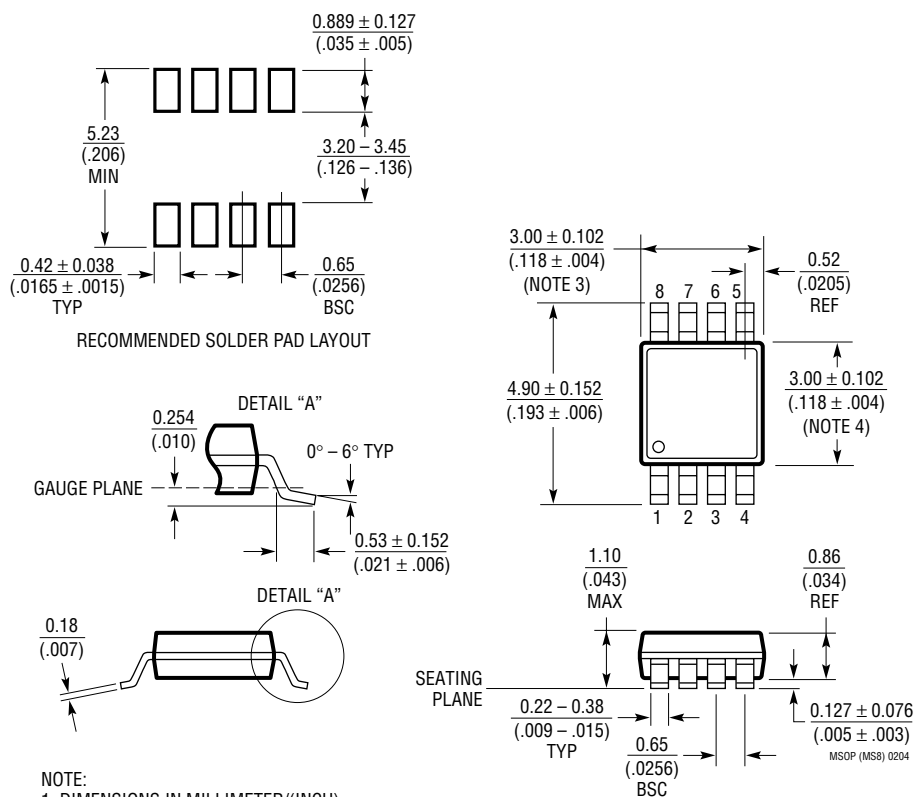
NOTE:

1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660)

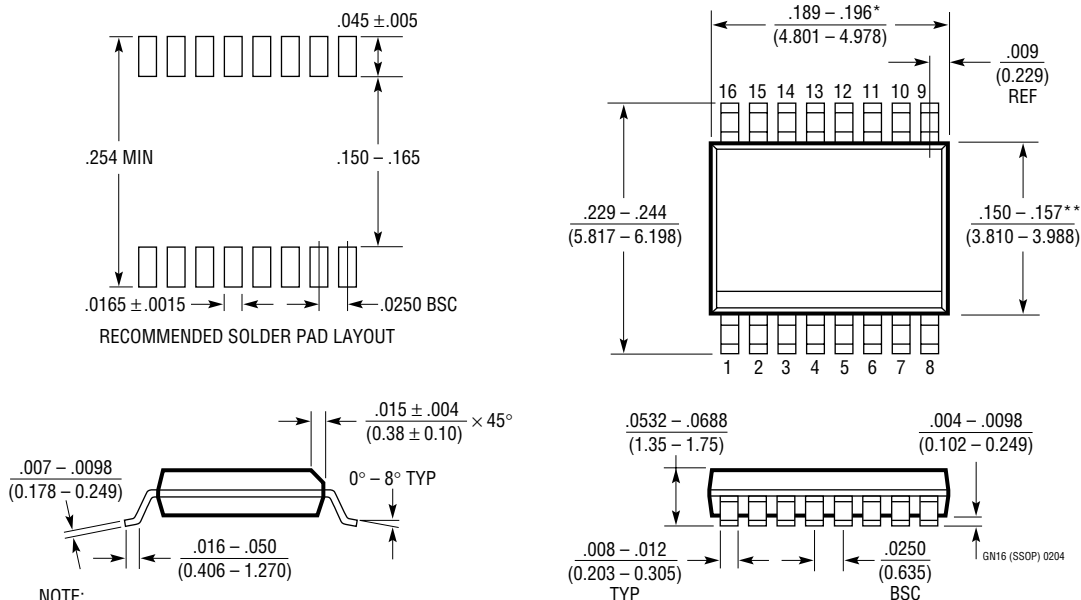


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

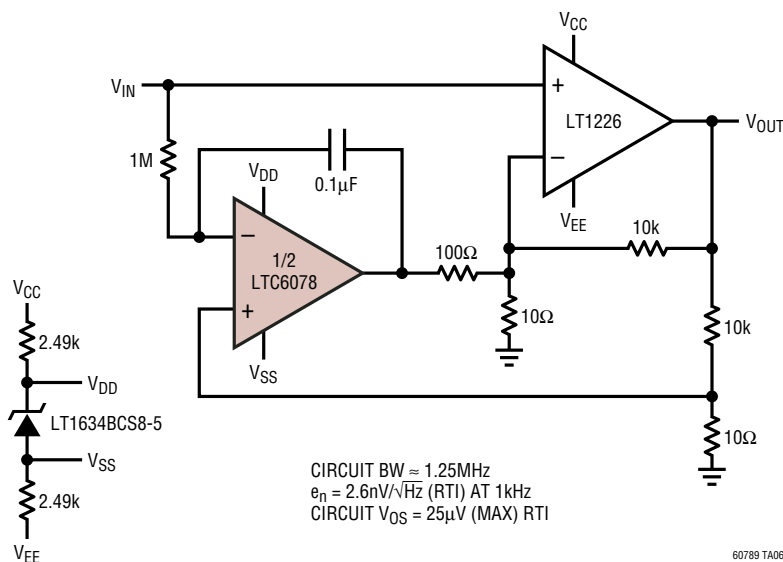
GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
 2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 3. DRAWING NOT TO SCALE
- *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

DC Accurate Composite Amplifier, Gain of 1000



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2051/LTC2052	Dual/Quad Zero-Drift Op Amps	3μV V _{OS} , 30nV/°C V _{OS} Drift
LT6011/LT6012	Dual/Quad Precision Op Amps	60μV V _{OS} , I _B = 300pA, I _S = 135μA