# DSC1104 | DSC1124

discera

## Low-Jitter Precision HCSL Oscillator

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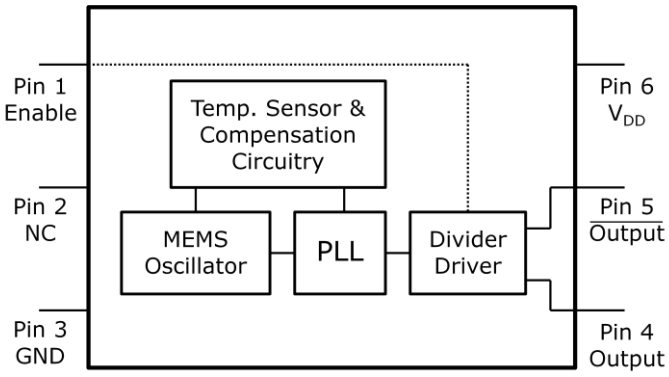
## General Description

The DSC1104 & DSC1124 series of high performance oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1104 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC1124, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 $mm^2$, and are "drop-in" replacements for standard 6-pin HCSL quartz crystal oscillators.

## Block Diagram




## Output Enable Modes

| EN Pin | DSC1104 | DSC1124 |
|---|---|---|
| High | Outputs Active | Outputs Active |
| NC | Outputs Active | Outputs Active |
| Low | Standby | Outputs Disabled |

## Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Short Lead Time: 2 Weeks**
- **Wide Freq. Range: 2.3 to 460 MHz**
- **Small Industry Standard Footprints**
  - 2.5x2.0, 3.2x2.5, 5.0x3.2, & 7.0x5.0 mm
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Low Current Consumption**
- **Supply Range of 2.25 to 3.6 V**
- **Standby & Output Enable Function**
- **Lead Free & RoHS Compliant**
- **LVPECL & LVDS Versions Available**

## Applications

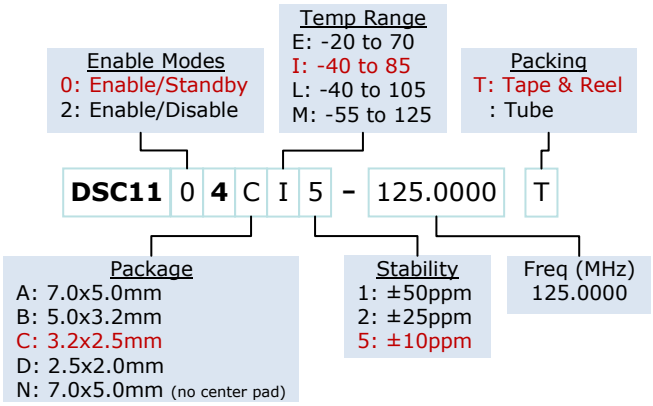
- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express: Gen 1 & Gen 2**
- **DisplayPort**

## Absolute Maximum Ratings

| Item | Min | Max | Unit | Condition |
|---|---|---|---|---|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | $V_{DD}$+0.3 | V | |
| Junction Temp | - | +150 | °C | |
| Storage Temp | -55 | +150 | °C | |
| Soldering Temp | - | +260 | °C | 40sec max. |
| ESD<br>HBM<br>MM<br>CDM | - | <br>4000<br>400<br>1500 | V | |

Note: 1000+ years of data retention on internal memory

## Ordering Code

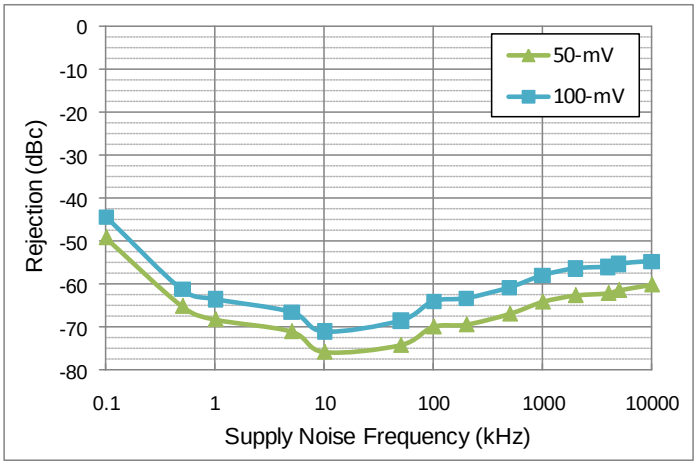



## Specifications

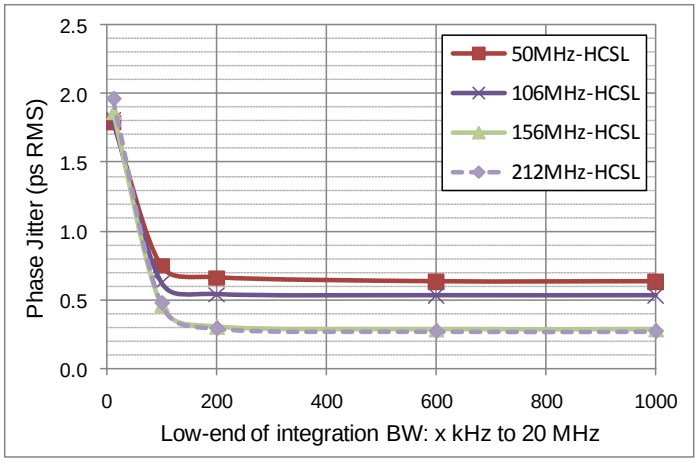
| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage[1] | $V_{DD}$ | | 2.25 | | 3.6 | V |
| Supply Current | $I_{DD}$ | EN pin low – outputs are disabled<br>DSC1104<br>DSC1124 | | <br>20 | <br>0.095<br>22 | mA |
| Frequency Stability | Δf | Includes frequency variations due to initial tolerance, temp. and power supply voltage | | | ±10<br>±25<br>±50 | ppm |
| Aging | Δf | 1 year @25°C | | | ±5 | ppm |
| Startup Time[2] | $t_{SU}$ | T=25°C | | | 5 | ms |
| Input Logic Levels<br>Input logic high<br>Input logic low | <br>$V_{IH}$<br>$V_{IL}$ | | <br>0.75x$V_{DD}$<br>- | | <br>-<br>0.25x$V_{DD}$ | V |
| Output Disable Time[3] | $t_{DA}$ | | | | 5 | ns |
| Output Enable Time | $t_{EN}$ | DSC1104<br>DSC1124 | | | 5<br>20 | ms<br>ns |
| Enable Pull-Up Resistor[4] | | Pull-up resistor exist | | 40 | | kΩ |
| **HCSL Outputs** | | | | | | |
| Supply Current | $I_{DD}$ | Output Enabled, $R_L$=50Ω | | 40 | 42 | mA |
| Output Logic Levels<br>Output logic high<br>Output logic low | <br>$V_{OH}$<br>$V_{OL}$ | $R_L$=50Ω | <br>0.725<br>- | | <br>-<br>0.1 | V |
| Pk to Pk Output Swing | | Single-Ended | | 750 | | mV |
| Output Transition time[3]<br>Rise Time<br>Fall Time | <br>$t_R$<br>$t_F$ | 20% to 80%<br>$R_L$=50Ω, $C_L$= 2pF | 200 | | 400 | ps |
| Frequency | $f_0$ | Single Frequency | 2.3 | | 460 | MHz |
| Output Duty Cycle | SYM | Differential | 48 | | 52 | % |
| Period Jitter | $J_{PER}$ | | | 2.5 | | $ps_{RMS}$ |
| Integrated Phase Noise | $J_{PH}$ | 200kHz to 20MHz @156.25MHz<br>100kHz to 20MHz @156.25MHz<br>12kHz to 20MHz @156.25MHz | | 0.25<br>0.37<br>1.7 | <br><br>2 | $ps_{RMS}$ |

Notes:
1. Pin 6 $V_{DD}$ should be filtered with 0.1uf capacitor.
2. $t_{su}$ is time to 100ppm of output frequency after $V_{DD}$ is applied and outputs are enabled.
3. Output Waveform and Test Circuit figures below define the parameters.
4. Output is enabled if pad is floated or not connected.

## Nominal Performance Parameters (Unless specified otherwise: T=25° C, $V_{DD}$=3.3 V)

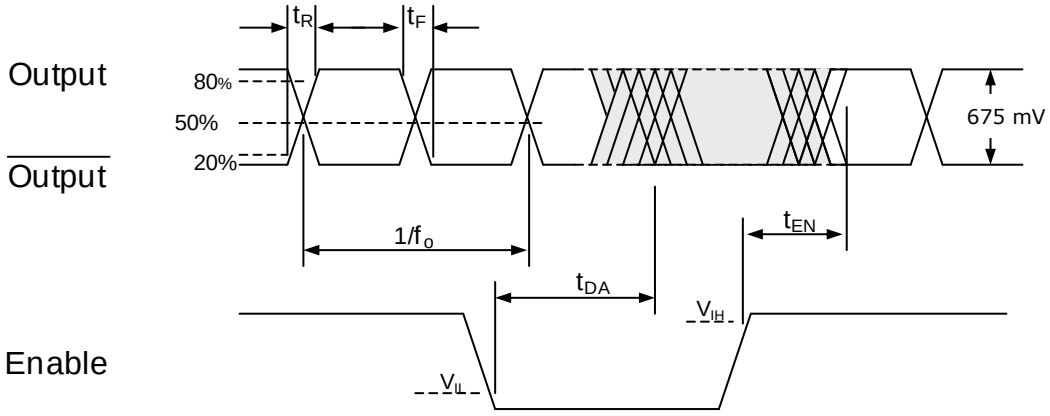



Power supply rejection ratio

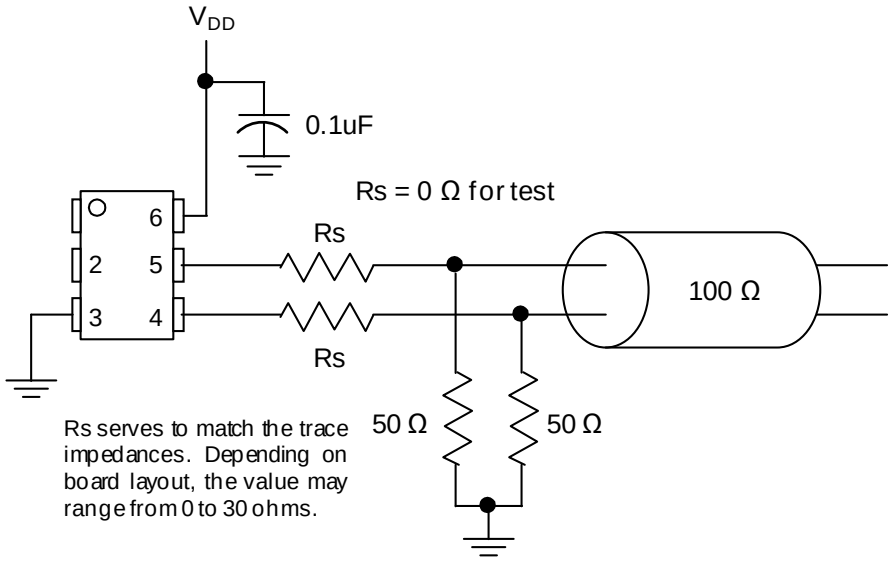



Phase jitter (integrated phase noise)

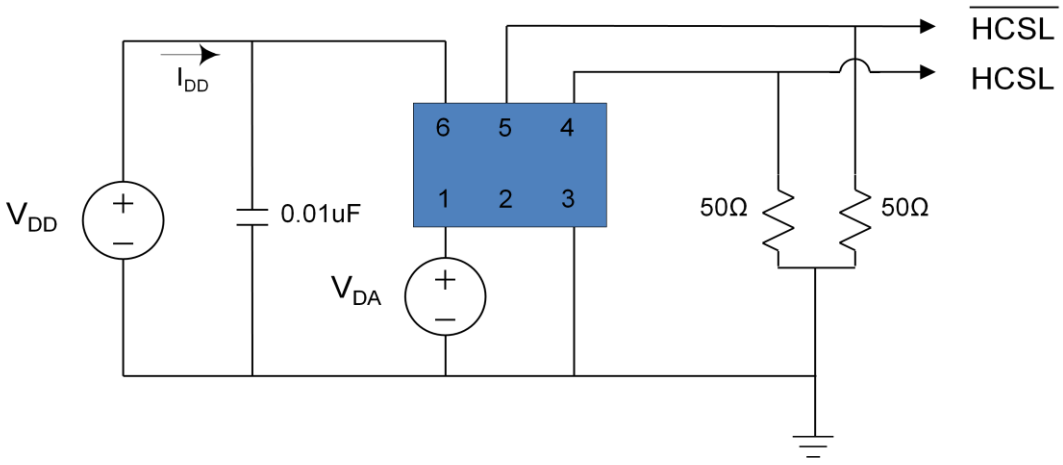
## Output Waveform



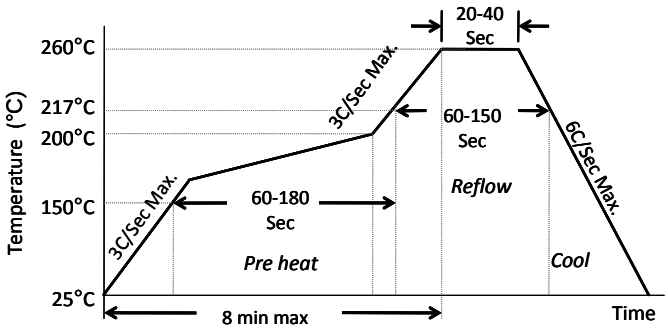

## Typical Termination Scheme



## Test Circuit



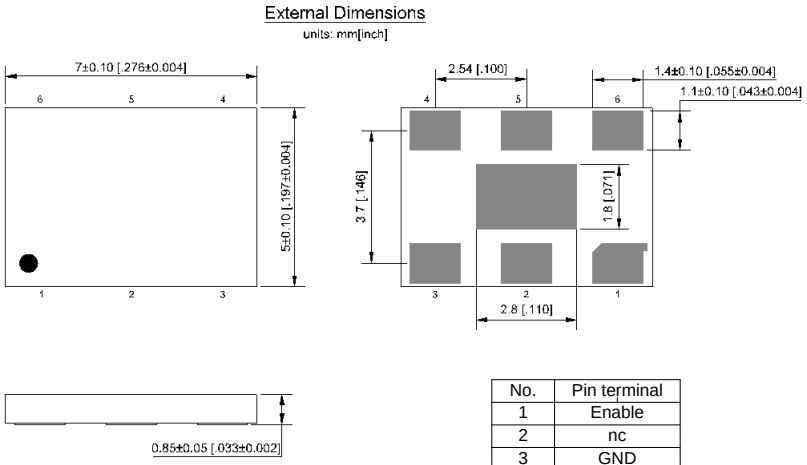

## Solder Reflow Profile



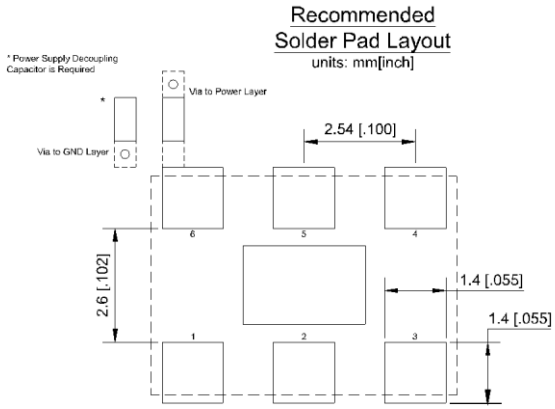

| MSL 1 @ 260°C refer to JSTD-020C | |
|---|---|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/Sec Max. |
| Preheat Time 150°C to 200°C | 60-180 Sec |
| Time maintained above 217°C | 60-150 Sec |
| Peak Temperature | 255-260°C |
| Time within 5°C of actual Peak | 20-40 Sec |
| Ramp-Down Rate | 6°C/Sec Max. |
| Time 25°C to Peak Temperature | 8 min Max. |

## Package Dimensions

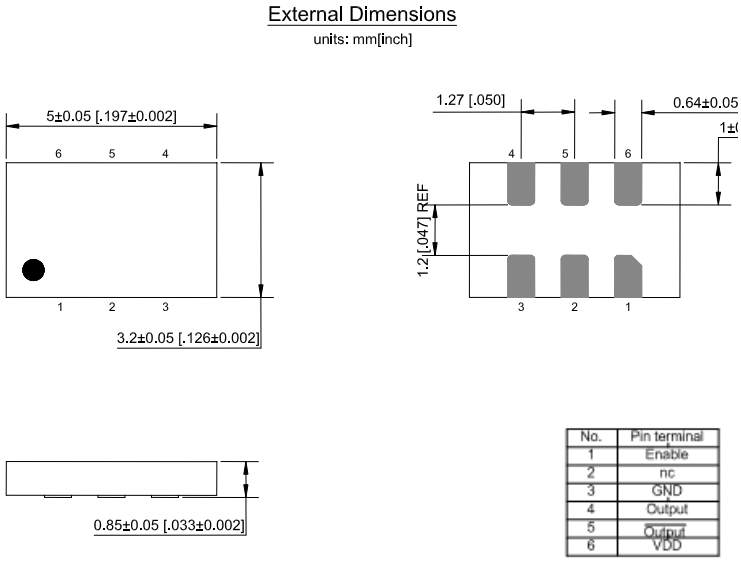
### 7.0 x 5.0 mm Plastic Package



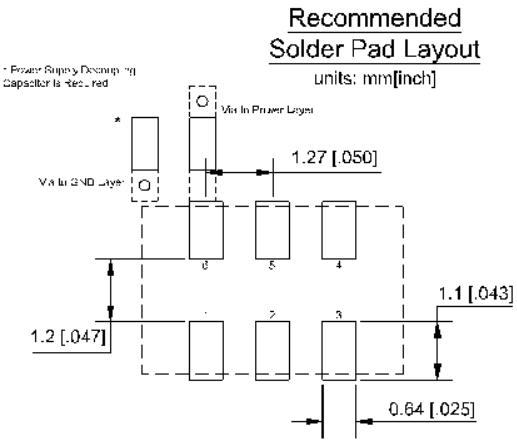

| No. | Pin terminal |
|---|---|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | $\overline{\text{Output}}$ |
| 6 | VDD |




### 5.0 x 3.2 mm Plastic Package



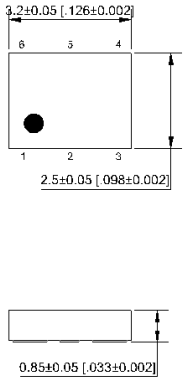

| No. | Pin terminal |
|---|---|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | $\overline{\text{Output}}$ |
| 6 | VDD |

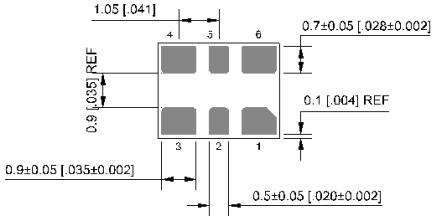


## 3.2 x 2.5 mm Plastic Package

External Dimensions

units: mm[inch]

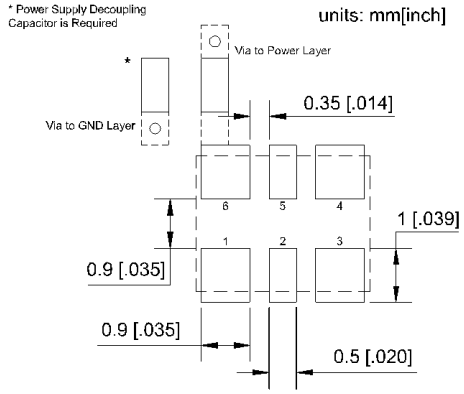


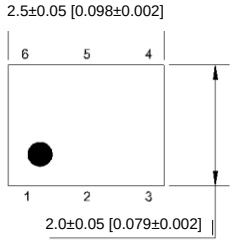

| No. | Pin terminal |
|---|---|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | $\overline{\text{Output}}$ |
| 6 | VDD |

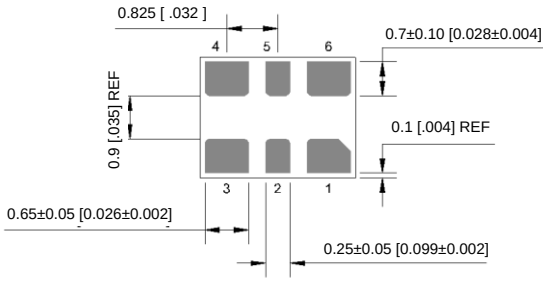
Recommended Solder Pad Layout

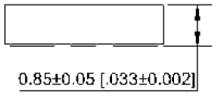
units: mm[inch]




## 2.5 x 2.0 mm Plastic Package



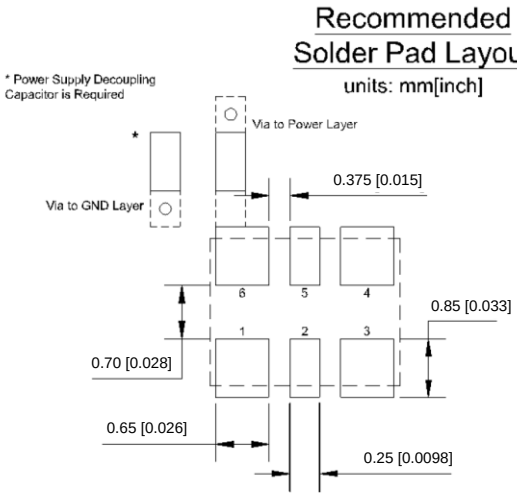



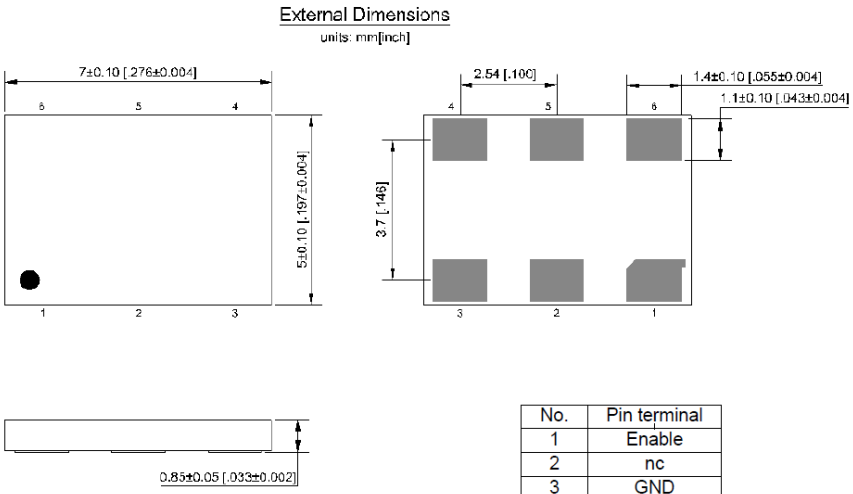

| No. | Pin terminal |
|---|---|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | $\overline{\text{Output}}$ |
| 6 | VDD |

Recommended Solder Pad Layout

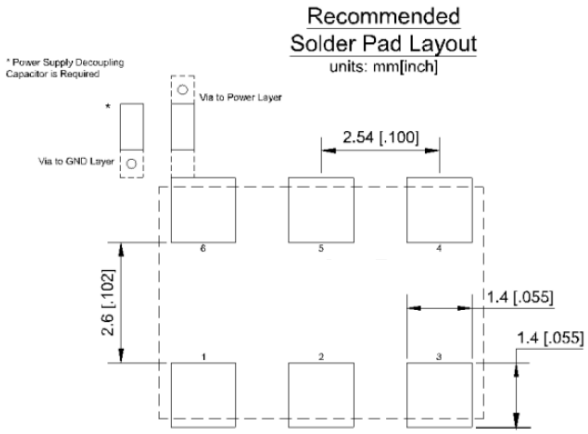
units: mm[inch]



## 7.0 x 5.0 mm Plastic Package




| No. | Pin terminal |
|---|---|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | $\overline{\text{Output}}$ |
| 6 | VDD |

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