

RDS / RBDS decoder

BU1923 / BU1923F

The BU1923 and BU1923F are RDS / RBDS decoders that employ a digital PLL and have a built-in anti-aliasing filter and an eight-stage BPF (switched-capacitor filter). Linear CMOS circuitry is used for low power consumption.

●Applications

RDS / RBDS compatible FM receivers for American and European markets, car stereos, high-fidelity stereo systems and components, and FM pagers.

●Features

- 1) Low current.
- 2) Two-stage anti-aliasing filter (LPF).
- 3) 57kHz band-pass filter.
- 4) DSB demodulation (digital PLL).
- 5) Quality indication output for demodulated data.

●Absolute maximum ratings (Ta = 25°C)

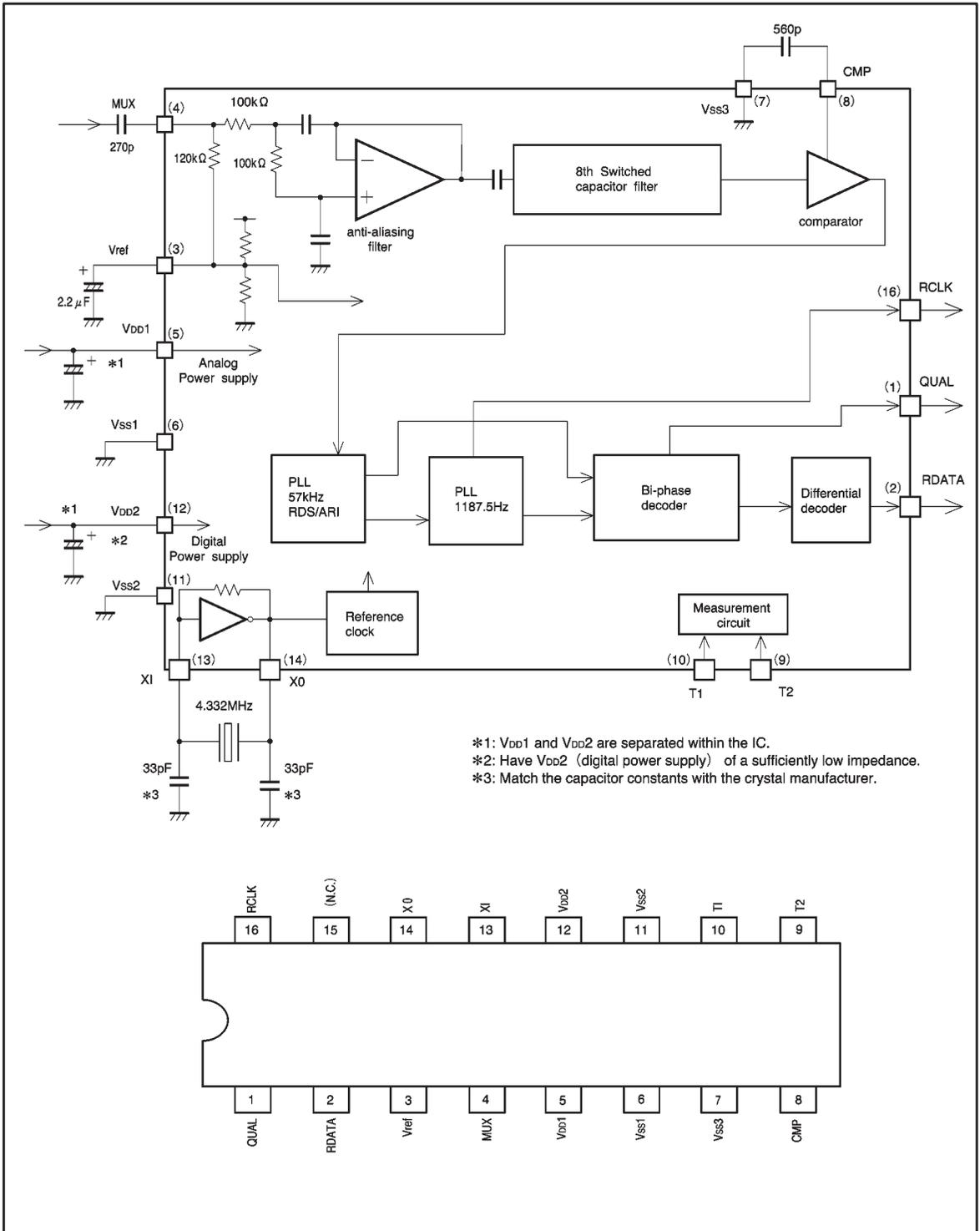
| Parameter | Symbol | Limits | Unit | Conditions |
|------------------------|------------------|---------------------------|------|-----------------------------------|
| Power supply voltage | V _{DD} | -0.3~+7.0 | V | V _{DD1} V _{DD2} |
| Maximum input voltage | V _{MAX} | -0.3~V _{DD} +0.3 | V | All input pins |
| Maximum output voltage | I _{MAX} | ±4.0 | mA | All output pins |
| Power dissipation | P _d | 350* | mW | — |
| Operating temperature | T _{opr} | -40~+85 | °C | — |
| Storage temperature | T _{stg} | -55~+125 | °C | — |

*Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|------------------|------|------|------|------|
| Power supply voltage | V _{DD1} | 4.5 | — | 5.5 | V |
| | V _{DD2} | 4.5 | — | 5.5 | V |

● Block diagram

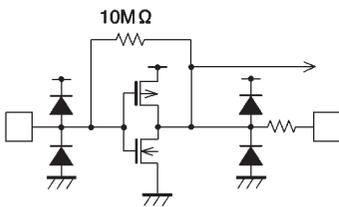


● Pin descriptions

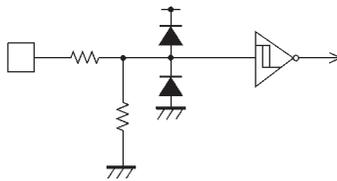
| Pin No. | Symbol | Pin name | Function | Input/output type |
|---------|------------------|----------------------|--|-------------------|
| 1 | QUAL | Demodulator quality | Good data: High, bad data: Low | Type C |
| 2 | RDATA | Demodulator data | Refer to output data timing | — |
| 3 | Vref | Reference voltage | 1/2 V _{DD1} (refer to input/output circuits) | Type E |
| 4 | MUX | Input | Composite signal input (refer to input/output circuits) | Type D |
| 5 | V _{DD1} | Analog power supply | 4.5V to 5.5V | — |
| 6 | V _{SS1} | | | |
| 7 | CMP | Comparator input | C-junction (refer to input/output circuits) | Type D |
| 8 | V _{SS3} | GND | — | — |
| 9 | T2 | Test input | Open or connected to ground | Type B |
| 10 | T1 | | | |
| 11 | V _{DD2} | Digital power supply | 4.5V to 5.5V | — |
| 12 | V _{SS2} | | | |
| 13 | XI | Crystal oscillator | Connects to 4.332MHz oscillator (refer to input/output circuits) | Type A |
| 14 | XO | | | |
| 15 | (N.C.) | — | — | — |
| 16 | RCLK | Demodulator clock | 1187.5Hz clock (refer to the timing diagram) | Type C |

● Input / output circuits

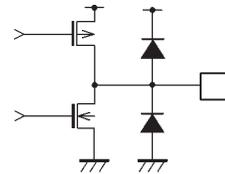
Type A



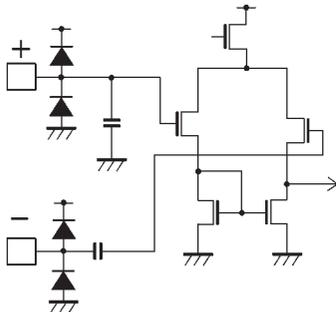
Type B



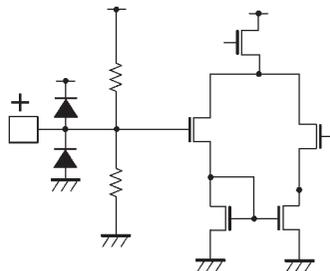
Type C



Type D



Type E

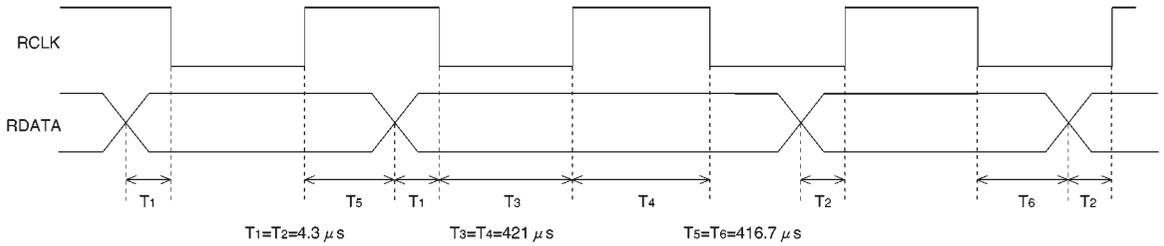


●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD1} = V_{DD2} = 5.0V, V_{SS1} = V_{SS2} = 0.0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------|-------------------|--------------------------|--------------------------|------|-------|--|
| Operating current | I _{DD} | — | 4.5 | 7.0 | mA | I _{DD1} + I _{DD2} |
| Reference voltage | V _{ref} | — | 1/2V _{DD1} | — | V | Pin 3 |
| Input current 1 | I _{IN1} | — | — | 1.0 | μA | MUX V _{IN} =V _{DD1} |
| Output current 1 | I _{OUT1} | — | — | 1.0 | μA | MUX V _{IN} =V _{DD1} |
| Input current 2 | I _{IN2} | — | — | 1.0 | μA | XI V _{IN} =V _{DD2} |
| Output current 2 | I _{OUT2} | — | — | 1.0 | μA | XI V _{IN} =V _{DD2} |
| Output high level voltage 1 | V _{OH1} | V _{DD2} −1.0 | V _{DD2} −0.3 | — | V | RCLK RDATA QUAL I _o =−1.0mA |
| Output low level voltage 1 | V _{OL1} | — | 0.2 | 1.0 | V | RCLK RDATA QUAL I _o =1.0mA |
| 〈Filter block〉 | | | | | | |
| Center frequency | FC | 56.5 | 57.0 | 57.5 | kHz | |
| Gain | GA | 23 | 26 | 29 | dB | F=57.0kHz |
| Attenuation 1 | ATT1 | 18 | 22 | — | dB | 57kHz±4kHz |
| Attenuation 2 | ATT2 | 65 | 80 | — | dB | 38kHz |
| Attenuation 3 | ATT3 | 35 | 50 | — | dB | 67kHz |
| S / N ratio | SN | 30 | 40 | — | dB | 57kHz V _{IN} =3mVrms |
| Maximum input level | V _{MAX1} | — | — | 500 | mVrms | |
| 〈Demodulator〉 | | | | | | |
| RDS detector sensitivity | SRDS | — | 0.5 | 1.0 | mVrms | |
| RDS input level | MRDS | — | — | 300 | mVrms | |
| ARI detector sensitivity | SARI | — | 1.5 | 3.0 | mVrms | |
| Data rate | DRATE | — | 1187.5 | — | Hz | |
| Clock transient vs. data | CT | — | 4.3 | — | μs | |

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● Output data timing



The clock (RCLK) frequency is 1187.5Hz. Depending on the state of the internal PLL clock, the data (RDATA) is replaced in synchronous with either the rising or falling edge of the clock. To read the data, you may choose ei-

ther the rising or the falling edge of the clock as the reference. The data is valid for 416.7μs. after the reference clock edge.

QUAL pin operation: Indicates the quality of the demodulated data.

- (1) Good data: HI
- (2) Poor data: LO

● Electrical characteristic curve

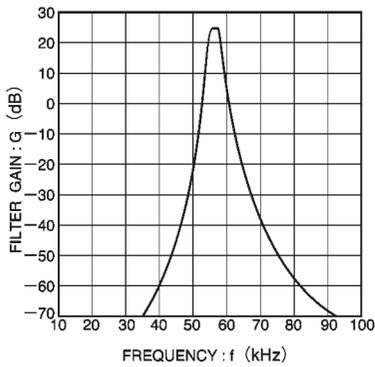


Fig.1 Band-pass filter characteristics

● External dimensions (Units: mm)

