
HA13705C

IPIC (Intelligent Power IC) High Side Solenoid Driver

HITACHI

ADE-207-207 (Z)
1st Edition
July 1996

Description

The HA13705C is high side power driver IC with protectors and diagnostic function. The device is especially designed to switch inductive loads.

Functions

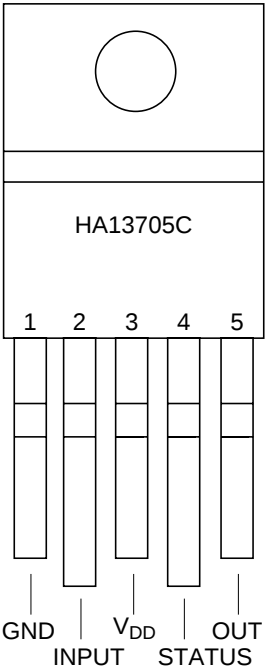
- Power MOS source follower output (2 A)
- With Over Voltage Shut Down circuit (OVSD)
- With Over Current protector circuit (OCSD)
- With Over Temperature Shut Down circuit (OTSD)
- With diagnostic circuit and status output
- With fail safe function under input open circuit condition
- With low voltage inhibit circuit (LVI)
- With output negative voltage clamp circuit

Features

- Protected against 60 V load dump condition
- Low R_{ON} (0.17 Ω Typ)
- Wide operating supply voltage range ($V_{DD} = 7$ V to 25 V)
- High sustaining voltage (-25 V)
- Protected against reverse supply voltage (-13 V)
- Protected against short circuit condition
- Input compatible with TTL, LS-TTL, or 5 V CMOS

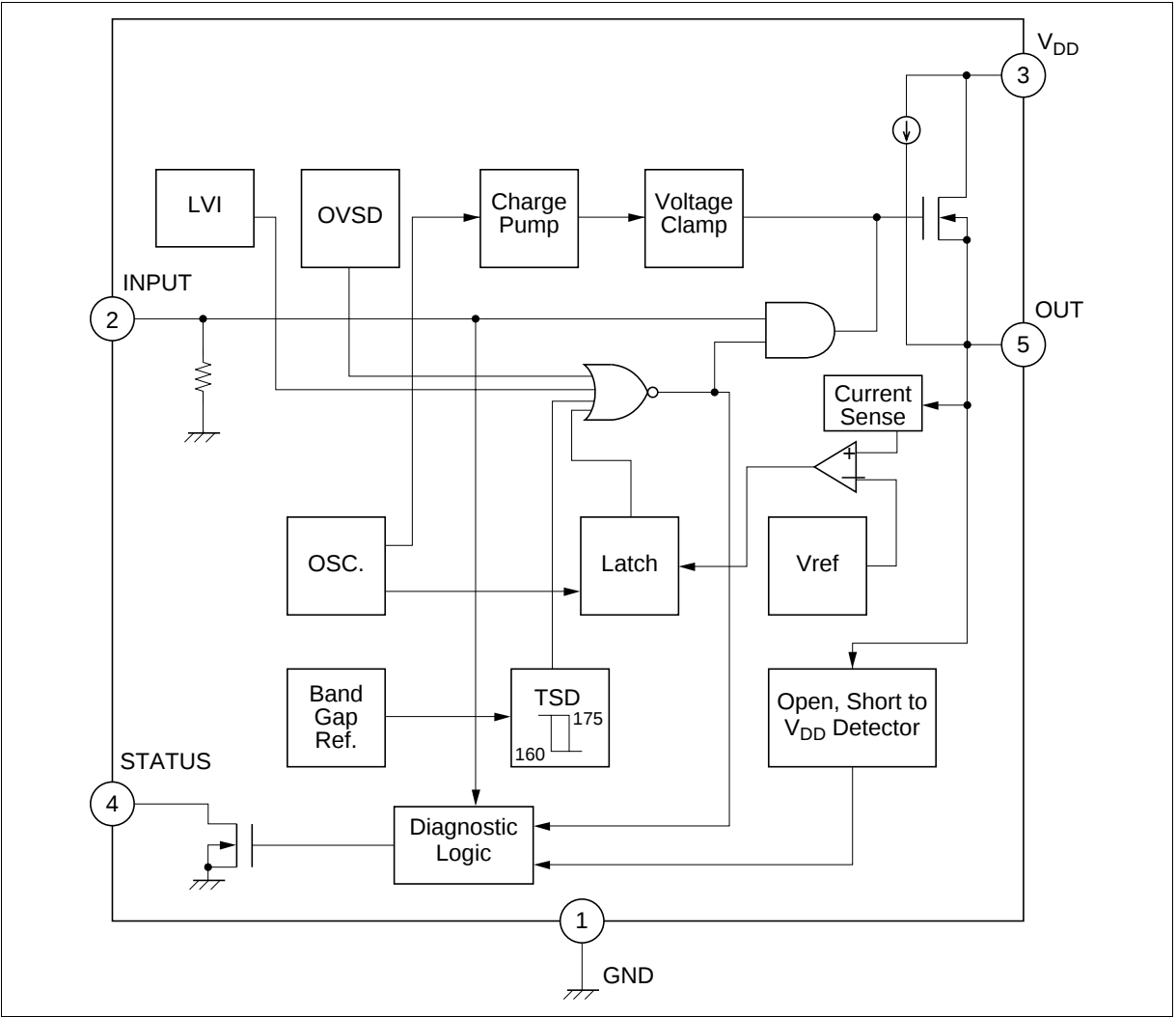
HA13705C

Pin Arrangement



(Top View)

Block Diagram



Truth Table

Mode	In	Out	Status
Normal	L	L	L
	H	H	H
Load short	L	L	L
	H	L	L
Load open	L	H	H
	H	H	H
Short to V _{DD}	L	H	H
	H	H	H
OTSD ^{*1}	L	L	L
	H	L	L
OVSD ^{*2}	L	L	H
	H	L	H
LVI ^{*3}	L	L	H
	H	L	H

L : Low level (0.8 V)

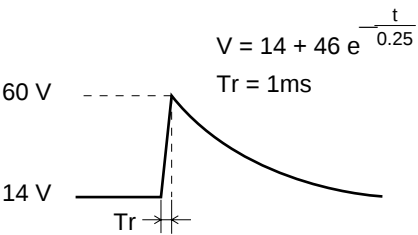
H : High level (2.0 V)

- Notes: 1. OTSD: Over temperature shut down
2. OVSD: Over voltage shut down
3. LVI: Low voltage inhhibit

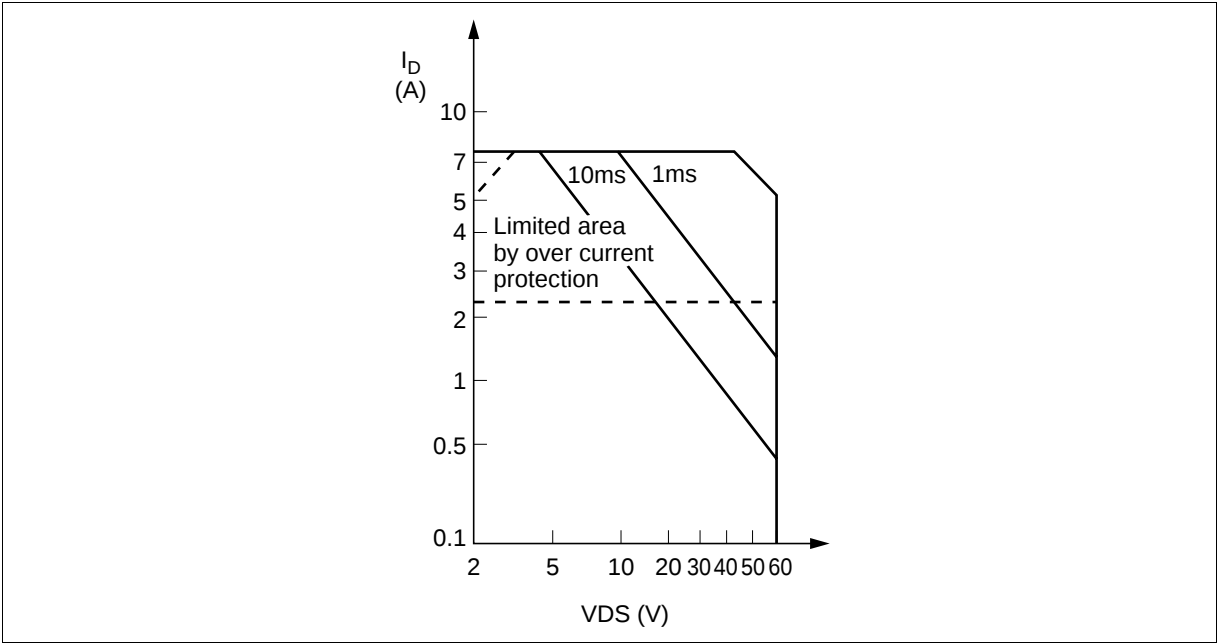
Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Notes
Continuous supply voltage	V _{DD}	−13 to 35	V	1
Transient supply voltage	V _{DD}	60	V	2
Input voltage	V _{IN}	−0.3 to 30	V	
Output voltage	V _{out}	−25 to V _{DD}	V	3
Status voltage	V _s	−0.3 to +15	V	
Output current	I _{out}	—	A	3, 4
Status current	I _s	5	mA	
Power dissipation	P _T	—	W	5
Package thermal resistance/ Junction to case	θ _{j-c}	5	°C/W	
Package thermal resistance/ Junction to air	θ _{j-a}	70	°C/W	
Junction temperature range	T _j	−40 to 150	°C	
Storage temperature range	T _{stg}	−55 to +150	°C	

- Notes: 1. Recommended operating voltage:
V_{DD} = 7 to 16 V (Normal)
16 to 25 V (Jump up start 5 minutes MAX)
−13 V (Reverse Battely 5 minutes MAX)
2. Load dump condition



3. Output Transistor ASO (Reference Data)



- 4. Internally limited
- 5. Maximum power dissipation (P_T (Max)) can be defined as:
$$P_T \text{ (Max)} = (T_{jopr}(\text{Max}) - T_{\text{ambient}}) / (\theta_{j-c} + \theta_{c-a})$$

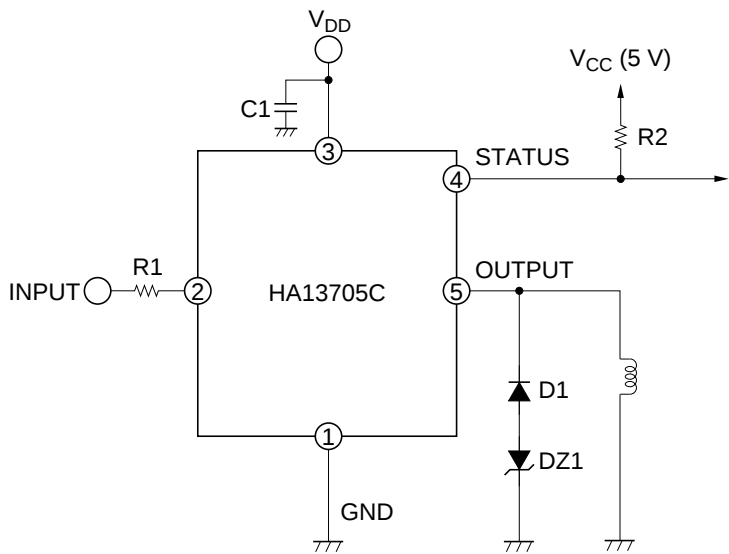
 θ_{c-a} : Thermal resistance between case and air (Depend on heat sink size)

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{ V} \pm 10\%$)

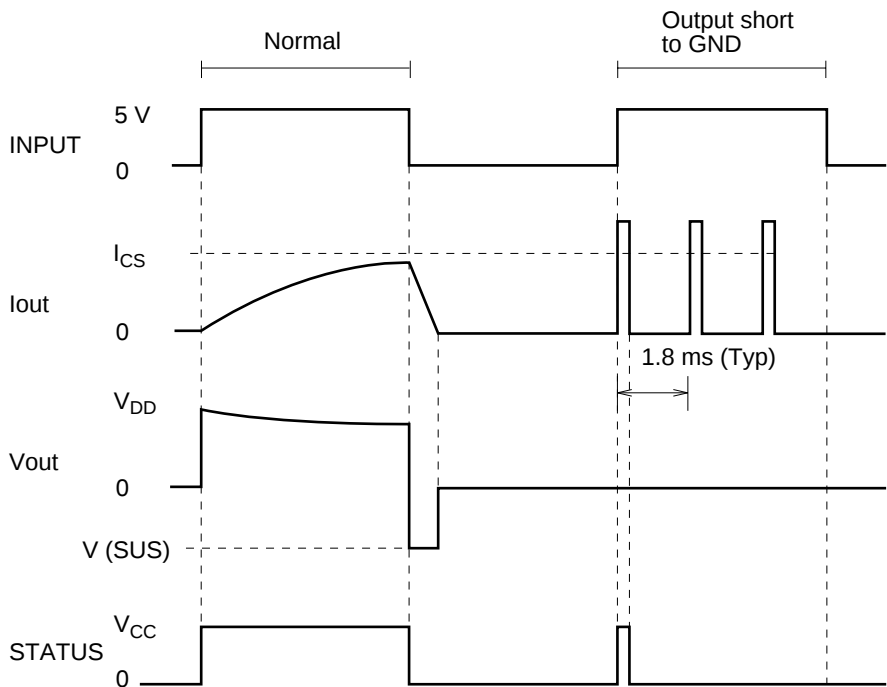
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Pin	Note
Output R (ON)	$R_{DS(ON)}$	—	0.17	0.36	Ω	$I_o = 2\text{ A}$ (@ $T_j = -40$ to 150°C)	5	
Operating supply voltage range	V_{DD}	7	—	25	V		3	
Quiescent current	I_{DD1}	—	—	0.3	mA	$V_{IN} = 0\text{ V}$, $V_{out} = 0\text{ V}$	3	
	I_{DD2}	—	6.0	10.0	mA	$V_{IN} = 5.5\text{ V}$, $V_{out} = \text{open}$	3	
Output leakage current	I_{LEAK}	—	—	0.1	mA	$V_{DD} = 25\text{ V}$, $V_{IN} = 0\text{ V}$, $V_{out} = 0\text{ V}$	5	
Input threshold voltage	V_{IL}	—	—	0.8	V		2	
	V_{IH}	2.0	—	—	V		2	
Input current	I_{IL}	−10	—	60	μA	$V_{IN} = 0.8\text{ V}$	2	
	I_{IH}	50	—	300	μA	$V_{IN} = 5.0\text{ V}$	2	
Propagation delay time	$t_{d(ON)}$	—	—	50	μs	$I_o = 1\text{ A}$	2, 5	
	t_r	—	—	90	μs		5	
	$t_{d(OFF)}$	—	—	50	μs		2, 5	
	T_f	—	—	50	μs		5	
Open det. threshold current	I_{OD}	2	10	100	μs		4, 5	
Current limiter operating level	I_{CS}	3.0	4.3	7.5	A		5	
LVI operating level	L.V.I	—	5	6	V		3	
Over voltage shut down	Operating level	OVSD	26	29	33	V	3	
	Hysteresis	VHYS	0.15	0.5	1.5	V	3	
Output sustain voltage	$V_{(SUS)}$	—	—	−25	V	$I_{out} = 20\text{ mA}$	5	
Over temperature shut down	Operating level	OTSD	150	175	—	$^\circ\text{C}$	5	1
	Hysteresis	THYS	—	15	—	$^\circ\text{C}$	5	1
Status on voltage	V_{SL}	—	—	0.4	V	$I_s = 1\text{ mA}$	4	
Status leakage current	$I_{S(Leak)}$	−10	—	100	μA	$V_s = 5.0\text{ V}$	4	

Notes: 1. Design parameter only (no test)

Solenoid Drive Application and it's Waveform

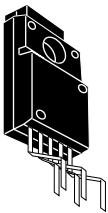
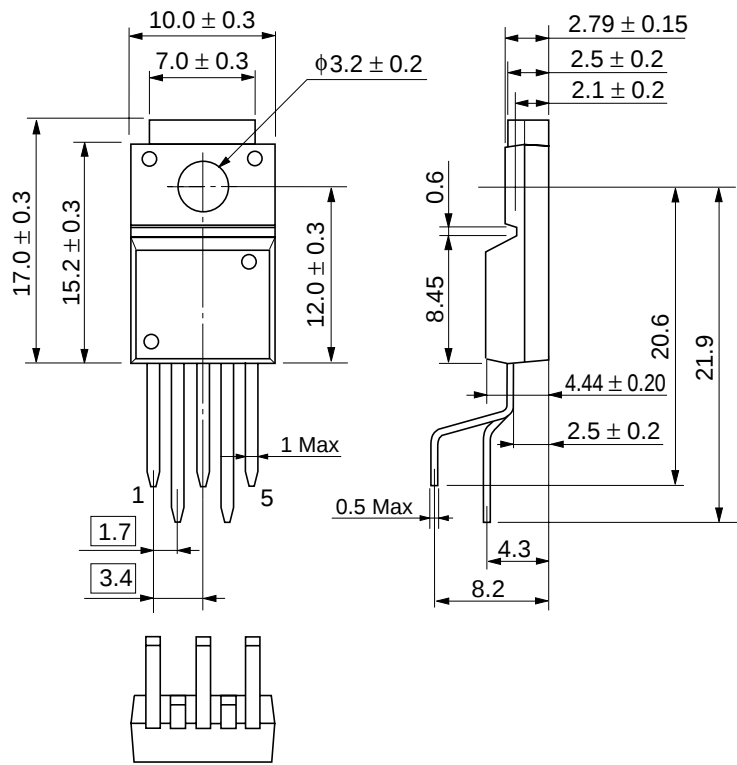


R1 : Input series resistance to protect CMOS driver.
R2 : Pull up resistance at status output.
C1 : The capacitor to compensate the inductance at V_{DD} line.
D1, DZ1 : for Reverse voltage clamp



Package Dimensions

Unit: mm



Hitachi Code	SP-5TA
JEDEC	—
EIAJ	—
Weight (reference value)	2.0 g

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