The Future of Analog IC Technology

MP2004

Dual, Low Noise, High PSRR 200mA Linear Regulator

DESCRIPTION

The MP2004 is a dual-channel, low noise, low dropout and high PSRR linear regulator. The output voltage of MP2004 ranges from 1.2V to 5V and 1% accuracy by operating from a +2.5V to +6.0V input. The MP2004 can supply up to 200mA of load current at each channel.

The MP2004 uses an internal PMOS as the pass element, which consumes 114μA supply current (both LDOs on) at no load condition. The EN1 and EN2 pins control each output respectively. When both channels shutdown simultaneously, the chip will be turned off and consume nearly zero operation current which is suitable for battery-power devices. The MP2004 features current limiting and over temperature protection.

It is available in a small 6-pin TSOT23 package.

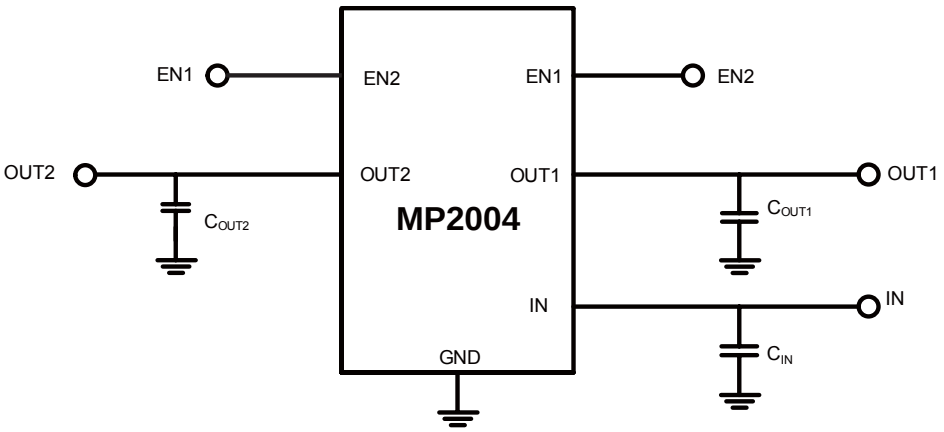
FEATURES

- Two LDOs in a TSOT23-6 Package
- Up to 200mA Output Current (Per Channel
- Two Enable Pins Control Each Output
- 69dB PSRR (100Hz)
- 95μV_{RMS} Low Noise Output
- 110mV Dropout at 100mA Load
- Very Fast Transient Responses with Small Output Capacitor
- Current Limiting and Thermal Protection

APPLICATIONS

- Cellular Phones
- Laptop PCs
- Hand-held Equipment
- Netbook Computing

TYPICAL APPLICATION



ORDERING INFORMATION*

Part Number	V_{OUT1}	V_{OUT2}	Package	Temperature	Top Marking
MP2004DJ-JG-LF-Z	2.5V	1.8V	TSOT23-6	-40°C to +85°C	2B
MP2004DJ-ZS-LF-Z	5.0V	3.3V			2L
MP2004DJ-PN-LF-Z	3.0V	2.85V			3L
MP2004DJ-DD-LF-Z	1.85V	1.85V			4L
MP2004DJ-SJ-LF-Z	3.3V	2.5V			5L
MP2004DJ-MG-LF-Z	2.8V	1.8V			6L

* Other output voltage versions between 1.2V and 5.0V are available in 100mV increments. Contact factory for availability.

ORDERING GUIDE**

MP2004DJ-☐☐-LF-Z

- V_{OUT2}
- V_{OUT1}
- Package Type
  J: TSOT23-6
- Operating Temperature Range
  D: Extended Temperature Range (-40°C to +85°C)

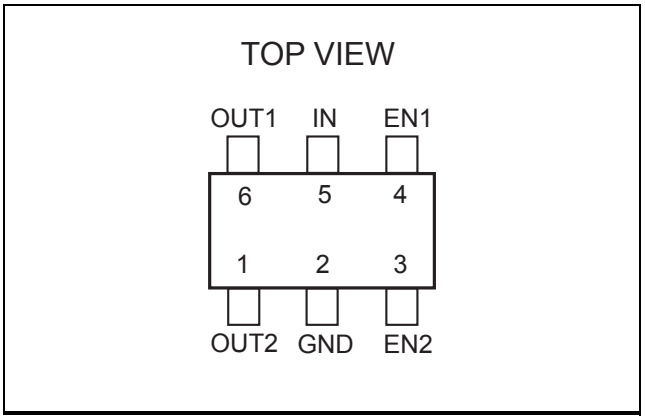
** For RoHS Compliant Packaging, add suffix - LF (e.g. MP2004DJ-☐☐-LF); For Tape and Reel, add suffix -Z (e.g. MP2004DJ-☐☐-LF-Z).

OUTPUT VOLTAGE SELECTOR GUIDE***

Code	V_{OUT}	Code	V_{OUT}
C	1.2	T	2.65
B	1.3	L	2.7
F	1.5	**M**	**2.8**
W	1.6	**N**	**2.85**
G	**1.8**	V	2.9
D	**1.85**	**P**	**3.0**
Y	1.9	Q	3.1
H	2.0	X	3.15
E	2.1	R	3.2
J	**2.5**	**S**	**3.3**
K	2.6	**Z**	**5.0**

*** Code in **Bold** are standard versions. For other output voltages between 1.2V and 5.0V contact factory for availability. Minimum order quantity on non-standard versions is 25,000 units.

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Input Voltage 6.5V
Continuous Power Dissipation (T_A = +25°C)(2)
..... 0.45W
Operation Temperature Range ... -40°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10sec) .....260°C

Recommended Operating Conditions (3)

Supply Input Voltage.....2.5V to 6.0V
Enable Input Voltage .....0V to 6.0V
Junction Temperature Range . –40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 .....220 ....110. . °C/W

Notes:

1) Exceeding these ratings may cause permanent damage to the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, V_{OUT1}=2.5V, V_{OUT2}=1.8V, C_{IN}=C_{OUT1}=C_{OUT2}=2.2uF, EN1=EN2=V_{IN}, Typical Value at T_A=25°C for each LDO unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Accuracy (Load regulation)(5)	ΔV_{OUT}	I_{LOAD} = 1mA to 200mA	-1		+1	%
Maximum Output Current	I_{MAX}	Continuous	200			mA
Current Limit	I_{LIM}	R_{Load}=1 Ω		450		mA
Quiescent Current	I_Q	No Load		114		uA
Dropout Voltage (6)	V_{DROP}	I_{OUT1} = 100mA		110		mV
		I_{OUT1} = 200mA		250		mV
Line Regulation(7)	ΔV_{LINE}	V_{IN} =(V_{OUT}+0.4V or 2.5V) to 6V, I_{OUT}=1mA	-0.05		+0.05	%/V
EN Input High Threshold	V_{IH}	V_{IN} = 2.5V to 6.0V	1.6			V
EN Input Low Threshold	V_{IL}	V_{IN} = 2.5V to 6.0V			0.45	V
EN Input Bias Current	I_{SD}	EN= V_{IN} =6.5V			300	nA
Shutdown Supply Current	I_{GSD}	EN1 = EN2 = GND		0.03	1	uA
Thermal Shutdown Temperature	T_{SD}			140		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			10		°C
Output Voltage Noise		10Hz to 100kHz, C_{OUT}=2.2μF, I_{LOAD}=1mA		95		μV_{RMS}
Output PSRR		100Hz, C_{OUT} = 2.2μF, I_{LOAD} = 100mA		69		dB

Notes:

5) Load Regulation= $\frac{V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}}{V_{OUT(NOM)}} \times 100(\%)$

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

7) Line Regulation= $\frac{V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times 100(\%/V)$

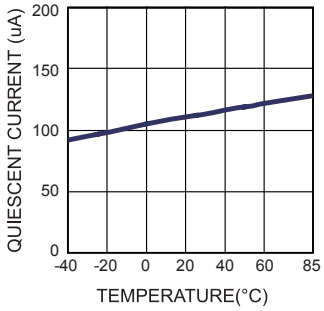
PIN FUNCTIONS

Pin #	Name	Description
1	VOUT2	Channel 2 Output Voltage
2	GND	Common Ground
3	EN2	Channel 2 Enable (Active High). Do Not Float This Pin.
4	EN1	Channel 1 Enable (Active High). Do Not Float This Pin.
5	VIN	Supply Input Pin
6	VOUT1	Channel 1 Output Voltage

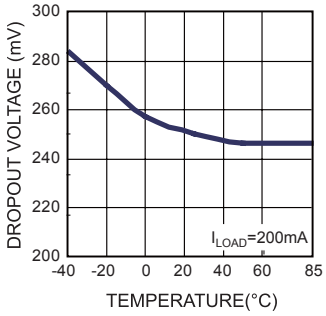
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.6V, V_{OUT1}=2.5V, V_{OUT2}=1.8V, C_{IN}=C_{OUT1}=C_{OUT2}=2.2uF, EN1=EN2=V_{IN}, Typical Value at T_A=25°C for Both Channel Enabled.

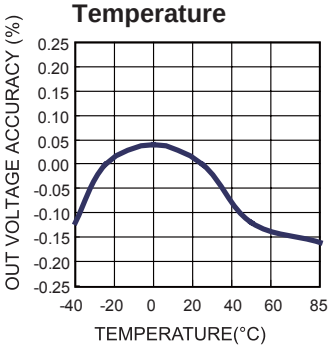
Quiescent Current vs. Temperature



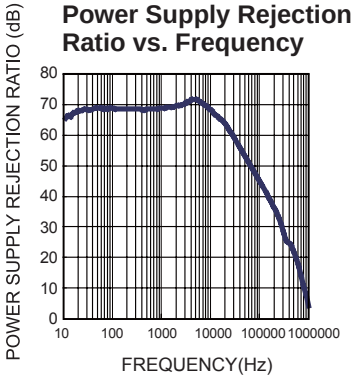
Dropout Voltage vs. Temperature



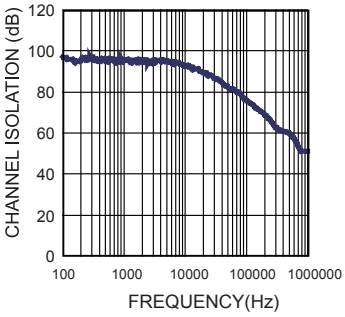
Out Voltage Accuracy vs. Temperature



Power Supply Rejection Ratio vs. Frequency

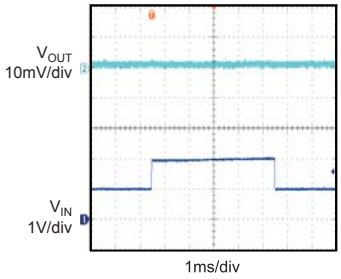


Channel-to-Channel Isolation vs. Frequency



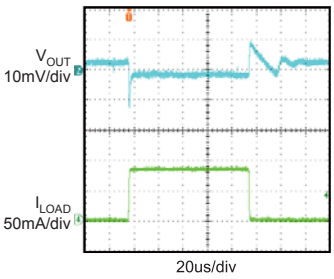
Line Transient Response

V_{OUT}=3.5V to 4.5V, C_{IN}=0uF, C_{OUT}=2.2uF
No Load



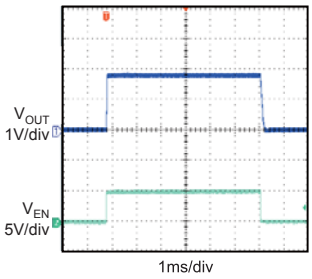
Load Transient Response

V_{IN}=3.6V, V_{OUT}=1.8V
I_{LOAD}=1mA to 80mA, with Resistor Load



EN Pin Shut Down Response

V_{IN}=3.6V, V_{OUT}=1.8V, V_{EN}=0 to 5V
I_{LOAD}=50mA, with Resistor Load



BLOCK DIAGRAM

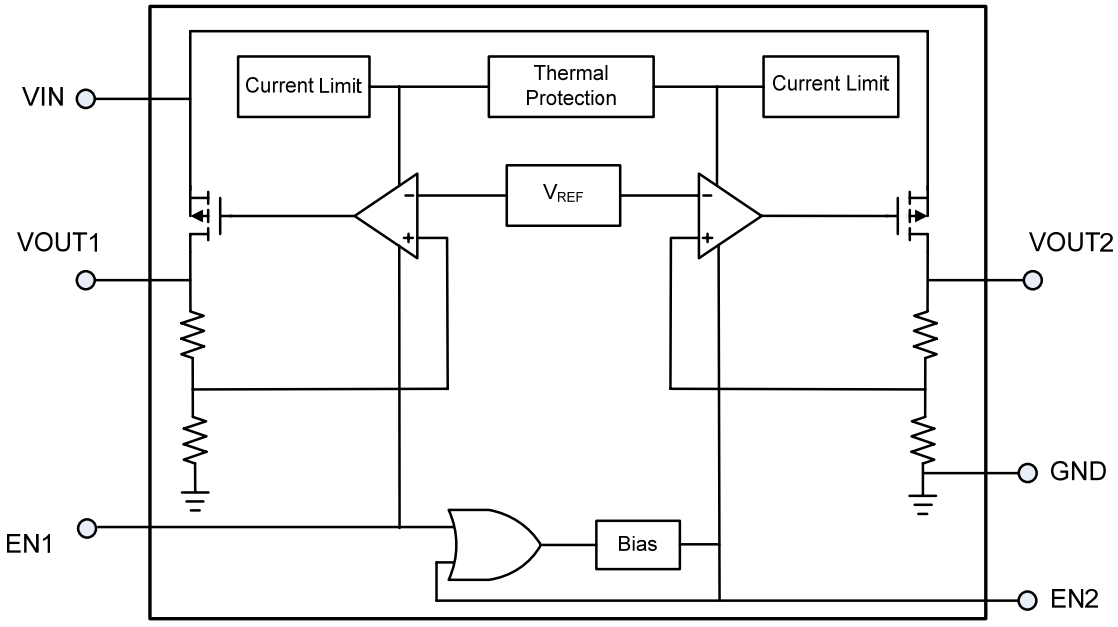


Figure1—Functional Block Diagram

OPERATION

The MP2004 integrates two low noise, low dropout, low quiescent current and high PSRR linear regulators. It is intended for use in devices that require very low voltage, low quiescent current power such as wireless LAN, battery-powered equipment and hand-held equipment. The MP2004 uses internal PMOSs as the pass elements and features internal thermal shutdown and an internal current limit circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP2004 is very low.

Shutdown

The MP2004 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be tied to VIN to keep the regulator output always on if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MP2004 includes two independent current limit structures which monitor and control each PMOS's gate voltage limiting the guaranteed maximum output current to 200mA.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds +140ºC, allowing the IC to cool. When the IC's junction temperature drops by 10ºC, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP2004. For reliable operation, junction temperature should be limited to 125 ºC maximum.

Load-Transient Considerations

The output response of load-transient consists of a DC shift and transient response. Because of the excellent load regulation of MP2004, the DC shift is very small. The output voltage transient depends on the output capacitor's value and the ESR. Increasing the capacitance and decreasing the ESR will improve the transient response. Typical output voltage transient spike of MP2004 for a step change in the load current from 0mA to 80mA is tens mV.

APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ - $T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connect the GND pin of MP2004 to ground using a large pad or ground plane helps to channel heat away.

Input Capacitor Selection

Using a capacitor whose value is >0.47μF on the MP2004 input and the amount of capacitance can be increased without limit. Larger values will help to improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also suffice.

Output Capacitor Selection

The MP2004 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A ceramic capacitor in the range of 0.47μF and 10μF, and with ESR lower than 1.2Ω is suitable for the MP2004 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

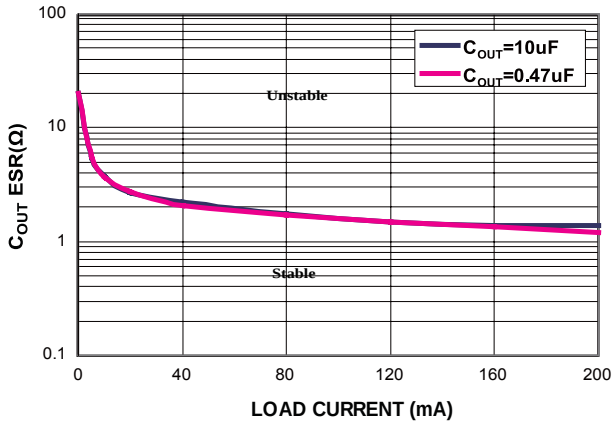


Figure 2—Relationship between ESR and LDO Stability

Reverse Current Path

The PMOS used in the MP2004 has an inherent diode connected between input and output (see Figure3). If V_{OUT} -V_{IN} is more than a diode-drop, this diode gets forward biased and starts to conduct. To avoid misoperation, an external Schottky connected in parallel with the internal parasitic diode prevents it from being turned on by limiting the voltage drop across it to about 0.3V (see Figure 4).

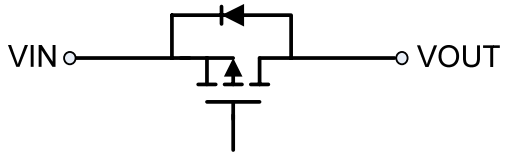


Figure 3—Inherent Diode Connected between Each Regulator Input and Output

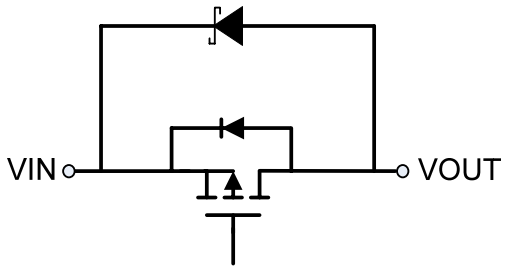


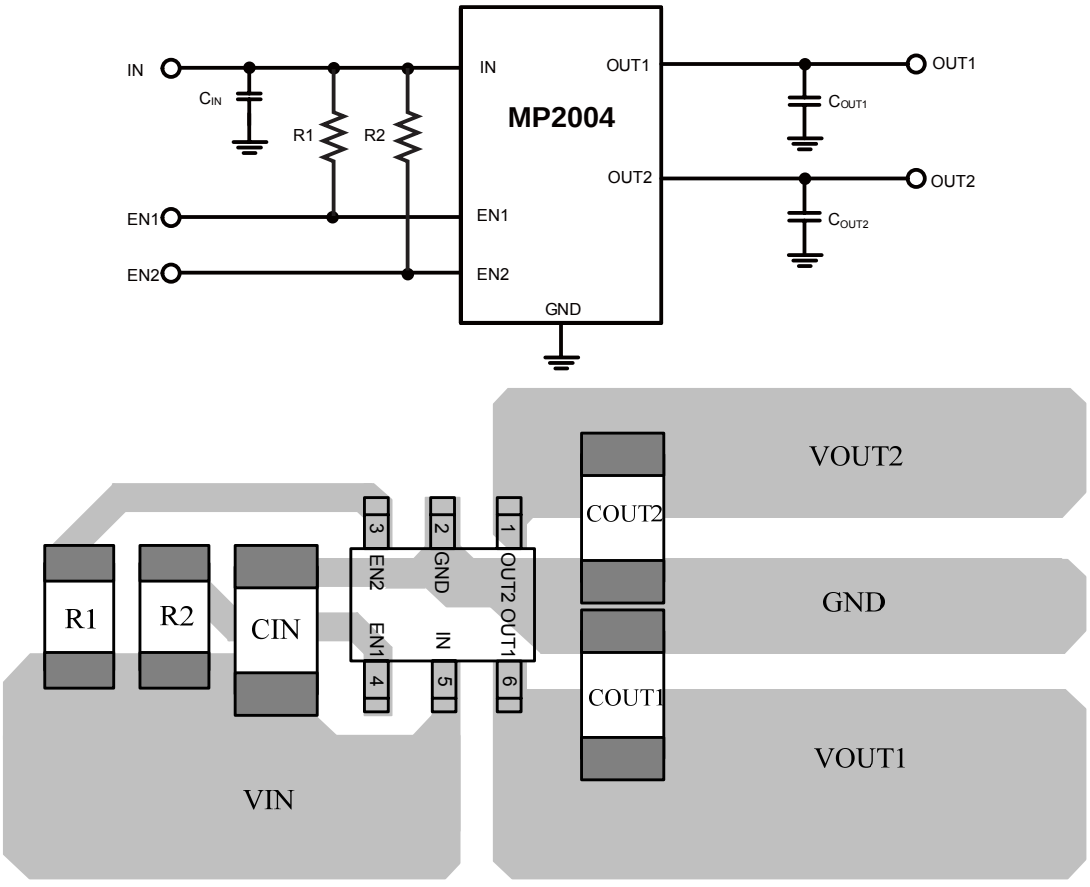
Figure 4—External Schottky Diode Connected in Parallel with the Internal Parasitic Diode

PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 5 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

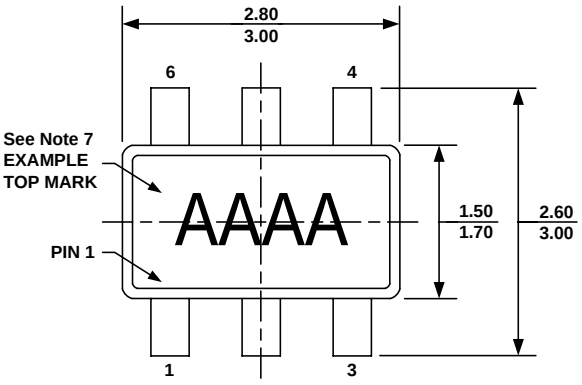


Top Layer

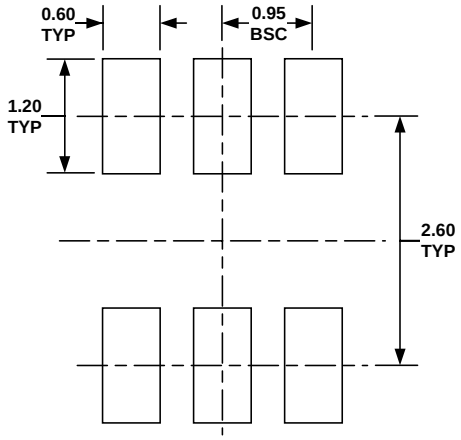
Figure 5—PCB Layout

PACKAGE INFORMATION

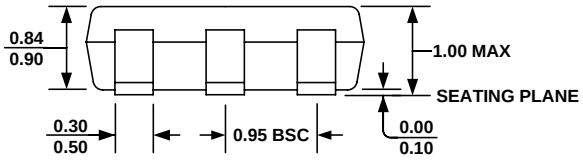
TSOT23-6



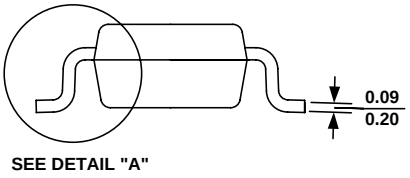
TOP VIEW



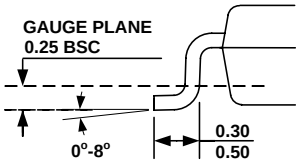
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)