

COMPOUND FIELD EFFECT POWER TRANSISTOR

μ PA1560

N-CHANNEL POWER MOS FET ARRAY

SWITCHING

INDUSTRIAL USE

DESCRIPTION

The μ PA1560 is N-Channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

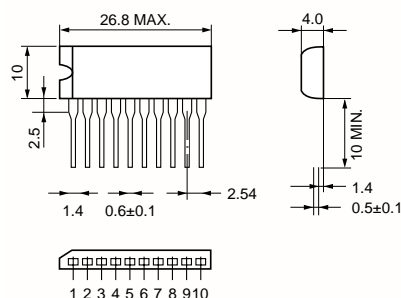
FEATURES

- Full mold package with 4 circuits
- 4 V driving is possible
- Low on-state resistance
 $R_{DS(on)1} = 165 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 1.5 \text{ A)}$
 $R_{DS(on)2} = 200 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 1.5 \text{ A)}$
- Low input capacitance
 $C_{iss} = 600 \text{ pF TYP.}$

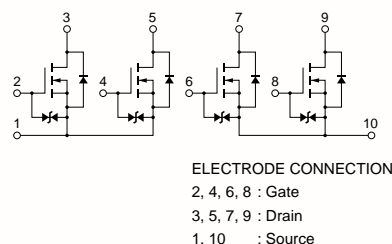
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1560H	10-pin SIP

PACKAGE DRAWING (Unit : mm)



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	120	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	$V_{GSS(DC)}$	+ 20, -10	V
Drain Current (DC)	$I_{D(DC)}$	± 3.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 12	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	28	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	3.7	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	3.0	A
Single Avalanche Energy ^{Note2}	E_{AS}	0.9	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 60 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

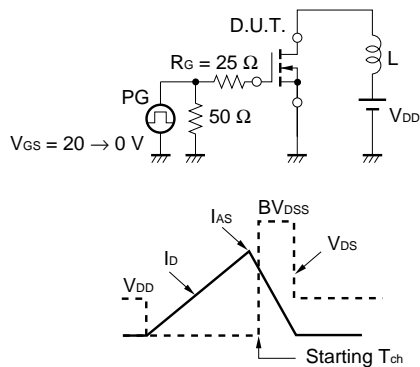
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

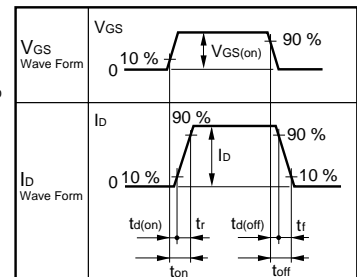
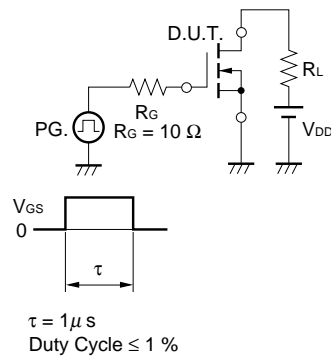
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 1.5 A		130	165	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 1.5 A		145	200	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	1.0	1.8	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 1.5 A	2	4.5		S
Drain Leakage Current	I _{DSS}	V _{DS} = 120 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		600		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		160		pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		70		pF
Turn-on Delay Time	t _{d(on)}	I _D = 1.5 A		35		ns
Rise Time	t _r	V _{GS(on)} = 10 V		80		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 60 V		700		ns
Fall Time	t _f	R _L = 30 Ω		250		ns
Total Gate Charge	Q _G	I _D = 3.0 A		28		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 96 V		2.5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		9		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 3.0 A, V _{GS} = 0 V		0.9		V
Reverse Recovery Time	t _{rr}	I _F = 3.0 A, V _{GS} = 0 V		160		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		280		nC

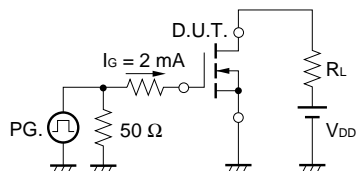
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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