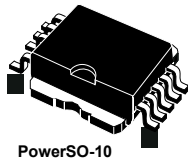


## Quad high-side smart power solid-state relay



### Product status link

[VN340SP-E & VN340SP-33-E](#)

### Product label



### Features

- Operating output current: 0.7 A (VN340SP-E) or 1 A (VN340SP-33-E)
- Digital I/O clamped at 32 V minimum voltage
- Shorted load and overtemperature protections
- Protection against loss of ground
- Built-in current limiter
- Undervoltage shutdown
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

### Applications

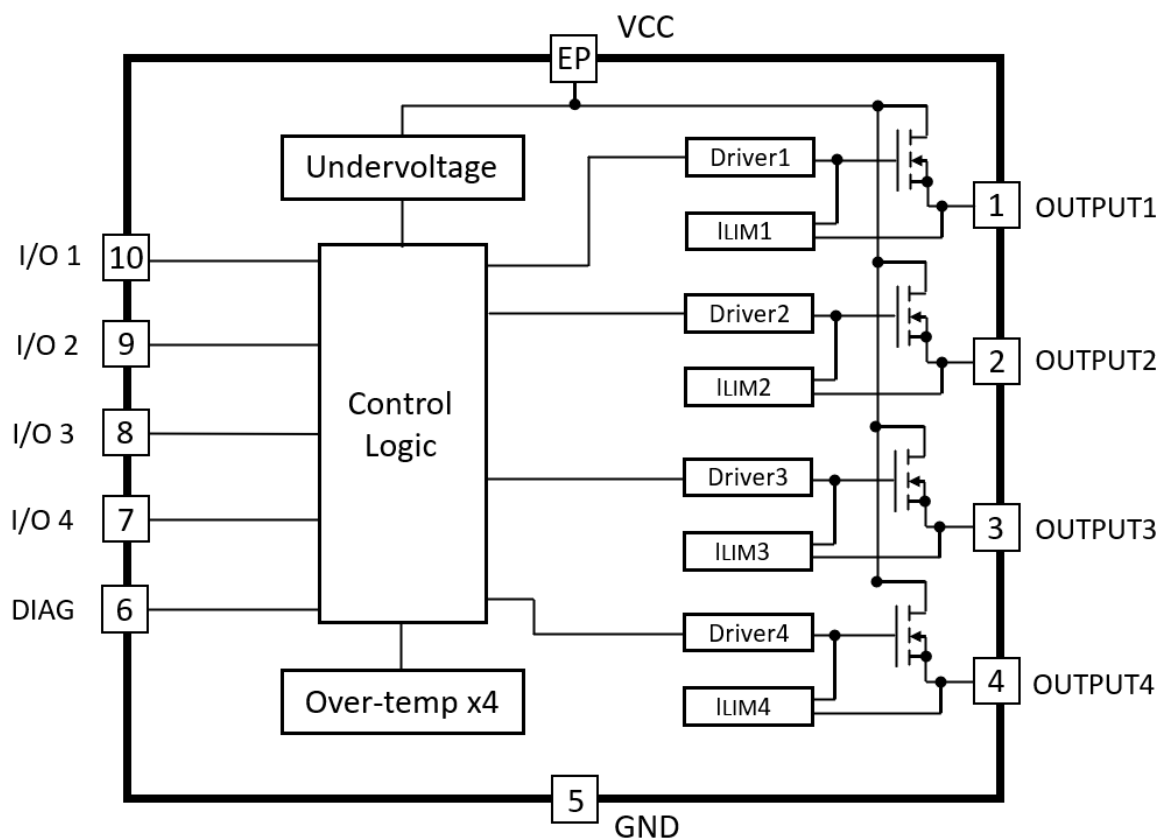
- Vending machines
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

### Description

VN340SP-E & VN340SP-33-E are monolithic devices developed using STMicroelectronics' VIPower technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation prevents dropping of the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. The open drain diagnostic output indicates overtemperature conditions. Each I/O is pulled down when the overtemperature condition of the relative channel is verified.

# 1 Block diagram

Figure 1. Block diagram



## 2 Pin connection

Figure 2. Connection diagram (top view)

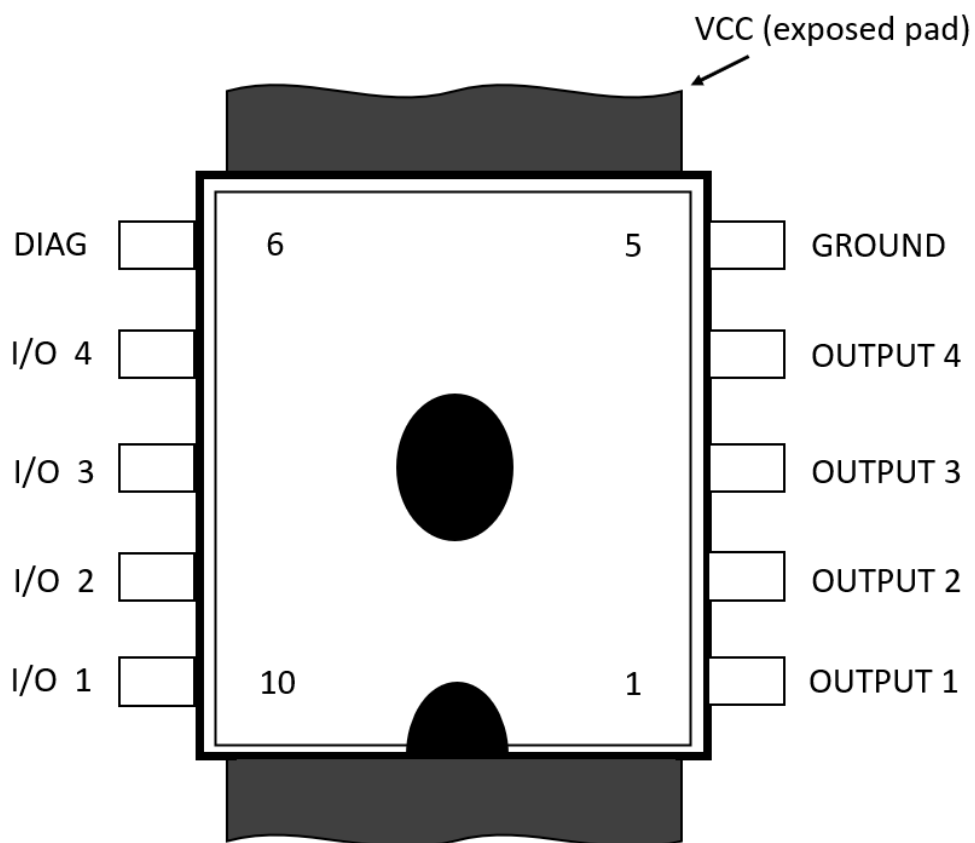
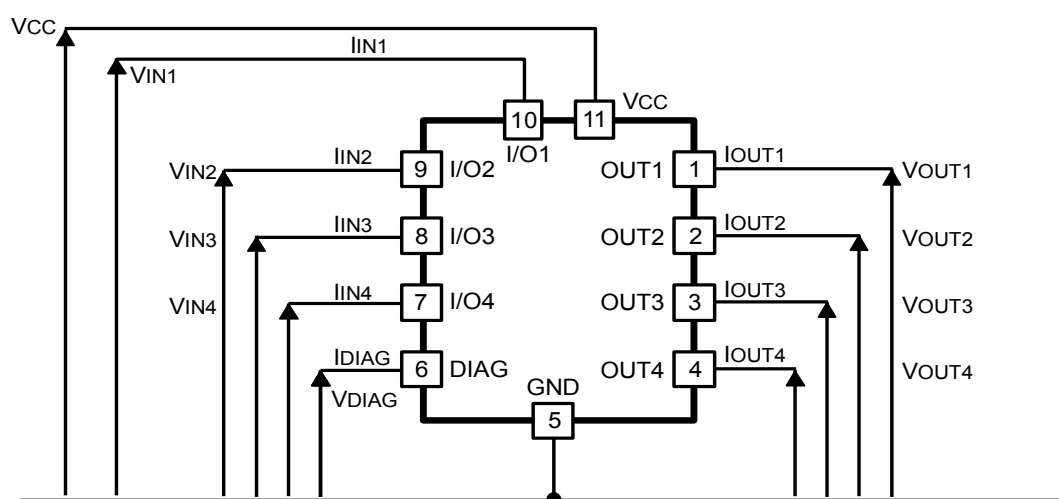


Figure 3. Current and voltage conventions



### 3 Maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol     | Parameter                                                                                                                         | Value              | Unit             |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------|
| $V_{CC}$   | Power supply voltage                                                                                                              | 45                 | V                |
| $-V_{CC}$  | Reverse supply voltage                                                                                                            | -4                 | V                |
| $I_{OUT}$  | Output current                                                                                                                    | Internally limited | A                |
| $I_R$      | Reverse output current (per channel)                                                                                              | -6                 | A                |
| $I_{IN}$   | Input current range                                                                                                               | -1 to +10          | mA               |
| $I_{DIAG}$ | Diag pin current                                                                                                                  | -1 to +10          | mA               |
| $V_{ESD}$  | Electrostatic discharge ( $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$ )                                                        | 2000               | V                |
| $E_{AS}$   | Single pulse avalanche energy, one channel active, $T_J = 125\text{ }^\circ\text{C}$ , $I_{LOAD} = 0.625\text{ A}$                | 10                 | J                |
|            | Single pulse avalanche energy all channels active simultaneously, $T_J = 125\text{ }^\circ\text{C}$ , $I_{LOAD} = 0.625\text{ A}$ | 2                  | J                |
| $P_{TOT}$  | Power dissipation at $T_C = 25\text{ }^\circ\text{C}$                                                                             | Internally limited | W                |
| $T_J$      | Junction operating temperature                                                                                                    | Internally limited | $^\circ\text{C}$ |
| $T_{STG}$  | Storage temperature                                                                                                               | -55 to 150         | $^\circ\text{C}$ |

**Table 2. Thermal data**

| Symbol       | Parameter                                          | Max Value | Unit               |
|--------------|----------------------------------------------------|-----------|--------------------|
| $R_{th(JC)}$ | Thermal resistance junction-case <sup>(1)</sup>    | 3         | $^\circ\text{C/W}$ |
| $R_{th(JA)}$ | Thermal resistance junction-ambient <sup>(2)</sup> | 50        | $^\circ\text{C/W}$ |

1. Per channel.

2. When mounted on a four-layer FR4, with the minimum recommended pad size.

## 4 Electrical characteristics

10 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>J</sub> < 125 °C; unless otherwise specified

**Table 3. Power section**

| Symbol              | Parameter                  | Test conditions                                                                                                          | Min.                | Typ.                | Max.                | Unit |
|---------------------|----------------------------|--------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|---------------------|------|
| V <sub>CC</sub>     | Supply voltage             |                                                                                                                          | 10                  |                     | 36                  | V    |
| R <sub>DS(on)</sub> | On-state resistance        | I <sub>OUT</sub> = 0.5 A @ T <sub>J</sub> = 25 °C                                                                        |                     |                     | 0.2                 | Ω    |
|                     |                            | I <sub>OUT</sub> = 0.5 A @ T <sub>J</sub> = 85 °C                                                                        |                     |                     | 0.32                |      |
|                     |                            | I <sub>OUT</sub> = 0.5 A @ T <sub>J</sub> = 125 °C                                                                       |                     |                     | 0.4                 |      |
| I <sub>S</sub>      | Supply current             | All channels in OFF-state                                                                                                |                     |                     | 1                   | mA   |
|                     |                            | V <sub>IN</sub> = 30 V, I <sub>OUT</sub> = 0 V, T <sub>J</sub> = 125 °C                                                  |                     |                     | 6                   |      |
| V <sub>OL</sub>     | Low state output voltage   | V <sub>IN</sub> = V <sub>IL</sub> ; R <sub>LOAD</sub> > = 10 MΩ                                                          |                     |                     | 1.5                 | V    |
| I <sub>LGND</sub>   | Output current at turn-off | V <sub>CC</sub> = V <sub>IN</sub> = V <sub>GND</sub> = V <sub>STAT</sub> = 18 to 30 V, T <sub>A</sub> = - 25 °C to 85 °C |                     |                     | 2                   | mA   |
| V <sub>demag</sub>  | Demagnetization voltage    | I <sub>OUT</sub> = 0.5 A; L <sub>LOAD</sub> >= 1 mH                                                                      | V <sub>CC</sub> -65 | V <sub>CC</sub> -55 | V <sub>CC</sub> -45 | V    |

**Table 4. Switching (V<sub>CC</sub> = 24 V, T<sub>J</sub> = 25 °C)**

| Symbol              | Parameter                             | Test conditions                                                    | Min. | Typ. | Max. | Unit |
|---------------------|---------------------------------------|--------------------------------------------------------------------|------|------|------|------|
| t <sub>d(ON)</sub>  | Turn-on delay time                    | I <sub>OUT</sub> = 0.5 A, resistive load, input rise time < 0.1 μs |      | 52   | 100  | μs   |
| t <sub>r</sub>      | Rise time of output current           |                                                                    |      | 94   | 250  |      |
| t <sub>d(OFF)</sub> | Turn-off delay time of output current |                                                                    |      | 34   | 50   |      |
| t <sub>f</sub>      | Fall time                             |                                                                    |      | 8    | 20   |      |

**Table 5. Logic inputs**

| Symbol               | Parameter                              | Test conditions         | Min. | Typ. | Max. | Unit |
|----------------------|----------------------------------------|-------------------------|------|------|------|------|
| V <sub>IL</sub>      | I/O input low level voltage            |                         |      |      | 2    | V    |
| V <sub>IH</sub>      | I/O input high level voltage           |                         | 3.5  |      |      | V    |
| V <sub>I(HYST)</sub> | I/O input hysteresis voltage           |                         |      | 0.5  |      | V    |
| I <sub>IN</sub>      | I/O input current                      | V <sub>IN</sub> = 30 V  |      |      | 25   | μA   |
| V <sub>ICL</sub>     | I/O input clamp voltage <sup>(1)</sup> | I <sub>IN</sub> = 1 mA  | 32   | 36   |      | V    |
|                      |                                        | I <sub>IN</sub> = -1 mA |      | -0.7 |      |      |

1. The input voltage is internally clamped at 32 V minimum, the input pins can be connected to a higher voltage by an external resistor, which cannot exceed 10 mA

**Table 6. Protection and diagnostic**

| Symbol           | Parameter                         | Test conditions                                                               | Min.               | Typ. | Max. | Unit               |
|------------------|-----------------------------------|-------------------------------------------------------------------------------|--------------------|------|------|--------------------|
| $V_{DIAG}^{(1)}$ | Status voltage output low         | $I_{DIAG} = 5 \text{ mA}$ (fault condition)                                   |                    |      | 1    | V                  |
| $V_{SCL}$        | Status clamp voltage              | $I_{DIAG} = 1 \text{ mA}$                                                     | 32                 | 36   |      | V                  |
|                  |                                   | $I_{DIAG} = -1 \text{ mA}$                                                    |                    | -0.7 |      | V                  |
| $V_{USD}$        | Undervoltage shutdown             |                                                                               | 5                  |      | 8    | V                  |
| $I_{lim}$        | DC short-circuit current          | $V_{CC} = 24 \text{ V}; R_{LOAD} < 10 \text{ m}\Omega$                        | 0.7 <sup>(2)</sup> |      | 2    | A                  |
|                  |                                   |                                                                               | 1 <sup>(3)</sup>   |      |      |                    |
| $I_{OVPK}$       | Peak short-circuit current        | $V_{CC} = 24 \text{ V}; V_{IN} = 30 \text{ V}; R_{LOAD} < 10 \text{ m}\Omega$ |                    |      | 4    | A                  |
| $I_{DIAGH}$      | Leakage on DIAG pin in high state | $V_{DIAG} = 24 \text{ V}$                                                     |                    |      | 25   | $\mu\text{A}$      |
| $I_{LOAD}$       | Output leakage current            | $V_{CC} = 10 \text{ to } 36 \text{ V}; V_{IN} = V_{IL}$                       |                    |      | 50   | $\mu\text{A}$      |
| $t_{SC}$         | Delay time of current limiter     |                                                                               |                    |      | 100  | $\mu\text{s}$      |
| $T_{TSD}$        | Junction shutdown temperature     |                                                                               | 150                | 170  |      | $^{\circ}\text{C}$ |
| $T_R$            | Junction reset temperature        |                                                                               | 135                | 155  |      | $^{\circ}\text{C}$ |

1. Status determination > 100  $\mu\text{s}$  after the switching edge.

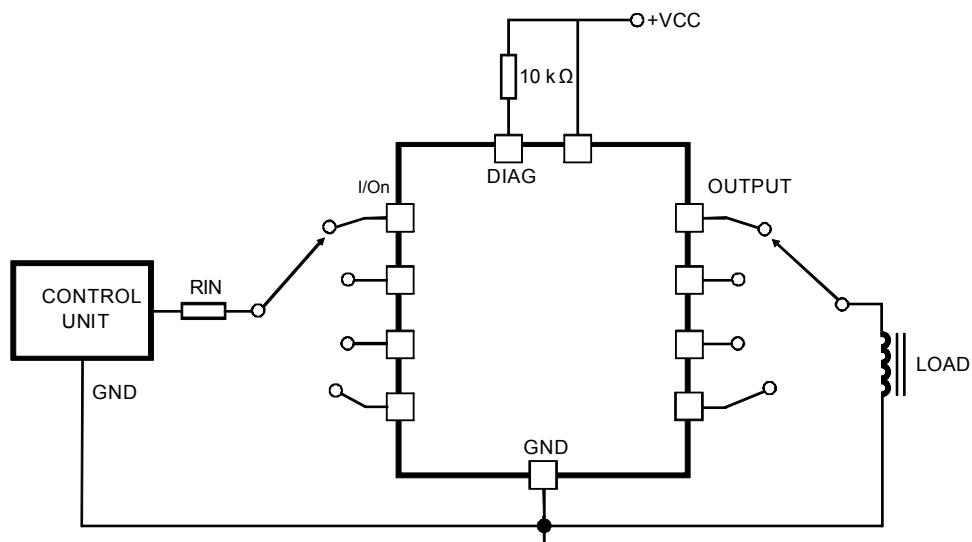
2. VN340SP-E

3. VN340SP-33-E

**Note:** If the INPUT pin is left floating the corresponding channel automatically switches off. If GND pin is disconnected the channel switches off provided that  $V_{CC}$  does not exceed 36 V.

## 5 Test circuits

**Figure 4. Avalanche energy test circuit**



**Figure 5. Peak short-circuit test diagram**

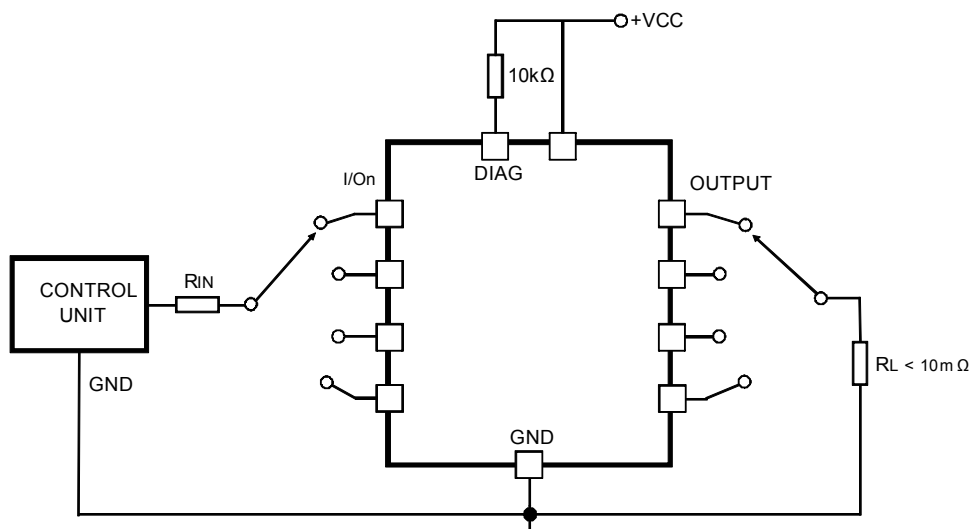
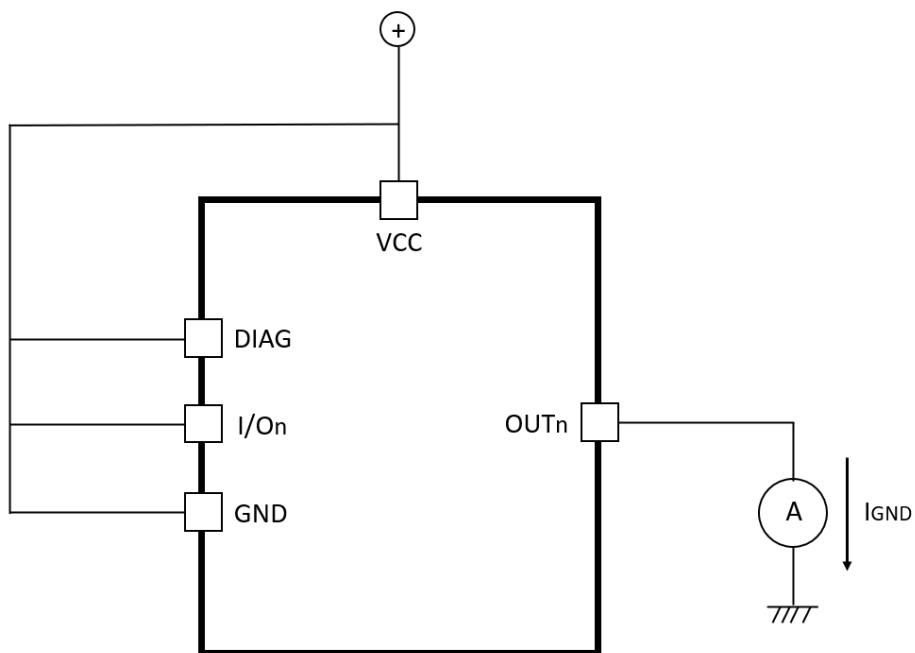


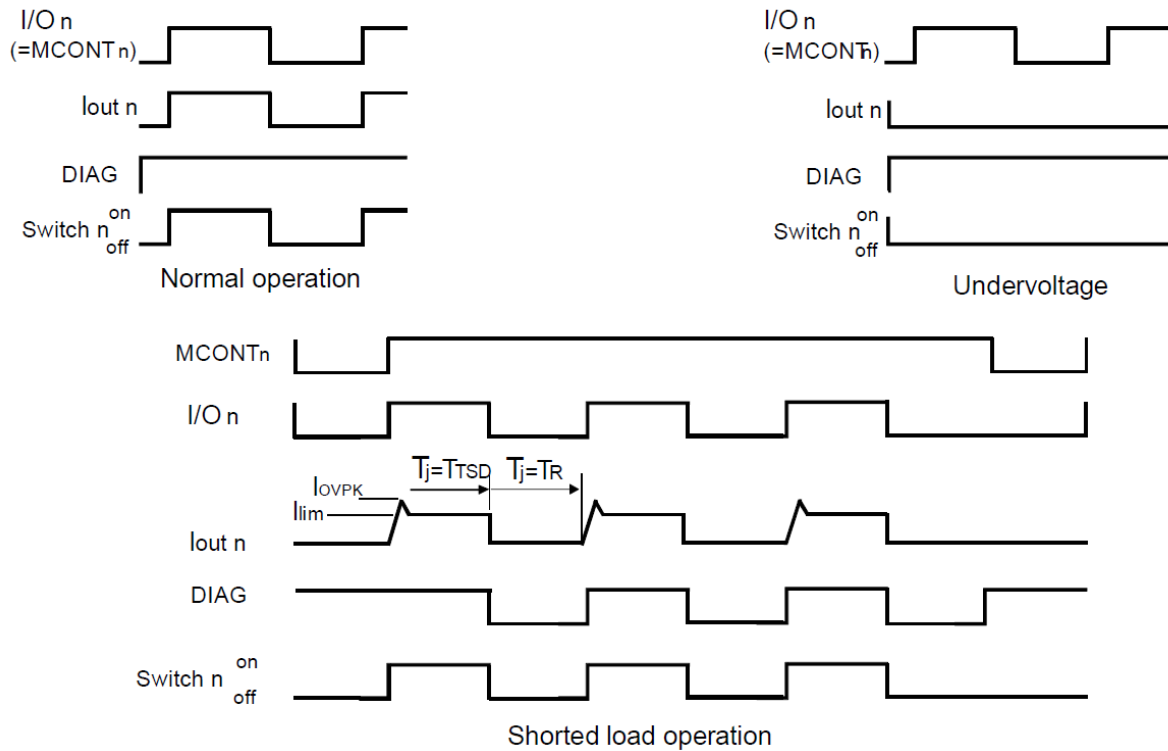
Figure 6.  $I_{LGND}$  test configuration



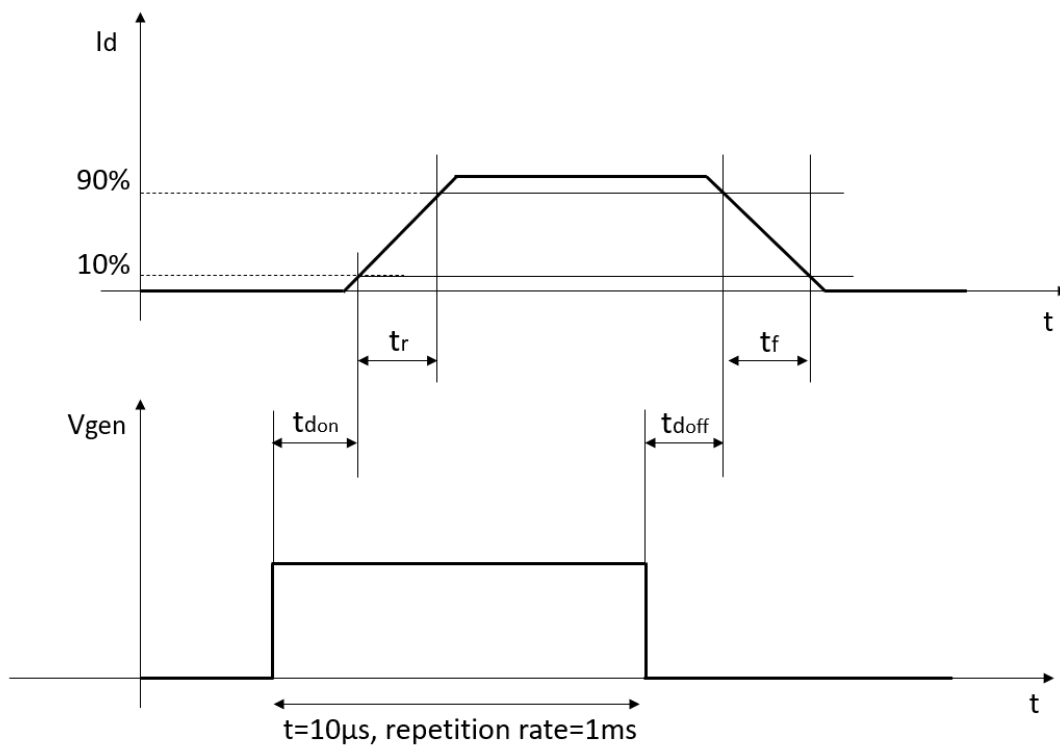


## 6 Switching time waveforms and truth table

**Figure 7. Switching waveforms**



**Figure 8. Switching parameter test conditions**

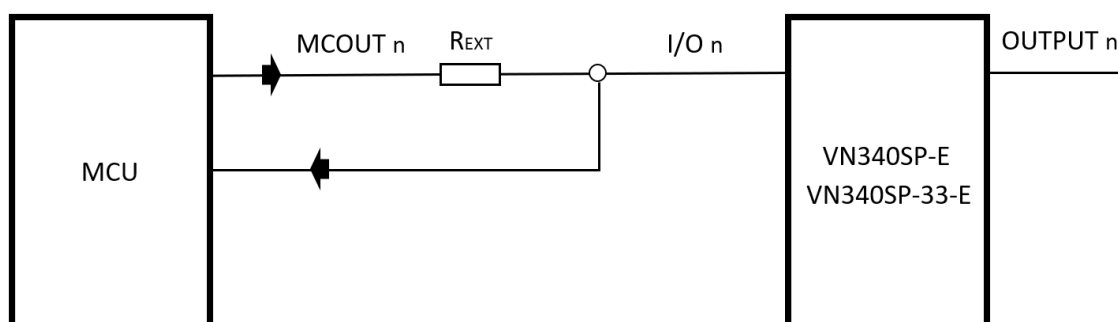


**Table 7. Truth table**

| Conditions                        | MCOUTn | I/On | OUTPUTn          | Diagnostic       |
|-----------------------------------|--------|------|------------------|------------------|
| Normal operation                  | L      | L    | L                | H                |
|                                   | H      | H    | H                | H                |
| Junction overtemperature          | L      | L    | L                | H                |
|                                   | H      | L    | L                | L                |
| Undervoltage                      | L      | L    | L                | H <sup>(1)</sup> |
|                                   | H      | H    | L                | H <sup>(1)</sup> |
| Shorted load (current limitation) | L      | L    | L                | H                |
|                                   | H      | H    | H <sup>(2)</sup> | H                |

1. DIAG pin is considered pulled-up at application voltage level

2.  $V_{OUT} = R_{LOAD} \times I_{LIM}$

**Figure 9. Driving circuit**

**Notes:**

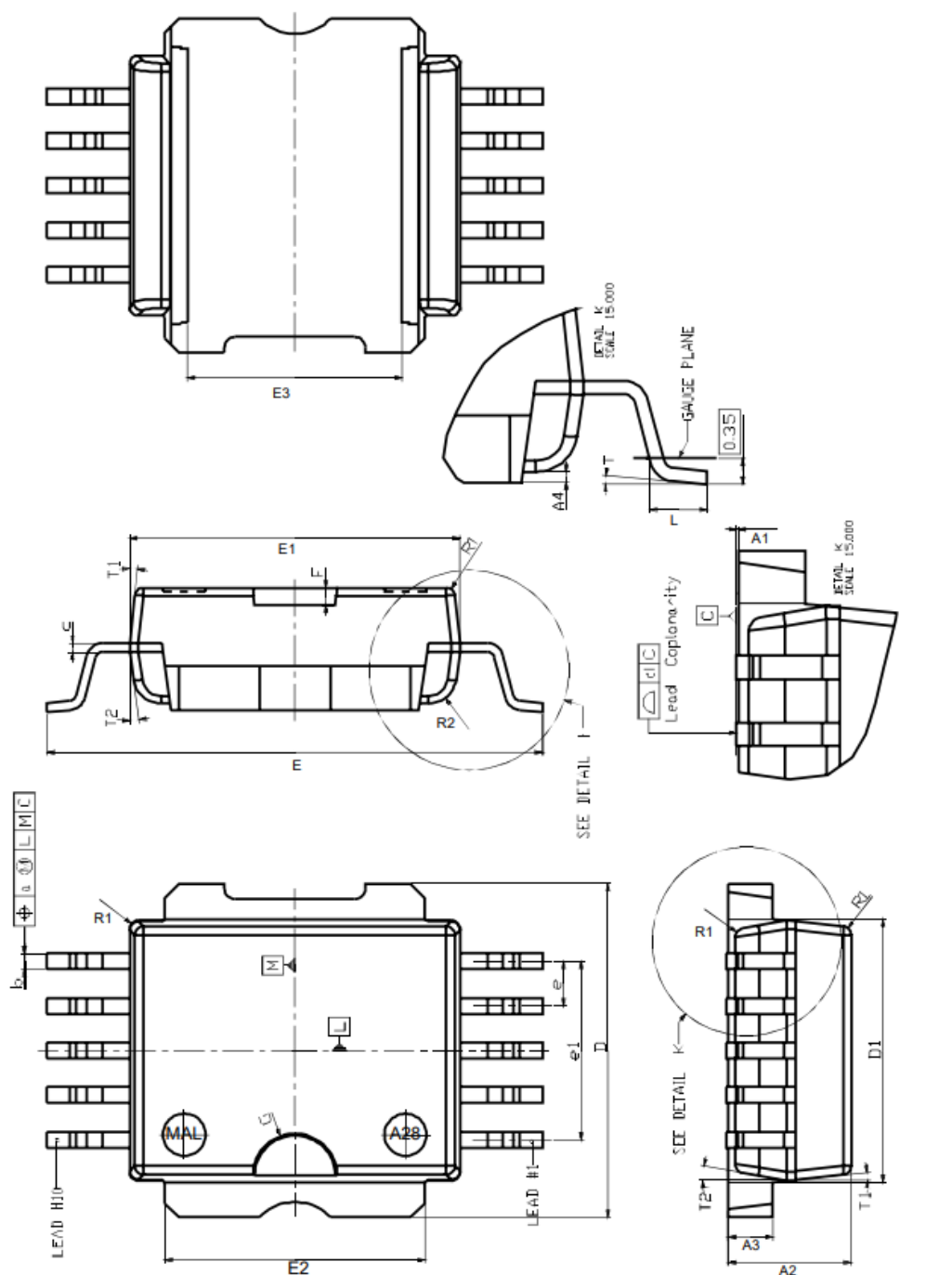
- The I/Os are internally pulled-down
- $R_{EXT}$  is for enhancement of EMI robustness

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 7.1 PowerSO-10 package information

**Figure 10. PowerSO-10 package outline**



7152835 rev.G

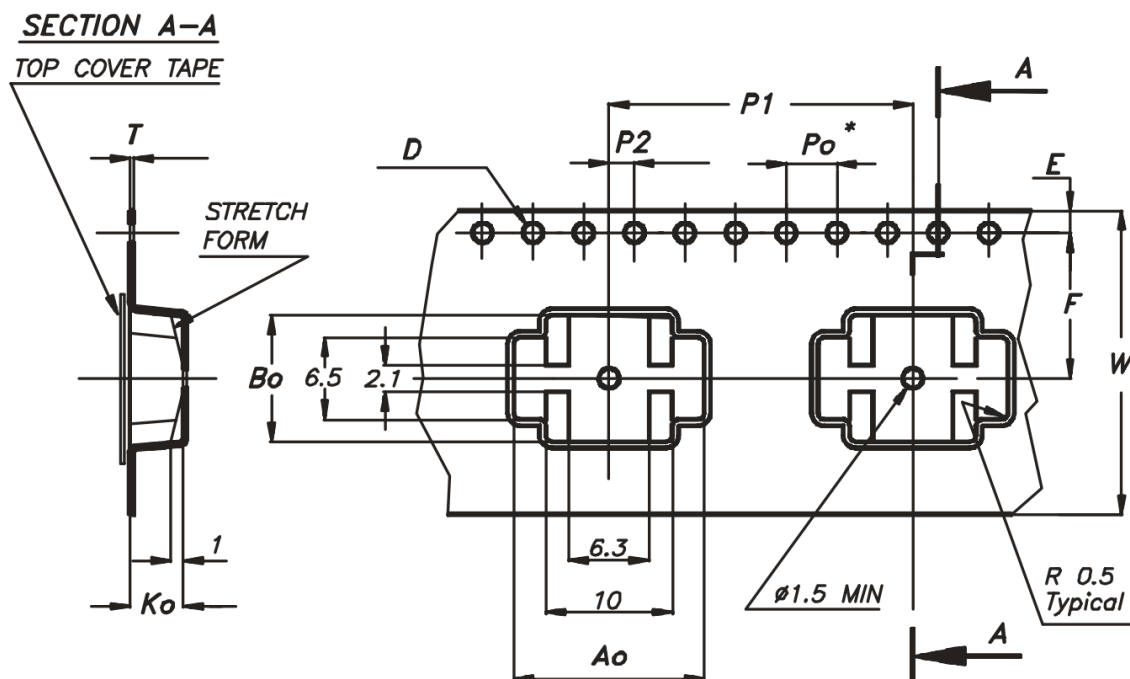
**Table 8. PowerSO-10 package mechanical data**

| Dim.              | mm    |        |       |
|-------------------|-------|--------|-------|
|                   | Min.  | Typ.   | Max.  |
| A1                | 0     | 0.05   | 0.08  |
| A2                | 3.45  | 3.5    | 3.55  |
| A3                | 1.24  | 1.28   | 1.32  |
| A4                | 0.15  | 0.2    | 0.25  |
| a                 |       | 0.2    |       |
| b                 | 0.4   | 0.45   | 0.5   |
| c                 | 0.24  | 0.27   | 0.3   |
| D                 | 9.45  | 9.52   | 9.59  |
| D1                | 7.42  | 7.5    | 7.58  |
| d                 | 0     | 0.04   | 0.09  |
| E                 | 13.9  | 14.1   | 14.3  |
| E1 <sup>(1)</sup> | 9.33  | 9.4    | 9.47  |
| E2                | 7.4   | 7.42   | 7.5   |
| E3                | 5.95  | 6.1    | 6.25  |
| e                 | 1.22  | 1.27   | 1.32  |
| e1                |       | 5.08   |       |
| F                 |       | 0.5    |       |
| G                 |       | 1.2    |       |
| L                 | 0.85  | 1      | 1.1   |
| R1                |       |        | 0.25  |
| R2                |       | 0.8    |       |
| T                 | 3 deg | 5 deg  | 7 deg |
| T1                |       | 6 deg  |       |
| T2                |       | 10 deg |       |

1. Resin protrusions are not included (max. value 0.15 mm per side)

## 7.2 PowerSO-10 packing information

Figure 11. PowerSO-10 career tape outline

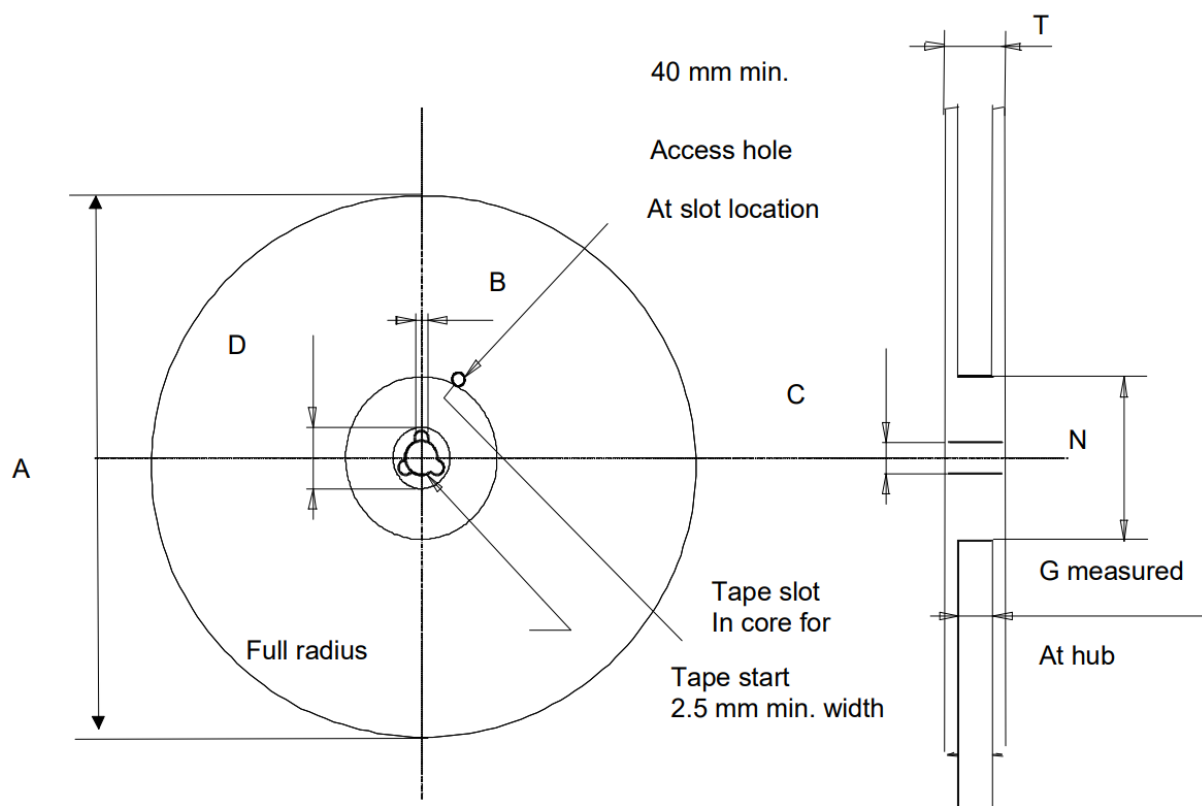


Note: Drawing is not in scale

Table 9. PowerSO-10 career tape dimension mechanical data

| Dim. | mm    |      |      |
|------|-------|------|------|
|      | Min.  | Typ. | Max. |
| A0   | 14.9  | 15.0 | 15.1 |
| B0   | 9.9   | 10.0 | 10.1 |
| K0   | 4.15  | 4.25 | 4.35 |
| F    | 11.4  | 11.5 | 11.6 |
| E    | 1.65  | 1.75 | 1.85 |
| W    | 23.7  | 24.0 | 24.3 |
| P2   | 1.9   | 2.0  | 2.1  |
| P0   | 3.9   | 4.0  | 4.1  |
| P1   | 23.9  | 24.0 | 24.1 |
| T    | 0.025 | 0.30 | 0.35 |
| D(Ø) | 1.50  | 1.55 | 1.60 |

Note: 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm

**Figure 12. PowerSO-10 reel outline**


*Note:* Drawing is not in scale

**Table 10. PowerSO-10 reel dimension mechanical data**

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    |      |      | 330  |
| B    | 1.5  |      |      |
| C    | 12.8 | 13   | 13.2 |
| D    | 20.2 |      |      |
| N    | 60   |      |      |
| G    | 23.7 | 24.4 |      |
| T    |      |      | 30.4 |

*Note:* 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm

**Table 11. PowerSO-10 base and bulk quantity**

| Base quantity | Bulk quantity |
|---------------|---------------|
| 600           | 600           |

## 8 Ordering information

**Table 12. Ordering information**

| Part Number    | Package    | Packaging     |
|----------------|------------|---------------|
| VN340SP-E      | PowerSO-10 | Tube          |
| VN340SPTR-E    |            | Tape and reel |
| VN340SP-33-E   |            | Tube          |
| VN340SPTR-33-E |            | Tape and reel |

## Revision history

**Table 13. Document revision history**

| Date        | Revision | Changes                                              |
|-------------|----------|------------------------------------------------------|
| 05-Sep-2005 | 1        | Initial release.                                     |
| 19-Mar-2007 | 2        | Document reformatted, typo in note 1.                |
| 22-Aug-2008 | 3        | Updated table 9.                                     |
| 07-Sep-2015 | 4        | Updated the table of absolute maximum ratings.       |
| 1-Sep-2022  | 5        | Merged VN340SP-33 and VN340SP DS; some minor changes |



## Contents

|          |                                                 |           |
|----------|-------------------------------------------------|-----------|
| <b>1</b> | <b>Block diagram</b>                            | <b>2</b>  |
| <b>2</b> | <b>Pin connection</b>                           | <b>3</b>  |
| <b>3</b> | <b>Maximum ratings</b>                          | <b>4</b>  |
| <b>4</b> | <b>Electrical characteristics</b>               | <b>5</b>  |
| <b>5</b> | <b>Test circuits</b>                            | <b>7</b>  |
| <b>6</b> | <b>Switching time waveforms and truth table</b> | <b>9</b>  |
| <b>7</b> | <b>Package information</b>                      | <b>11</b> |
| 7.1      | PowerSO-10 package information                  | 11        |
| 7.2      | PowerSO-10 packing information                  | 13        |
| <b>8</b> | <b>Ordering information</b>                     | <b>15</b> |
|          | <b>Revision history</b>                         | <b>16</b> |
|          | <b>List of tables</b>                           | <b>18</b> |
|          | <b>List of figures</b>                          | <b>19</b> |

## List of tables

|                  |                                                                       |    |
|------------------|-----------------------------------------------------------------------|----|
| <b>Table 1.</b>  | Absolute maximum ratings . . . . .                                    | 4  |
| <b>Table 2.</b>  | Thermal data . . . . .                                                | 4  |
| <b>Table 3.</b>  | Power section . . . . .                                               | 5  |
| <b>Table 4.</b>  | Switching ( $V_{CC} = 24\text{ V}$ , $T_J = 25\text{ °C}$ ) . . . . . | 5  |
| <b>Table 5.</b>  | Logic inputs . . . . .                                                | 5  |
| <b>Table 6.</b>  | Protection and diagnostic . . . . .                                   | 6  |
| <b>Table 7.</b>  | Truth table . . . . .                                                 | 10 |
| <b>Table 8.</b>  | PowerSO-10 package mechanical data . . . . .                          | 12 |
| <b>Table 9.</b>  | PowerSO-10 carrier tape dimension mechanical data . . . . .           | 13 |
| <b>Table 10.</b> | PowerSO-10 reel dimension mechanical data . . . . .                   | 14 |
| <b>Table 11.</b> | PowerSO-10 base and bulk quantity . . . . .                           | 14 |
| <b>Table 12.</b> | Ordering information . . . . .                                        | 15 |
| <b>Table 13.</b> | Document revision history . . . . .                                   | 16 |

## List of figures

|                   |                                                |    |
|-------------------|------------------------------------------------|----|
| <b>Figure 1.</b>  | Block diagram . . . . .                        | 2  |
| <b>Figure 2.</b>  | Connection diagram (top view) . . . . .        | 3  |
| <b>Figure 3.</b>  | Current and voltage conventions . . . . .      | 3  |
| <b>Figure 4.</b>  | Avalanche energy test circuit . . . . .        | 7  |
| <b>Figure 5.</b>  | Peak short-circuit test diagram . . . . .      | 7  |
| <b>Figure 6.</b>  | I <sub>LGND</sub> test configuration . . . . . | 8  |
| <b>Figure 7.</b>  | Switching waveforms . . . . .                  | 9  |
| <b>Figure 8.</b>  | Switching parameter test conditions . . . . .  | 9  |
| <b>Figure 9.</b>  | Driving circuit . . . . .                      | 10 |
| <b>Figure 10.</b> | PowerSO-10 package outline . . . . .           | 11 |
| <b>Figure 11.</b> | PowerSO-10 carrier tape outline . . . . .      | 13 |
| <b>Figure 12.</b> | PowerSO-10 reel outline . . . . .              | 14 |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved