CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX865A
Telecom Signalling Device

D/865A/5 May 2012

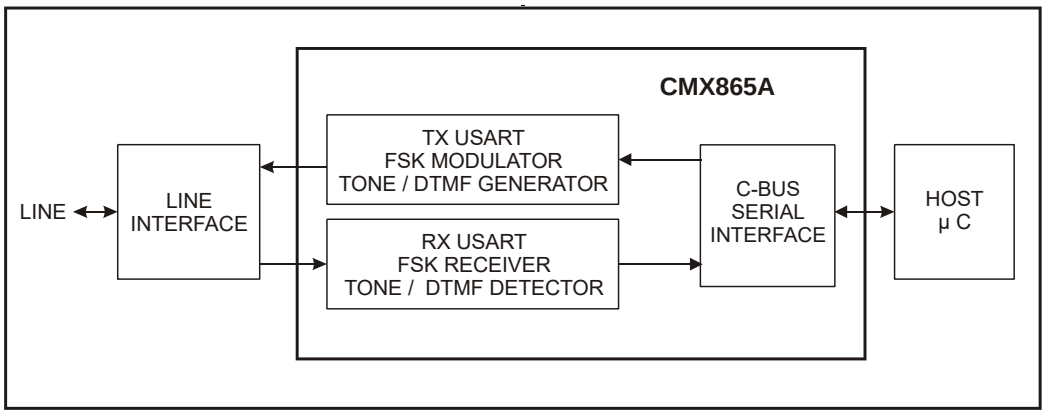
CMX865A – DTMF CODEC AND TELECOM SIGNALLING COMBO

Features

- **V.23 1200/75, 1200/1200, 75, 1200 bps FSK**
- **Bell 202 1200/150, 1200/1200, 150, 1200 bps FSK**
- **V.21 or Bell 103 300/300 bps FSK**
- **Low Voice Falsing DTMF Decoder**
- **DTMF/Tones Transmit and Receive**
- **Low Power - High Performance**

Applications

- **Wireless Local Loops**
- **SMS Phones**
- **Security Systems**
- **Remote Utility Meter Reading**
- **Industrial Control Systems**
- **Pay-Phones**
- **Set-Top Boxes**



1. Brief Description

The CMX865A is a multi-standard modem for use in Wireless Local Loop, Short Message Service telephone based information and telemetry systems. Flexible line driver, hybrid and receiver circuits are integrated on chip, requiring only passive external components to build a 2 or 4-wire line interface.

A high-quality DTMF decoder with excellent immunity to falsing on voice and a standard DTMF encoder are included. Alternatively, these blocks can be used to transmit and detect user-specific, programmed single and dual-tone signals, simple melodies, call progress signals or modem calling and answering tones.

Host control and data transfer is via a high-speed serial bus that operates in normal and Powersave modes and which is compatible with most simple types of µC serial interface. An embedded USART allows multi-format asynchronous data and unformatted synchronous data to be received or transmitted as 8-bit bytes.

The CMX865A operates from a single 3.0V to 3.6V supply over a temperature range of -40°C to +85°C and is available in 16-pin SOIC (D4) and 16-pin TSSOP (E4) packages.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

2. Block Diagram

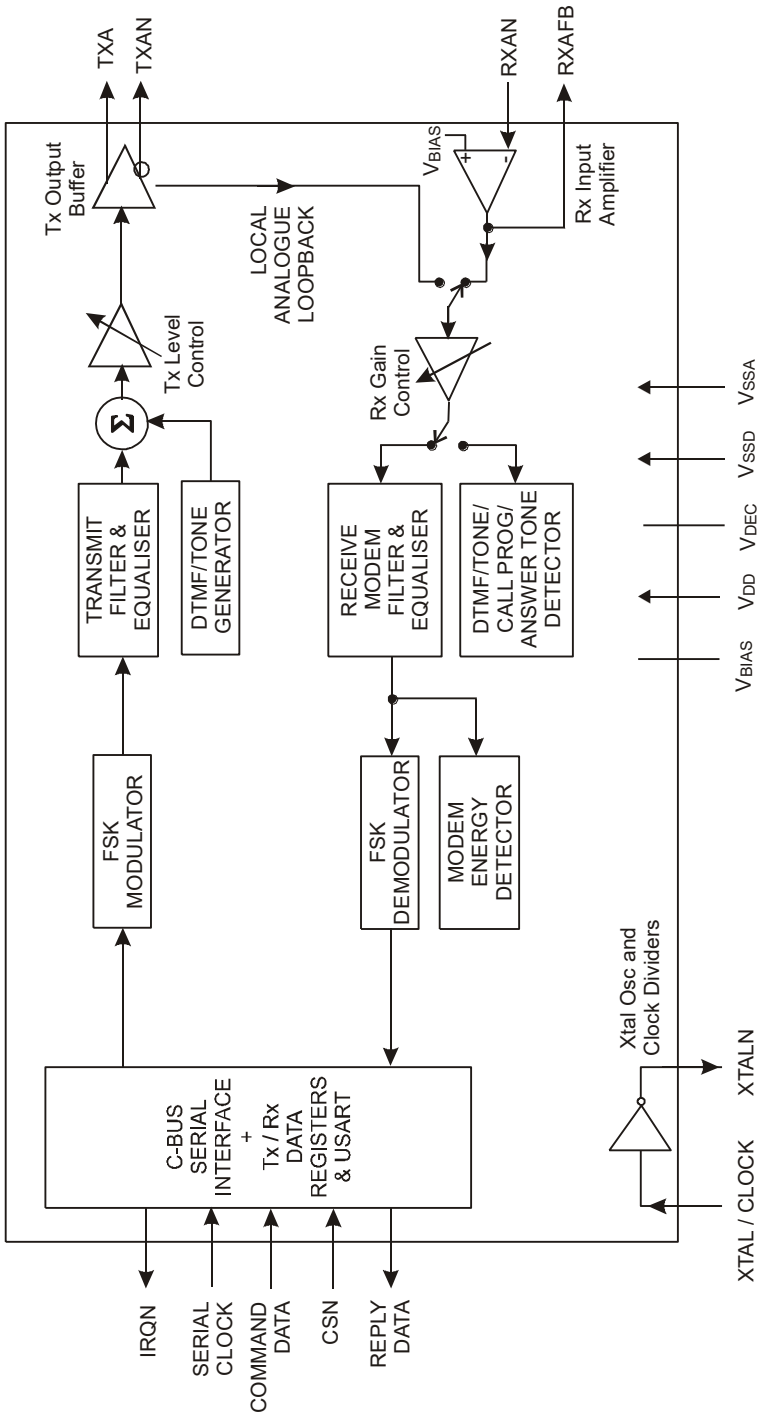


Figure 1 Block Diagram

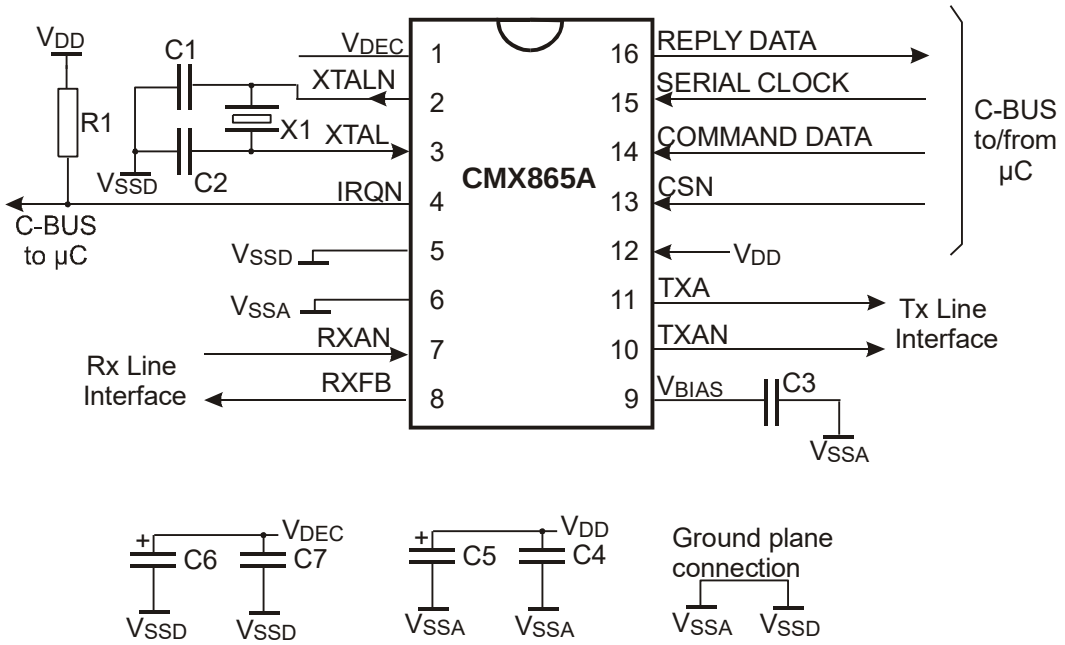
3. Signal List

CMX865A (D4 and E4)	Signal		Description
Pin No.	**Name**	**Type**	
1	V_{DEC}	Power	Internally generated 2.5V supply voltage. Must be decoupled to V_{SSD} by capacitors mounted close to the device pins. No other connections allowed.
2	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
3	XTAL/CLOCK	I/P	The input to the oscillator inverter from the Xtal circuit or external clock source.
4	IRQN	O/P	A 'wire-ORable' output for connection to a μC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pull-up resistor is required i.e. R1 of Figure 2.
5	V_{SSD}	Power	The digital negative supply rail (ground).
6	V_{SSA}	Power	The analogue negative supply rail (ground).
7	RXAN	I/P	The inverting input to the Rx Input Amplifier
8	RXAFB	O/P	The output of the Rx Input Amplifier.
9	V_{BIAS}	O/P	Internally generated bias voltage of approximately V_{DD} /2, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to V_{SS}. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	TXAN	O/P	The inverted output of the Tx Output Buffer.
11	TXA	O/P	The non-inverted output of the Tx Output Buffer.
12	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage.
13	CSN	I/P	The C-BUS chip select input from the μC.
14	COMMAND DATA	I/P	The C-BUS serial data input from the μC.
15	SERIAL CLOCK	I/P	The C-BUS serial clock input from the μC.
16	REPLY DATA	T/S	A 3-state C-BUS serial data output to the μC. This output is high impedance when not sending data to the μC.

Notes:

I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

4. External Components



R1	68kΩ	C1, C2	22pF
X1	6.144MHz (± 300ppm)	C3, C4, C7	100nF
		C5, C6	10uF

Resistors ±5%, capacitors ±20% unless otherwise stated

Figure 2 Recommended External Components for a Typical Application

This device is capable of detecting and decoding small amplitude signals. To achieve this, V_{DD}, V_{DEC} and V_{BIAS} should be decoupled close to the package and the receive path protected from extraneous in-band signals.

It is recommended that the printed circuit board is laid out with low impedance analogue and digital ground planes. The analogue ground plane should be a solid area under the analogue section of the device defined by pins 6 – 11, plus associated external components. The digital ground plane should be a solid area under the digital section of the device defined by pins 1 – 5 and 13 –16, plus associated external components. The two ground planes should be connected together at a suitable point and connected into the board ground.

The V_{SS} connections to the Xtal oscillator capacitors C1 and C2 should also be low impedance and preferably be part of the digital V_{SS} ground plane to ensure reliable start up of the oscillator.

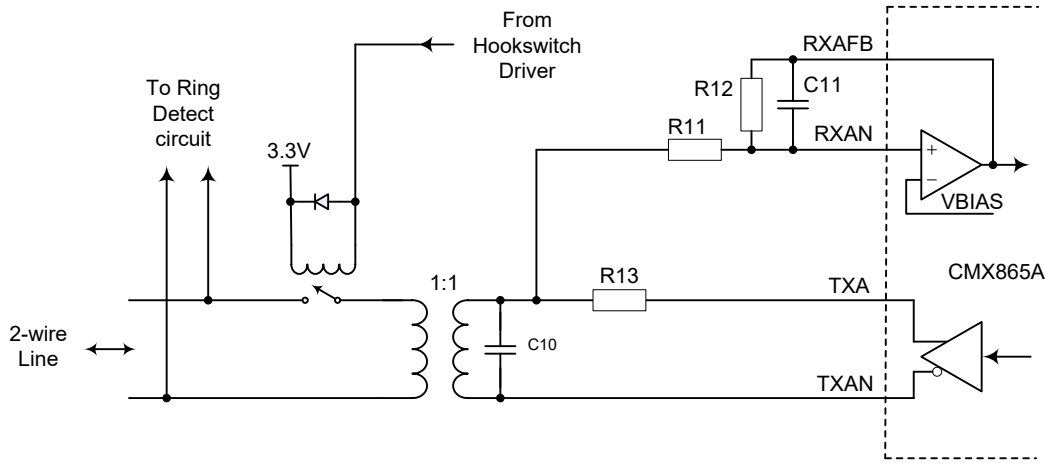
For best results, an Xtal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak-to-peak. To obtain Xtal oscillator design assistance, please consult your Xtal manufacturer.

4.1. Line Interface (DAA)

A line interface circuit is needed to provide dc isolation and to terminate the line. Typical interface circuits are described below.

4.1.1. 2-Wire Line Interface

Figure 3 shows a simplified interface for use with a 600Ω 2-wire line. The complex line termination is provided by R13 and C10, high frequency noise is attenuated by C10 and C11, while R11 and R12 set the receive signal level into the modem. For clarity the 2-wire line protection circuits have not been shown.



R11	See text	C10	33nF
R12	100kΩ	C11	100pF
R13	600Ω nominal, but see text		

Resistors ±5%, capacitors ±20%

Figure 3 Typical 2-Wire Line Interface Circuit

Resistor R13 is used to match the ac impedance of the interface to the line. With an ideal transformer this resistor would be equal to the desired impedance (e.g. 600Ω); however in practice with a real transformer, R13 should be set such that the interface as a whole presents the desired impedance. Line transformer manufacturers normally provide guidance in this regard.

The transmit line signal level is determined by the voltage swing between the TXA and TXAN pins, less 6dB due to the line termination and less the loss in the line coupling transformer.

Allowing for 1dB loss in the transformer, then with the Tx Mode Register set for a Tx Level Control gain of 0dB the nominal transmit line levels will be:

	V_{DD} = 3.3V
Tx modem modes	-9.2dBm
Single tone transmit mode	-9.2dBm
DTMF transmit mode	-5.2 and –7.2 dBm

For a line impedance of 600Ω, 0dBm = 775mVrms. See also section 7.1.3.

In the receive direction, the signal detection thresholds within the CMX865A are proportional to V_{DD} and are affected by the Rx Gain Control gain setting in the Rx Mode Register. The signal level into the CMX865A is affected by the line coupling transformer loss and the values of R11 and R12 of Figure 3.

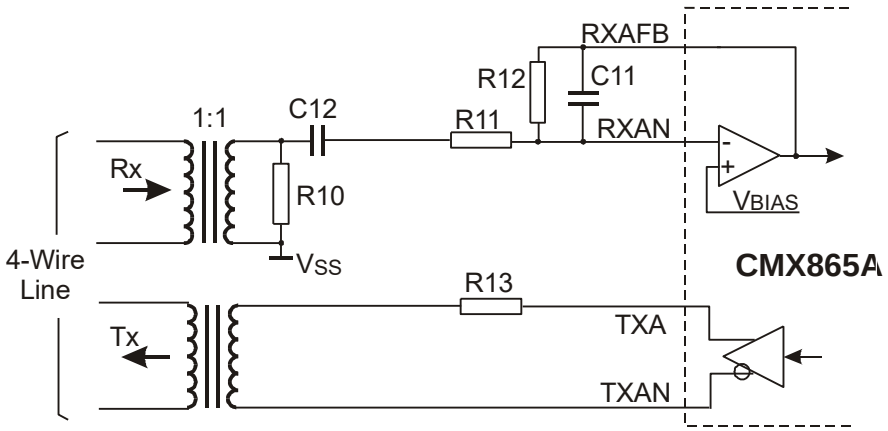
Assuming 1dB transformer loss, the Rx Gain Control programmed to 0dB and R12 = 100kΩ, then for correct operation (see section 7.1.3) the value of R11 should be equal to 500 / V_{DD} kΩ i.e. 150kΩ at 3.3V.

For best Rx performance it is recommended that the transformer coupling arrangement should provide at least 7dB trans-hybrid loss. This is achieved by minimising the amount of the transmitted signal presented to the receiver as measured at RXAFB.

4.1.2. 4-Wire Line Interface

Figure 4 shows a simplified interface for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R13, the values of which are dependent on the choice of transformer: line transformer manufacturers normally provide guidance in this regard. High frequency noise is attenuated by C11 while R11 and R12 set the receive signal level into the modem.

Transmit and receive line level settings and the value of R11 are as for the 2-wire circuit.



R10, 13	See text	C11	100pF
R11	See text	C12	33nF
R12	100kΩ		

Resistors ±5%, capacitors ±20%

Figure 4 Typical 4-Wire Line Interface Circuit

4.1.3. Wireless Local Loop Interface

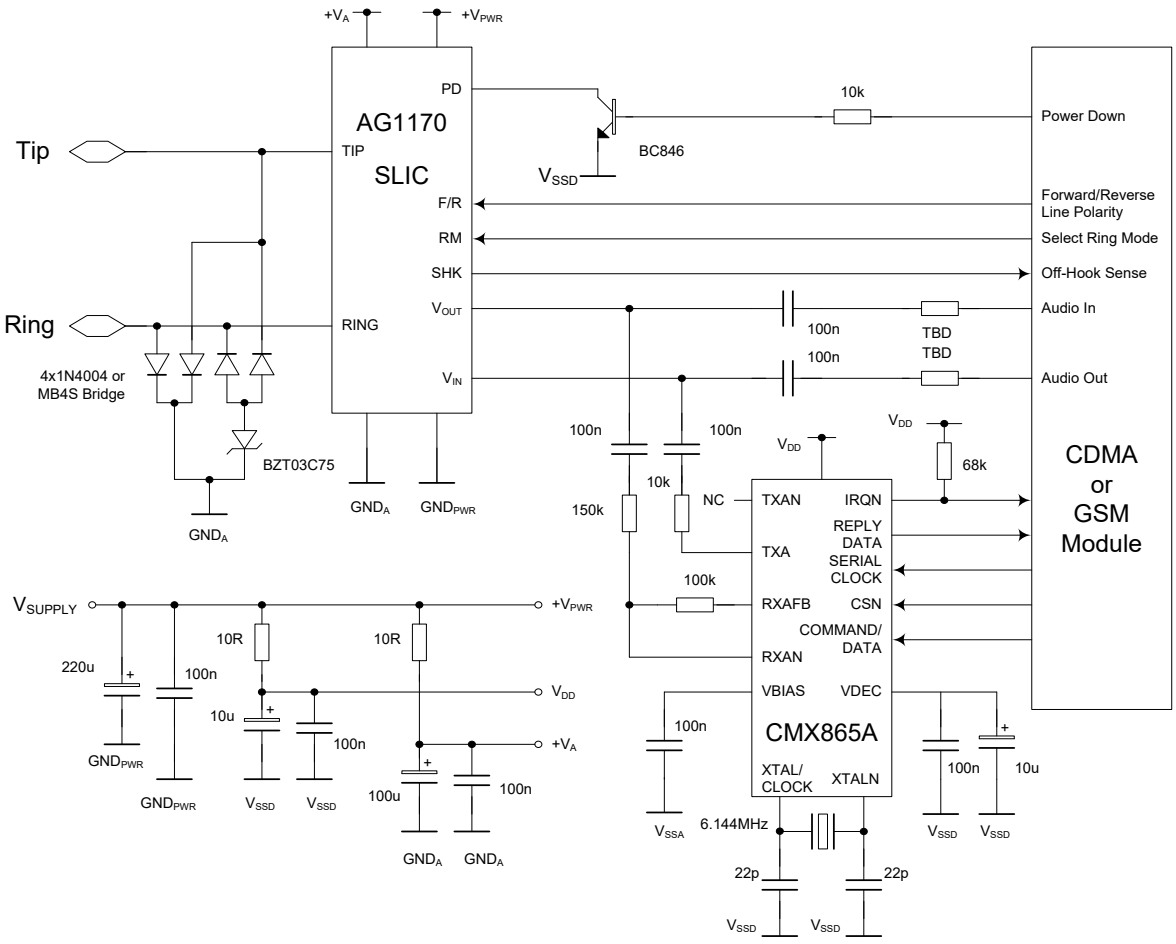


Figure 5 The CMX865A in a Wireless Local Loop Application

The above circuit is a simplified representation of a typical design. In practice, the actual circuit design and external components should be implemented with due regard to the datasheets of the SLIC and wireless module. Particular emphasis should be given to the design of the power supply decoupling arrangement in order to minimise the effects of noise currents between the ICs.

5. General Description

The CMX865A transmit and receive operating modes are independently programmable.

The transmit mode can be set to any one of the following:

- V.21 modem. 300bps FSK (Frequency Shift Keying).
- Bell 103 modem. 300bps FSK.
- V.23 modem. 1200 or 75 bps FSK.
- Bell 202 modem. 1200 or 150 bps FSK.
- DTMF transmit.
- Single tone transmit (from a range of modem calling, answer and other tone frequencies).
- User programmed tone or tone pair transmit (programmable frequencies and levels).
- Disabled.

The receive mode can be set to any one of the following:

- V.21 modem. 300bps FSK.
- Bell 103 modem. 300bps FSK.
- V.23 modem. 1200 or 75 bps FSK.
- Bell 202 modem. 1200 or 150 bps FSK.
- DTMF decode.
- 2100Hz and 2225Hz answer tone detect.
- Call progress signal detect.
- User programmed tone or tone pair detect.
- Disabled.

The CMX865A may also be set into a powersave mode which disables all circuitry except for the C-BUS interface.

5.1. TXA/TXAN Differential Output

With a transformer-based interface, a differential output is required to provide sufficient power to the line from a 3.3V supply. Active interfaces such as SLICS and COICS have high-impedance I/O so can be driven single-ended from either TXA or TXAN. The states of TXA and TXAN are automatically set according to the selected operating mode.

CMX865A Mode	Transmit mode enabled ($E1 b15-12 ≠ 0000)	Transmit mode disabled ($E1 b15-12 = 0000)
Receive mode enabled ($E2 b15-12 ≠ 0000)	Vdd/2	Vdd/2
Receive mode disabled ($E2 b15-12 = 0000)	Vdd/2	High-impedance

Table 1 TXA/TXAN state with selected operating mode

This enables the correct bias conditions to be applied to a transformer-based interface for both transmitting and receiving modes. When both transmit and receive modes are disabled, the transmit output pins go to a high-impedance state and the output amplifiers are power saved. The high-impedance state is useful to allow other devices to share the line interface using only passive components. See Section 6.2.

Switches are provided on TXA and TXAN to allow these pins to assume a high-impedance state. For normal modem operation TXA and TXAN should always be be set to "output connected", General Control register $E0 b15-b14 = 00. The ‘output disconnected’ mode is provided to improve reception of caller-ID signals when using a transformer based design. See Section 5.11.2.

5.2. Tx USART

A flexible Tx USART is provided for all modem modes. It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous Data.

In both Synchronous Data and Start-Stop modes the data to be transmitted is written by the µC into the 8-bit C-BUS Tx Data Register from which it is transferred to the Tx Data Buffer.

If Synchronous Data mode has been selected the 8 data bits in the Tx Data Buffer are transmitted serially, b0 being sent first.

In Start-Stop mode a single Start bit is transmitted, followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - b0 first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the Tx Data Register.

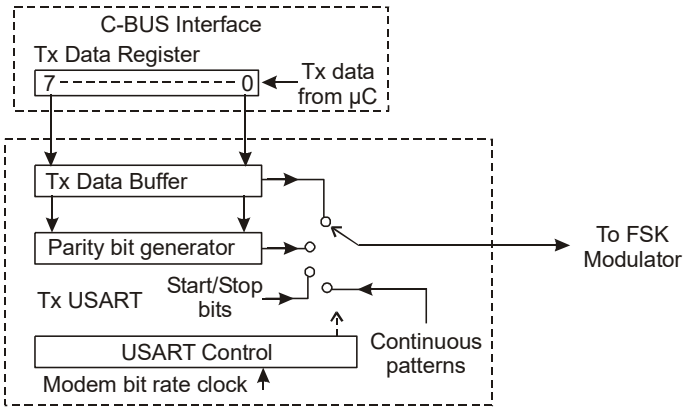


Figure 6 Tx USART

Every time the contents of the C-BUS Tx Data Register are transferred to the Tx Data Buffer the Tx Data Ready flag bit of the Status Register is set to 1 to indicate that a new value should be loaded into the C-BUS Tx Data Register. This flag bit is cleared to 0 when a new value is loaded into the Tx Data Register.

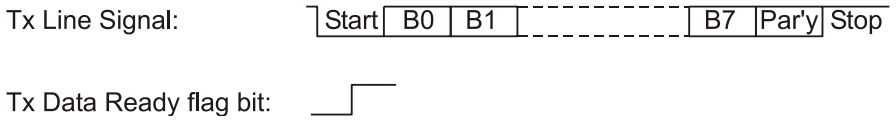


Figure 7 Tx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If a new value is not loaded into the Tx Data Register in time for the next Tx Data Register to Tx Data Buffer transfer then the Status Register Tx Data Underflow bit will be set to 1. In this event the contents of the Tx Data Buffer will be re-transmitted if Synchronous Data mode has been selected, or if the Tx modem is in Start-Stop mode then a continuous Stop signal (1) will be transmitted until a new value is loaded into the Tx Data Register.

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the XTAL frequency accuracy.

5.3. FSK Modulator

Serial data from the USART is fed to the FSK modulator if a V.21, V.23, Bell 103 or Bell 202 mode has been selected.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of the current transmit data bit.

5.4. Tx Filter and Equaliser

The FSK modulator output signal is fed through the Transmit Filter which limits the out-of-band signal energy to acceptable limits. In 1200bps modem modes this block includes a fixed compromise line equaliser which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equaliser may be enabled or disabled by b10 of the General Control Register. The amount of Tx equalisation provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.

5.5. DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals (with programmable twist) or single or dual frequency tones.

5.6. Tx Level Control and Output Buffer

The outputs (if present) of the Transmit Filter and DTMF/Tone Generator are passed through the programmable Tx Level Control and Tx Output Buffer to the pins TXA and TXAN. The Tx Output Buffer has symmetrical outputs to provide sufficient line voltage swing at low values of V_{DD} and to reduce harmonic distortion of the signal.

5.7. Rx DTMF/Tones Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF / Tones / Call Progress / Answer Tone detector. The user may select any one of four separate detectors:

The DTMF detector detects standard DTMF signals. A valid DTMF signal will set b5 of the Status Register to 1 for as long as the signal is detected.

The programmable tone pair detector includes two separate tone detectors (see Figure 17). The first detector will set to 1 b6 of the Status Register for as long as a valid signal is detected, the second detector sets b7 to 1, and b10 of the Status Register will be set to 1 when both tones are detected.

The call progress detector measures the amplitude of the signal at the output of a 275 - 665 Hz bandpass filter and sets b10 of the Status Register to 1 when the signal level exceeds the measurement threshold.

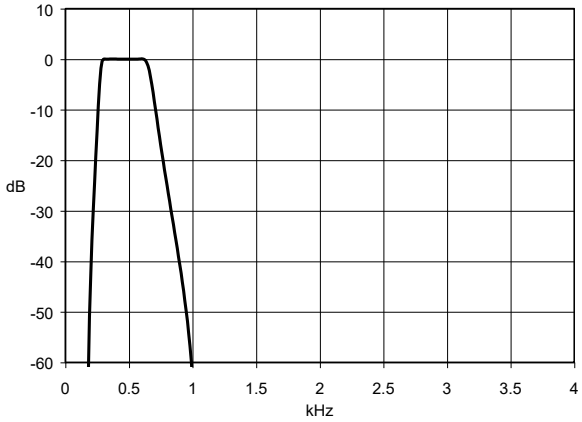


Figure 8 Response of Call Progress Filter

The Answer Tone detector measures both amplitude and frequency of the received signal and sets b6 or b7 of the Status Register to 1 when a valid 2225Hz or 2100Hz signal is received.

5.8. Rx Modem Filtering and Demodulation

When the receive part of the CMX865A is operating as a modem, the received signal is fed to a bandpass filter to attenuate unwanted signals and to provide fixed compromise line equalisation for 1200bps modem modes. The characteristics of the bandpass filter and equaliser are determined by the chosen receive modem type and frequency band. The line equaliser may be enabled or disabled by b10 of the General Control Register and compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1.

The responses of these filters, including the line equaliser and the effect of external components used in Figure 3 and Figure 4, are shown in Figure 9 to Figure 11:

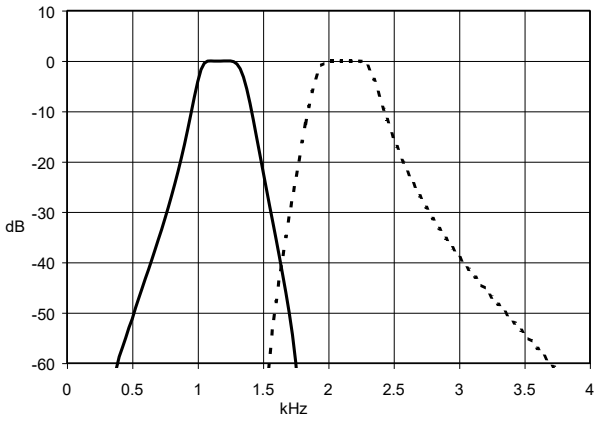


Figure 9 Bell 103 Rx Filters

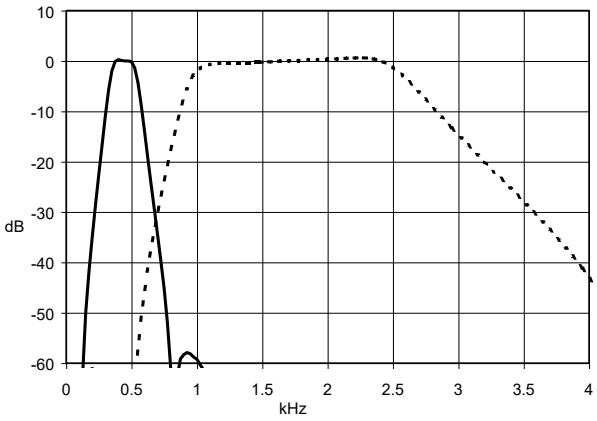


Figure 10 V.23/Bell 202 Rx Filters

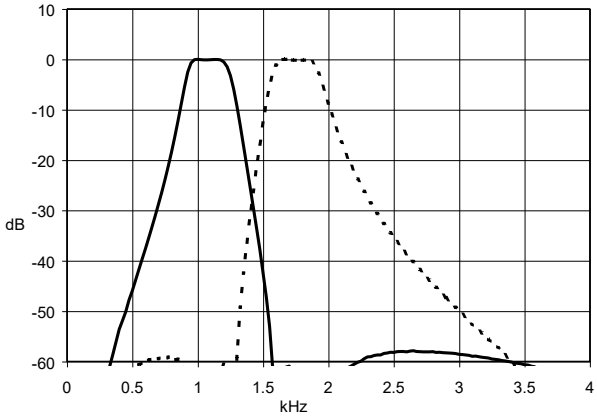


Figure 11 V.21 Rx Filters

The signal level at the output of the Receive Modem Filter and Equaliser is measured in the Modem Energy Detector block, compared to a threshold value, and the result controls b10 of the Status Register.

The output of the Receive Modem Filter and Equaliser is also fed to the FSK demodulator.

The FSK demodulator recognises individual frequencies as representing received 1 or 0 data bits:

The FSK demodulator produces a serial data bit stream which is fed to the Rx pattern detector and USART block, see Figure 12.

The demodulator input is also monitored for continuous alternating 1s and 0s.

5.9. Rx Modem Pattern Detectors

See Figure 12.

The 1010.. pattern detector will set b9 of the Status Register when 32 bits of alternating 1s and 0s have been detected.

The ‘Continuous 0s’ detector sets b8 of the Status Register when 32 consecutive 0s have been detected.

The ‘Continuous 1s’ detector sets b7 of the Status Register when 32 consecutive 1s have been detected.

All of these pattern detectors will hold the ‘detect’ output for 12 bit times after the end of the detected pattern unless the received bit rate or operating mode is changed, in which case the detectors are reset within 2 msec.

5.10. Rx Data Register and USART

A flexible Rx USART is provided for all modem modes. It can be programmed to treat the received data bit stream as Synchronous data or as Start-Stop characters.

In Synchronous mode the received data bits are all fed into the Rx Data Buffer which is copied into the C-BUS Rx Data Register after every 8 bits.

In Start-Stop mode the USART Control logic looks for the start of each character, then feeds only the required number of data bits (not parity) into the Rx Data Buffer. The parity bit (if used) and the presence of a Stop bit are then checked and the data bits in the Rx Data Buffer copied to the C-BUS Rx Data Register.

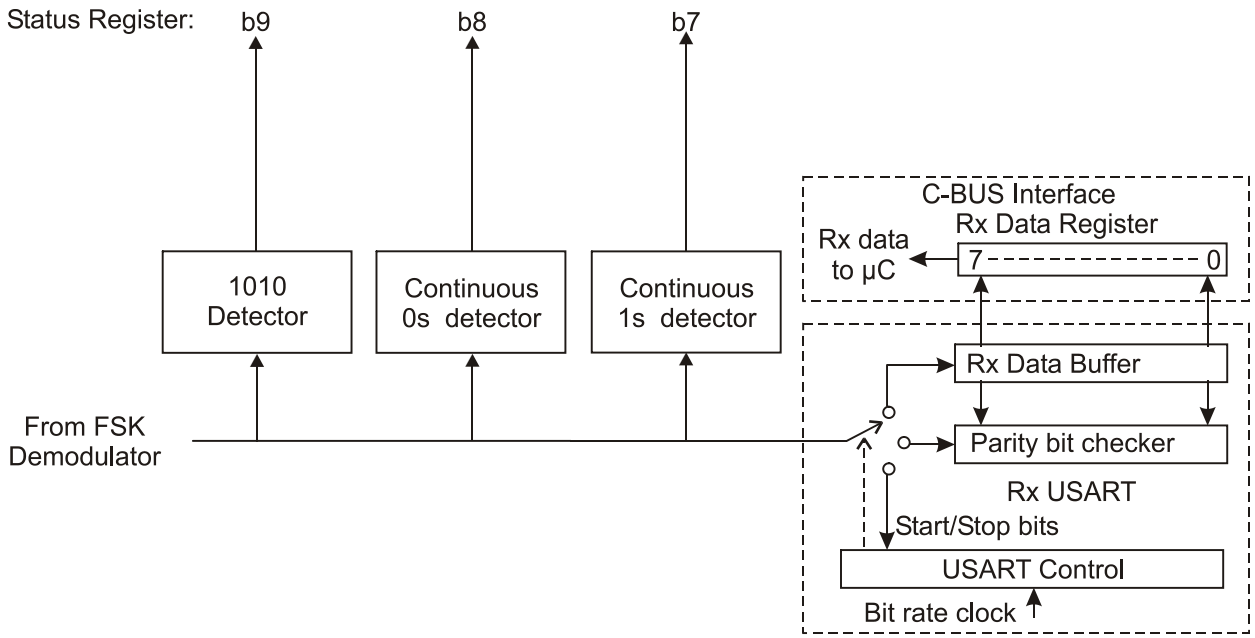


Figure 12 Rx Modem Data Paths

Whenever a new character is copied into the C-BUS Rx Data Register, the Rx Data Ready flag bit of the Status Register is set to ‘1’ to prompt the µC to read the new data and, in Start-Stop mode, the Even Rx Parity flag bit of the Status Register is updated.

In Start-Stop mode, if the Stop bit is missing (received as a ‘0’ instead of a ‘1’) the received character will still be placed into the Rx Data Register and the Rx Data Ready flag bit set, but the Status Register Rx

Framing Error bit will also be set to '1' and the USART will re-synchronise onto the next '1' – '0' (Stop – Start) transition. The Rx Framing Error bit will remain set until the next character has been received.

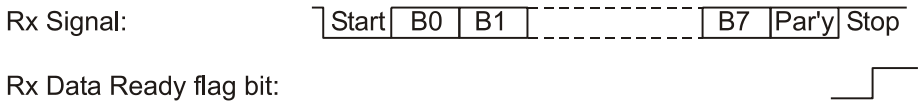


Figure 13 Rx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If the µC has not read the previous data from the Rx Data Register by the time that new data is copied to it from the Rx Data Buffer then the Rx Data Overflow flag bit of the Status Register will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are cleared to 0 when the Rx Data Register is read by the µC.

A received character which has all bits '0', including the Stop and any Parity bits, will always cause the Rx Framing Error bit to be set to 1 and the USART to re-synchronise onto the next 1 – 0 transition.

5.11. C-BUS Interface

This block provides for the transfer of data and control or status information between the CMX865A's internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data bytes sent from the µC to be written into one of the CMX865A's Write Only Registers, or one or more bytes of data read out from one of the CMX865A's Read Only Registers, as illustrated in Figure 14.

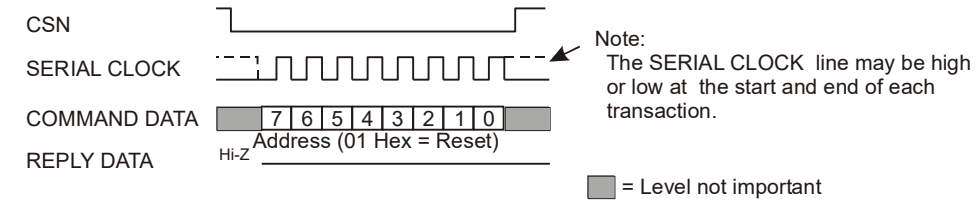
Data sent from the µC on the Command Data line is clocked into the CMX865A on the rising edge of the Serial Clock input. Reply Data sent from the CMX865A to the µC is valid when the Serial Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 23 gives detailed C-BUS timing requirements.

The following C-BUS addresses and registers are used by the CMX865A:

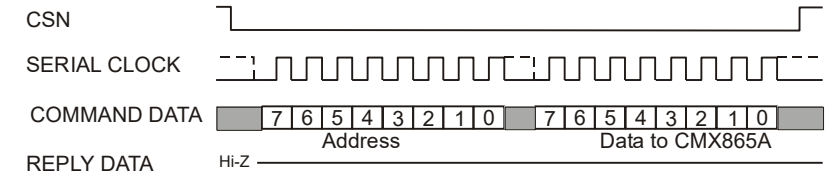
General Reset Command (address only, no data).	Address $01
General Control Register, 16-bit write only.	Address $E0
Transmit Mode Register, 16-bit write-only.	Address $E1
Receive Mode Register, 16-bit write-only.	Address $E2
Transmit Data Register, 8-bit write only.	Address $E3
Receive Data Register, 8-bit read-only.	Address $E5
Status Register, 16-bit read-only.	Address $E6
Programming Register, 16-bit write-only.	Address $E8

Note: The C-BUS addresses $E9, $EA and $EB are allocated for production testing and should not be accessed in normal operation.

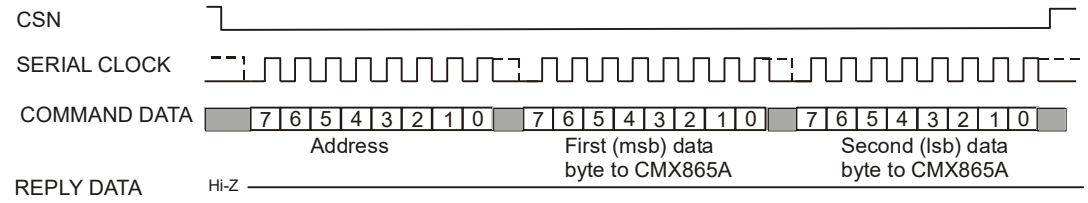
a) Single byte from µC



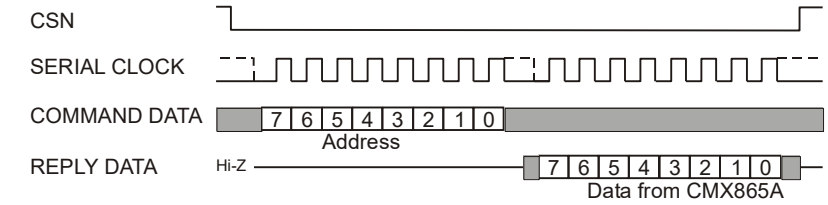
b) One Address and one Data byte from µC



c) One Address and 2 Data bytes from µC



d) One Address byte from µC and one Reply byte from CMX865A



e) One Address byte from µC and 2 Reply bytes from CMX865A

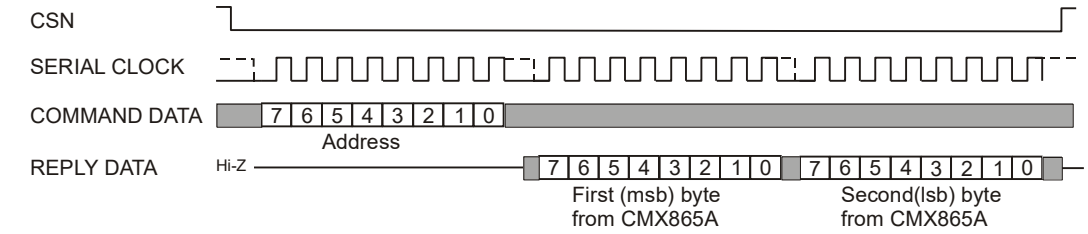


Figure 14 C-BUS Transactions

5.11.1. General Reset Command

General Reset Command (no data) C-BUS address $01
This command resets the device and clears all bits of the General Control, Transmit Mode and Receive Mode Registers and b15 and b13-0 of the Status Register.

The CMX865A will automatically perform a power-on reset when power is first applied, however, it is good practice to issue a C-BUS General Reset command. This action will cause the device to enter a powersave state (General Control Register bit 8 will be cleared to '0').

To bring the device out of powersave, please refer to the description of bits 7 and 8 in the General Control Register, Section 5.11.2.

5.11.2. General Control Register

General Control Register: 16-bit write-only. C-BUS address $E0

This register controls general features of the CMX865A such as the Powersave, Loopback mode and the IRQ mask bits. It also allows the fixed compromise equalisers in the Tx and Rx signal paths to be disabled if desired.

All bits of this register are cleared to 0 by a General Reset command.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXAN off	TXA off	0	0	LB	Equ	0	Pwr	Rst	Irqn en	0	IRQ Mask Bits				

General Control Register b13, b12, b9, b5: Reserved, set to 0

General Control Register b15: Disconnect TXAN Output
This bit allows the TXAN output to be disconnected and set to high impedance. See below for conditions applying to the setting of this bit.

b15 = 1	TXAN output disconnected
b15 = 0	TXAN output connected (normal modem operation)

General Control Register b14: Disconnect TXA Output
This bit allows the TXA output to be disconnected and set to high impedance. See below for conditions applying to the setting of this bit.

b14 = 1	TXA output disconnected
b14 = 0	TXA output connected (normal modem operation)

Requirements when using TXA/TXAN set to disconnected (b14=1 and/or b15=1)
1. While TXA/TXAN are set to disconnected, call progress mode must not be enabled.
2. If call progress mode has been previously enabled, a General Reset command must be sent before TXA/TXAN are set to disconnected.

General Control Register b11: Analogue Loopback Test Mode
This bit controls the analogue loopback test mode. Note that in loopback test mode both Transmit and Receive Mode Registers should be set to the same modem type and band or bit rate.

b11 = 1	Local analogue loopback mode enabled
b11 = 0	No loopback (normal modem operation)

General Control Register b10: Tx and Rx Fixed Compromise Equalisers
This bit allows the Tx and Rx fixed compromise equalisers in the modem transmit and receive filter blocks to be disabled.

b10 = 1	Disable equalisers
b10 = 0	Enable equalisers (1200bps modem modes)

General Control Register b8: Powerup
This bit controls the internal power supply to most of the internal circuits, including the Xtal oscillator and VBIAS supply. Note that the General Reset command clears this bit, putting the device into Powersave mode.

b8 = 1	Device powered up normally
b8 = 0	Powersave mode (ALL circuits, except C-BUS interface, are disabled)

When power is first applied to the device, the following powerup procedure should be followed to ensure correct operation.

i. (Power is applied to the device)
ii. Issue a General Reset command
iii. Write to the General Control Register (address $E0) setting both the Powerup bit (b8) and the Reset bit (b7) to '1' – leave in this state for a minimum of about 20ms – it is required that the crystal initially runs for this time in order to clock the internal logic into a defined state. The device is now powered up, with the crystal and VBIAS supply operating, but is otherwise not running any transmit or receive functions.
iv. The device is now ready to be programmed as and when required. Examples:
- A General Reset command could be issued to clear all the registers and therefore powersave the device.
- The Reset bit in the General Control Register could be set to '0' as part of a routine to program all the relevant registers for setting up a particular operating mode.

When the device is switched from Powersave mode to normal operation by setting the Powerup bit to '1', the Reset bit should also be set to '1' and should be held at '1' for about 20ms while the internal circuits, Xtal oscillator and V_{BIAS} stabilise before starting to use the transmitter or receiver.

General Control Register b7: Reset
Setting this bit to 1 resets the CMX865A's internal circuitry, clearing all bits of the Transmit and Receive Mode Registers, the Programming Register and b13-0 of the Status Register.

b7 = 1	Internal circuitry in a reset condition.
b7 = 0	Normal operation

General Control Register b6: IRQNEN (IRQN O/P Enable)
Setting this bit to 1 enables the IRQN output pin.

b6 = 1	IRQN pin driven low (to VSS) if the IRQ bit of the Status Register = 1
b6 = 0	IRQN pin disabled (high impedance)

General Control Register b4-0: IRQ Mask Bits
These bits affect the operation of the IRQ bit of the Status Register as described in section 5.11.7

5.11.3. Transmit Mode Register

Transmit Mode Register: 16-bit write-only. C-BUS address $E1

This register controls the CMX865A transmit signal type and level. All bits of this register are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx mode = modem				Tx level			0	0	0	0	Start-stop / synch data		# data bits / synch data source		
Tx mode = DTMF/Tones				Tx level			0	DTMF Twist			DTMF or Tone select				
Tx mode = Disabled				Set to 0000 0000 0000											

Tx Mode Register b15-12: Tx Mode
These 4 bits select the transmit operating mode.

B15	b14	b13	b12		
1	0	0	1	V.21 300bps FSK	High band (Answering modem)
1	0	0	0	"	Low band (Calling modem)
0	1	1	1	Bell 103 300bps FSK	High band (Answering modem)
0	1	1	0	"	Low band (Calling modem)
0	1	0	1	V.23 FSK	1200bps
0	1	0	0	"	75bps
0	0	1	1	Bell 202 FSK	1200bps
0	0	1	0	"	150bps
0	0	0	1	DTMF / Tones	
0	0	0	0	Transmitter disabled	

Tx Mode Register b11-9: Tx Level
These three bits set the gain of the Tx Level Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Tx Mode Register b8: Reserved, set to 0

Tx Mode Register b7-5: DTMF Twist (Tx DTMF Mode)
These three bits allow for adjustment of the DTMF twist to compensate for the frequency response of different external circuits. The device varies the twist by making changes to the upper tone-group levels. Note that the twist cannot be adjusted mid-tone.

b7	b6	b5	
0	0	0	+2.0dB twist (normal setting when external response is flat)
0	0	1	+1.0dB twist
0	1	0	+1.5dB twist
0	1	1	+2.5dB twist
1	0	0	+3.0dB twist
1	0	1	+3.5dB twist
1	1	0	+4.0dB twist
1	1	1	+4.5dB twist (do not use in conjunction with the 0dB Tx level setting)

Tx Mode Register b4-3: Tx Data Format (Tx Modem Modes)
These two bits select Synchronous or Start-stop mode and the addition of a parity bit to transmitted characters in the Start-stop mode.

b4	b3	
1	1	Tx Synchronous mode
1	0	Tx Start-stop mode, no parity
0	1	Tx Start-stop mode, even parity bit added to data bits
0	0	Tx Start-stop mode, odd parity bit added to data bits

Tx Mode Register b2-0: Tx Data and Stop Bits (Tx Start-Stop Modes)
In Tx Start-stop mode these three bits select the number of Tx data and stop bits.

b2	b1	b0	
1	1	1	8 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
0	1	0	6 data bits, 1 stop bit
0	0	1	5 data bits, 2 stop bits
0	0	0	5 data bits, 1 stop bit

Tx Mode Register b2-0: Tx Data Source (Tx Synchronous Mode)
In Tx Synchronous mode (b4-3 = 11) these three bits select the source of the data fed to the Tx FSK modulator.

b2	b1	b0	
1	x	x	Data bytes from Tx Data Buffer
0	1	1	Continuous 1s
0	1	0	Continuous 0s
0	0	x	Continuous alternating 1s and 0s

Tx Mode Register b3-0: DTMF/Tones Mode

If DTMF/Tones transmit mode has been selected (Tx Mode Register b14-12 = 001), then b7-5 should be set to 000 and b4-0 will select a DTMF signal, a fixed tone or one of four programmed tones or tone pairs for transmission.

b4 = 0: Tx fixed tone or programmed tone pair

b3	b2	b1	b0	Tone frequency (Hz)	
0	0	0	0	No tone	
0	0	0	1	697	
0	0	1	0	770	
0	0	1	1	852	
0	1	0	0	941	
0	1	0	1	1209	
0	1	1	0	1336	
0	1	1	1	1477	
1	0	0	0	1633	
1	0	0	1	1300	(Calling tone)
1	0	1	0	2100	(Answer tone)
1	0	1	1	2225	(Answer tone)
1	1	0	0	Tone pair TA	Programmed Tx tone or tone pair, see 5.11.8
1	1	0	1	Tone pair TB	“
1	1	1	0	Tone pair TC	“
1	1	1	1	Tone pair TD	“

b4 = 1: Tx DTMF

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

5.11.4. Receive Mode Register

Receive Mode Register: 16-bit write-only. C-BUS address $E2

This register controls the CMX865A receive signal type and level.

All bits of this register are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rx mode = Modem				Rx level			0	0	0	Start-stop/Synch			No. of bits and parity		
Rx mode = Tones detect				Rx level			DTMF/Tones/Call Progress select								
Rx mode = Disabled				Set to 0000 0000 0000											

Rx Mode Register b15-12: Rx Mode
These 4 bits select the transmit operating mode.

B15	b14	b13	b12		
1	0	0	1	V.21 300bps FSK	High band (Calling modem)
1	0	0	0	"	Low band (Answering modem)
0	1	1	1	Bell 103 300bps FSK	High band (Calling modem)
0	1	1	0	"	Low band (Answering modem)
0	1	0	1	V.23 FSK	1200bps
0	1	0	0	"	75bps
0	0	1	1	Bell 202 FSK	1200bps
0	0	1	0	"	150bps
0	0	0	1	Tones	Detect
0	0	0	0	Receiver disabled	

Rx Mode Register b11-9: Rx Level
These three bits set the gain of the Rx Gain Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Rx Mode Register b5-3: Rx USART Setting (Rx Modem Modes)
These three bits select the Rx USART operating mode.

b5	b4	b3	
1	1	1	Rx Synchronous mode
1	1	0	Rx Start-stop mode
1	0	x	Reserved
0	x	x	Rx USART function disabled

Rx Mode Register b2-0: Rx Data Bits and Parity (Rx Start-Stop Modes)
In Rx Start-stop mode these three bits select the number of data bits (plus any parity bit) in each received character. These bits are ignored in Rx Synchronous mode.

b2	b1	b0	
1	1	1	8 data bits + parity
1	1	0	8 data bits
1	0	1	7 data bits + parity
1	0	0	7 data bits
0	1	1	6 data bits + parity
0	1	0	6 data bits
0	0	1	5 data bits + parity
0	0	0	5 data bits

Rx Mode Register b2-0: Tones Detect Mode
In Tones Detect Mode (Rx Mode Register b14-12 = 001) b8-3 should be set to 000000. These three bits select the detector type.

b2	b1	b0	
1	0	0	Programmable Tone Pair Detect
0	1	1	Call Progress Detect
0	1	0	2100Hz, 2225Hz Answer Tone Detect
0	0	1	DTMF Detect
0	0	0	Disabled

While TXA/TXAN are set to disconnected, call progress mode must not be enabled. See General Control register b15 and b14, Section 5.11.2.

5.11.5. Tx Data Register

Tx Data Register: 8-bit write-only. C-BUS address $E3

Bit:	7	6	5	4	3	2	1	0
	Data bits to be transmitted							

In Tx Synchronous mode, this register contains the next 8 data bits to be transmitted. b0 is transmitted first.

In Tx Start-Stop mode, the specified number of data bits will be transmitted from this register (b0 first). A Start bit, a Parity bit (if required) and Stop bit(s) will be added automatically.

This register should only be written to when the Tx Data Ready bit of the Status Register is 1.

5.11.6. Rx Data Register

Rx Data Register: 8-bit read-only. C-BUS address $E5

Bit:	7	6	5	4	3	2	1	0
	Received data bits							

In Rx synchronous mode, this register contains 8 received data bits, b0 of the register holding the earliest received bit, b7 the latest.

In Rx Start-Stop mode, this register contains the specified number of data bits from a received character, b0 holding the first received bit. Unused bits are set to 0.

5.11.7. Status Register

Status Register: 16-bit read-only. C-BUS address $E6

All the bits of this register (except b15-14) are cleared to 0 by a General Reset command, or when b7 (Reset) of the General Control Register is 1. Bit b13 of this register will automatically be set to 1 after the General Control Register Reset bit (b7) has been cleared to 0 and the CMX865A is ready to accept any parameters sent to the Programming Register ($E8).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ	0	PF	See below for uses of these bits												

The meanings of the Status Register b12-0 depend on whether the receive circuitry is in Modem or Tones Detect mode.

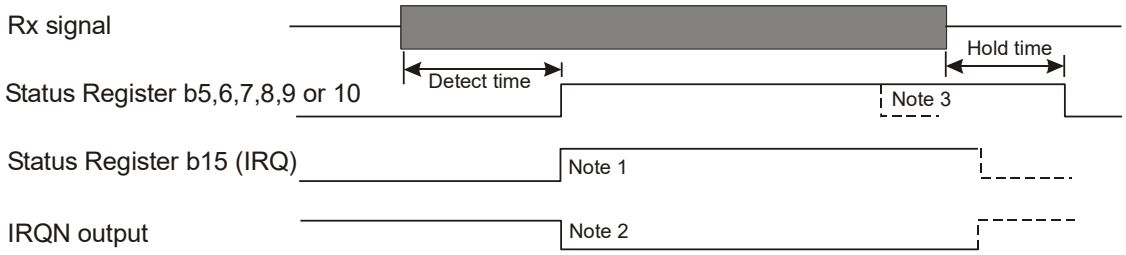
Status Register bits:

	Rx Modem modes	Rx Tones Detect modes	** IRQ Mask bit
b15	IRQ		
b14	0		-
b13	Programming Flag bit. See 5.11.8		b4
b12	Set to 1 on Tx data ready. Cleared by write to Tx Data Register		b3
b11	Set to 1 on Tx data underflow. Cleared by write to Tx Data Register		b3
b10	1 when energy is detected in Rx modem signal band	1 when energy is detected in Call Progress band or when both programmable tones are detected	b2
b9	1 when '1010..' pattern is detected	0	b1
b8	1 when continuous 0s detected	0	b1
b7	1 when continuous 1s detected	1 when 2100Hz answer tone or the second programmed tone is detected	b1
b6	Set to 1 on Rx data ready. Cleared by read from Rx Data Register	1 when 2225Hz answer tone or the first programmed tone is detected	b0
b5	Set to 1 on Rx data overflow. Cleared by read from Rx Data Register	1 when DTMF code is detected	b0
b4	Set to 1 on Rx framing error	0	-
b3	Set to 1 on even Rx parity	Rx DTMF code b3, see Table 3	-
b2	0	Rx DTMF code b2	-
b1	0	Rx DTMF code b1	-
b0	FSK frequency demodulator output	Rx DTMF code b0	-

Table 2 Status Register

Notes: ** This column shows the corresponding IRQ Mask bits in the General Control Register. A 0-to-1 transition on any of the Status Register b13-5 will cause the IRQ b15 to be set to 1 if the corresponding IRQ Mask bit is 1. The IRQ bit is cleared by a read of the Status Register or a General Reset command or by setting b7 or b8 of the General Control Register to 1.

The operation of the data demodulator and pattern detector circuits within the CMX865A does not depend on the state of the Rx energy detect function.



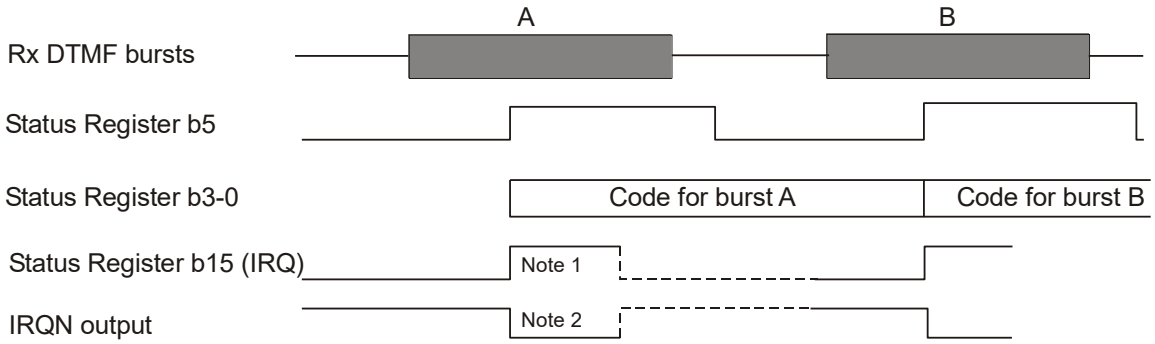
Notes:
1. IRQ will go high only if appropriate IRQ Mask bit in General Control Register is set to 1. The IRQ bit is cleared by a read of the Status Register.
2. IRQN o/p will go low when the IRQ bit is high if the IRQNEN bit of General Control Register is set to 1.
3. In Rx Modem modes Status Register b5 and b6 are set to 1 by a Rx Data Ready or Rx Data Underflow event and cleared by a read of the Rx Data Register

Figure 15 Operation of Status Register b10-5

The IRQN output pin will be pulled low (to VSS) when the IRQ bit of the Status Register and the IRQNEN b6 of the General Control Register are both 1.

Changes to Status Register bits caused by a change of Tx or Rx operating mode can take up to 150μs to take effect.

In Rx modem modes b2-1 will be 0 and b0 will show the output of the frequency demodulator, updated at 8 times the nominal data rate.



Notes:
1. IRQ will go high only if the IRQ Mask b0 in the General Control Register is set to 1. The IRQ bit is cleared to 0 by a read of the Status Register.
2. IRQN o/p will go low when the IRQ bit is high if the IRQNEN bit of the General Control Register is set to 1.

Figure 16 Operation of Status Register in DTMF Rx Mode

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

Table 3 Received DTMF Code: Status Register b3-0

5.11.8. Programming Register

Programming Register : 16-bit write-only. C-BUS address $E8

This register is used to program the transmit and receive programmed tone pairs by writing appropriate values to RAM locations within the CMX865A. Note that these RAM locations are cleared by Powersave or Reset operations.

The Programming Register should only be written to when the Programming Flag bit (b13) of the Status Register is 1. The act of writing to the Programming Register clears the Programming Flag bit. When the programming action has been completed (normally within 150μs) the CMX865A will set the bit back to 1.

When programming Transmit or Receive Tone Pairs, do not change the Transmit or Receive Mode registers until programming is complete and the Programming Flag bit has returned to 1.

Transmit Tone Pair Programming

4 transmit tone pairs (TA to TD) can be programmed.

The frequency (max 3.4kHz) and level must be entered for each tone to be used.

Single tones are programmed by setting both level and frequency values to zero for one of the pair.

Programming is done by writing a sequence of up to seventeen 16-bit words to the Programming Register. The first word should be 32768 (8000 hex), the following 16-bit words set the frequencies and levels and are in the range 0 to 16383 (0-3FFF hex):

Word	Tone Pair	Value written
1		32768
2	TA	Tone 1 frequency
3	TA	Tone 1 level
4	TA	Tone 2 frequency
5	TA	Tone 2 level
6	TB	Tone 1 frequency
7	TB	Tone 1 level
---	---	----------
---	---	----------
16	TD	Tone 2 frequency
17	TD	Tone 2 level

The frequency values to be entered are calculated from the formula:

Value to be entered = desired frequency (Hz) * 3.414

i.e. for 1kHz the value to be entered is 3414 (or 0D56 in Hex).

The level values (measured at TXA or TXAN) to be entered are calculated from the formula:

$$\text{Value to be entered} = \text{desired Vrms} * 93780 / V_{DD}$$

i.e. for 0.5Vrms at VDD = 3.3V, the value to be entered is 14209 (3781 in Hex).

This will give a signal of 1.0Vrms when measured between TXA and TXAN pins, or approximately 0.45Vrms when measured across the line, with the component values in section 4.1.

Programming a no-tone pair is done by writing zero to all four tone pair words.

Note that allowance should be made for the transmit signal filtering in the CMX865A which attenuates the output signal for frequencies above 2kHz by 0.25dB at 2.5kHz, by 1dB at 3kHz and by 2.2dB at 3.4kHz.

After resetting the device, by toggling the Reset bit (b7) of the General Control Register ($E0), the tone pairs TA, TB and TC are set to notone and TD is set to generate 2130Hz + 2750Hz at approximately –20dBm for each tone, when measured at either TXA or TXAN pin.

Receive Tone Pair Programming

The programmable tone pair detector is implemented as shown in Figure 17. The filters are 4th order IIR sections. The frequency detectors measure the time taken for a programmable number of complete input signal cycles, and compare this time against programmable upper and lower limits.

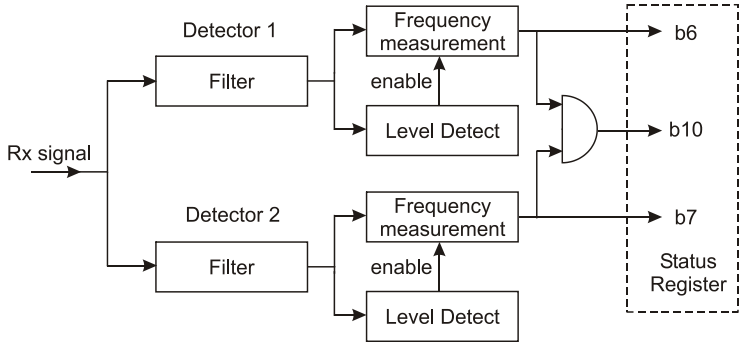


Figure 17 Programmable Tone Detectors

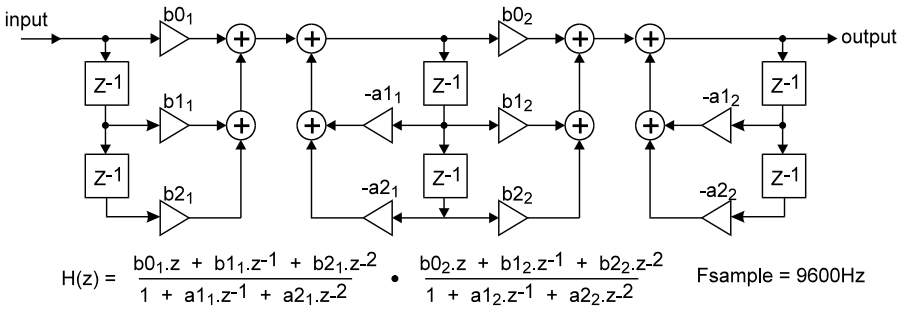


Figure 18 Filter Implementation

Programming is done by writing a sequence of twenty-seven 16-bit words to the Programming Register. The first word should be 32769 (8001 hex), the following twenty-six 16-bit words set the frequencies and levels and are in the range 0 to 32767 (0000-7FFF hex).

Word	Value written	Word	Value written
1	32769		
2	Filter #1 coefficient $b2_1$	15	Filter #2 coefficient $b2_1$
3	Filter #1 coefficient $b1_1$	16	Filter #2 coefficient $b1_1$
4	Filter #1 coefficient $b0_1$	17	Filter #2 coefficient $b0_1$
5	Filter #1 coefficient $a2_1$	18	Filter #2 coefficient $a2_1$
6	Filter #1 coefficient $a1_1$	19	Filter #2 coefficient $a1_1$
7	Filter #1 coefficient $b2_2$	20	Filter #2 coefficient $b2_2$
8	Filter #1 coefficient $b1_2$	21	Filter #2 coefficient $b1_2$
9	Filter #1 coefficient $b0_2$	22	Filter #2 coefficient $b0_2$
10	Filter #1 coefficient $a2_2$	23	Filter #2 coefficient $a2_2$
11	Filter #1 coefficient $a1_2$	24	Filter #2 coefficient $a1_2$
12	Freq measurement #1 ncycles	25	Freq measurement #2 ncycles
13	Freq measurement #1 mintime	26	Freq measurement #2 mintime
14	Freq measurement #1 maxtime	27	Freq measurement #2 maxtime

Table 4 Programming Register: Filter Coefficients

The coefficients are entered as 15-bit signed (two's complement) integer values (the most significant bit of the 16-bit word entered should be zero) calculated as 8192 * coefficient value from the user's filter design program (i.e. this allows for filter design values of -1.9999 to +1.9999).

The design of the IIR filters should make allowance for the fixed receive signal filtering in the CMX865A which has a low pass characteristic above 1.5kHz of 0.4dB at 2kHz, 1.2dB at 2.5kHz, 2.6dB at 3kHz and 4.1dB at 3.4kHz.

'ncycles' is the number of signal cycles for the frequency measurement.

'mintime' is the smallest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'mintime' = 9600 * ncycles / high frequency limit.

'maxtime' is the highest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'maxtime' = 9600 * ncycles / low frequency limit.

The level detectors include hysteresis. The threshold levels - measured at the 2 or 4-wire line with unity gain filters, using the line interface circuits described in section 4.1, 1.0dB line coupling transformer loss and with the Rx Gain Control block set to 0dB - are nominally:

'Off' to 'On' -44.5dBm
'On' to 'Off' -47.0dBm

Note that if any changes are made to the programmed values while the CMX865A is running in Programmed Tone Detect mode they will not take effect until the CMX865A is next switched into Programmed Tone Detect mode.

After resetting the device, by toggling the Reset bit (b7) of the General Control Register ($E0), all previously programmed filter coefficients are lost and the programmable tone pair detector is set to act as a simple 2130Hz + 2750Hz detector.

6. Application Notes

DAA designs, application notes, FAQs and other design resources can be found on the CML website.

6.1. Simple voice record and playback on the CMX865A

In alarm panels and telecom terminals there is frequently a requirement to record and playback voice signals. The CMX865A has a codec at the front end and this can be accessed via a test mode. The record and playback path can be handled independently so voice samples can be either recorded or pre-recorded as required. By arranging the CMX865A signal input source to be switched, voice signals can be recorded locally via a microphone. This application note gives a starting point for evaluation of this function.

The codec interface transfers a pair of signed, 16-bit words in both directions every 1/9600 second. This gives an effective sample rate of 19.2ks/s in both receive (ADC) and transmit (DAC) paths. Because the CMX865A is intended for telecom use, additional filtering, particularly of the playback path may be desired. However, the method given has been found to produce toll-quality results provided attention is paid to the signal levels to be recorded.

To playback, the C-BUS test register DDW and the Tx Data register need to be written with a pair of 16-bit samples for the DAC path. The write to test register DDW causes the Programming Flag (PF flag) in the Status register to go low until the next pair of samples is required. The PF flag will then go high, providing a timing reference that indicates the next pair of samples can be written. As the CMX865A services the DAC path, it will also service the ADC path and deliver a pair of samples to the receive registers.

To record, it is necessary to write the DAC path to obtain the PF flag timing reference. This can be a dummy write of the test register DDW if no simultaneous transmit signal is required (use $2000 if Tx bias is wanted). When the PF flag changes state from 0 to 1, the receive pair of samples from the ADC path are valid. These can be read from the test register DDR and the Rx Data register.

The test mode, used here to provide the record/playback facility, must not be called during normal modem operation. It can be called immediately following a standard modem operation or after a General Reset has been issued. A General Reset must be issued after the CMX865A has been used in this test mode before resuming normal modem function.

The set-up below was used with the following PE0002 script example to illustrate a simple speech recorder and playback device. The sound samples were recorded with a level at RXFB around 500mV pk-pk average and peaking at no more than +/- 1V. No anti-alias filters or reconstruction filters were used in the set-up. Users must ensure that the recording path is suitable for the signal source used and that the playback path meets the requirements applicable to the system in which is to be used.

To reduce the amount of data storage required a simple decimation method discards one of the samples from each of the receive path pair. To reduce the noise on transmit, the sample rate is increased using a simple interpolation method. The average of the current and previous sample are used to replace the sample discarded in the decimation process.

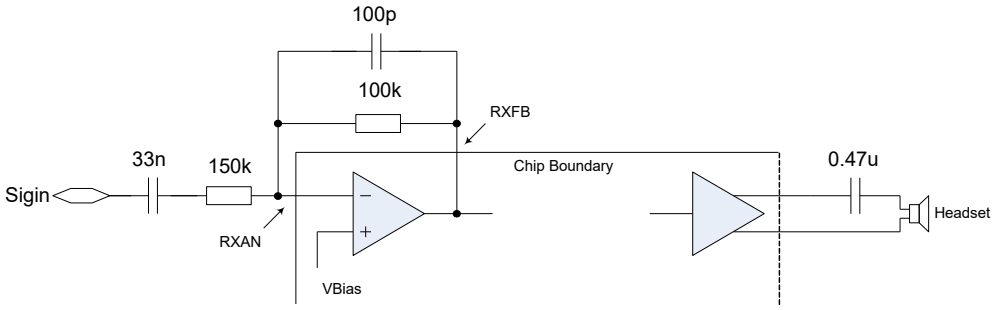


Figure 19 Voice Record and Playback - Test Set-up

```
;This PE0002 script provides test access to the codec in the CMX865A allowing speech
;to be recorded and played back.
;
; Data transfers are synchronised using the Programming Flag bit of the C-BUS Status
;Register.
;
;Set up the C-BUS General Mode Reg ($E0) as required. Interrupts cannot be used. Then:
;       Wait for b13 of the Status Reg to be 1
;       Write $C012 to the C-BUS test register ($E9)
;       Repeat the following for the required recording length.
;               Wait for b13 of the Status Reg to go to 1.
;               Write 0 to the C-BUS Tx Data Reg ($E3)
;               Write codec word #2 to the C-BUS Debug Data Write ($EA), doing
;               this will clear b13 of the Status Reg.
;               Read A/D word #1 from the C-BUS Rx Data Reg ($E5)
;               Read A/D word #2 from the C-BUS Debug Data Read Reg ($EB)
;       Finish by sending a General Reset to the CMX865A.
;
;The data written to the codec is 16-bit signed. The values read from the codec
;are 15-bit signed. In this test mode, the C-BUS Tx and Rx Data Registers are set
;to 2-character mode. The normal CMX865A Tx and Rx functions are disabled while this
;routine runs.
;
*********************************************************************************
Gain            const 2         ;set the gain here n x 2 (sets no of asl operations)
temp0           word 0          ;G/P var
temp1           word 0          ;G/P var
temp2           word 0          ;G/P var
count           word 0          ;G/P counter 0
GEN_RESET       const $01       ;General Reset Register
cbusgcr         const $E0       ;General Control Register
cbustxd         const $E3       ;Tx data reg
cbusrxd         const $E5       ;Rx data register
cbussr          const $E6       ;Status Register
cbusprr         const $E8       ;Programming Register
cbusddar        const $E9       ;Test Register
cbusddw         const $EA       ;Test Data Write
cbusddr         const $EB       ;Test Data Read
TestMode        const $C012     ;Word to invoke test mode
VoiceFrame      buffer 60000    ;Array for coded voice
BufferSize      const 60000     ;Make Buffersize = VoiceFrame array length

;*********************************************************************************

; Reset and Powerup the CMX865A
        jsr GenReset                    ;General Reset is only needed if it hasn't been
                                        ;called since powering on.
        jsr Status_wait                 ;Wait until Programming flag (PF) is set.
```

```
; Start the test mode
       copy TestMode *cbusddar       ;Write C012H to Test register.
       jsr Status_wait               ;Wait for PF flag

;RecordMode
; Read approx 15 seconds of voice data into array
       copy 0 *cbustxd               ;Zero DAC for alternate codec writes
       copy 0 count                  ;Initialise count
       while count < BufferSize
       copy 0 *cbusddw               ;Dummy write to codec. This write triggers the PF
                                     ;flag
              jsr Status_wait        ;Wait for PF flag
              copy *cbusrxd VoiceFrame[count++]     ;Get 1st sample
;             copy *cbusddr VoiceFrame[count++]     ;Simple decimation- discard 2nd
                                                    ;sample
       endwhile

;Copy Voiceframe to PC file for evaluation if required.
;       fopenw "ADCRecordData.txt"           ;Create/open the PC file to write.
;       copy    0 count                      ;Initialise count.
;       while count < BufferSize             ;Copy the entire array to the file.
;              filew "%04x" VoiceFrame[count++]
;              microdelay 8                  ;Use microdelay or delay to prevent
;       endwhile                             ;Text Out Buffer overflows.

;Playback mode
       dialog "Ready to playback"
       copy 0 count
       while count < BufferSize
              copy VoiceFrame[count++] temp1        ;Initialise temp1/temp2 for
                                                    ;simple averaging.
              copy VoiceFrame[count] temp2

;Simple averaging interpolation
              add temp1 temp2
              asr 1 temp2

;Add gain as required
              lsl Gain temp1
              lsl Gain temp2
;and write them
              jsr Status_wait               ;Wait for PF flag then
              copy temp1 *cbustxd           ;write the averaged samples.
              copy temp2 *cbusddw
        endwhile

       jsr Status_wait               ; Wait for PF flag.
       copy 0 *cbustxd               ; Done so zero the DACs to silence them.
       copy 0 *cbusddw

       stop

;******* Read Status register and return when b13 set *******
Status_wait
       copy *cbussr temp0                   ; Read Status reg into temp0.
       and $2000 temp0                      ; Mask off unwanted bits.
       jmpc temp0 != $2000 Status_wait      ; If PF flag (b13) not set, loop.
       return

;*******

;******* Send a General Reset to device 1 *******
GenReset
       register 1 GEN_RESET 0        ;Set data length of C-BUS port $01
       copy 0 *GEN_RESET             ;Send General Reset.
       copy $0180 *cbusgcr           ;Set Powerup (b8) and Reset (b7).
       delay 50                      ;Wait 50ms for bias to settle.
       copy $0100 *cbusgcr           ;Clear Reset bit (b7).
       return                        ;CMX865A ready to use.

;*******
```

6.2. Mixing external signals such as voice onto the transmit path

The state of the transmit output pins TXA and TXAN depends on the operating mode selected. When both the transmit and receive modes are disabled, TXA and TXAN become tri-state. See Table 1. Because these paths are high impedance, a signal path can be connected to them without significant loss. The tri-state impedance is around 100k so the signal source impedance should be around 10k or less. The signal source must also have a tri-state capability to ensure that when the CMX865A is transmitting, the transmit signal is not excessively attenuated.

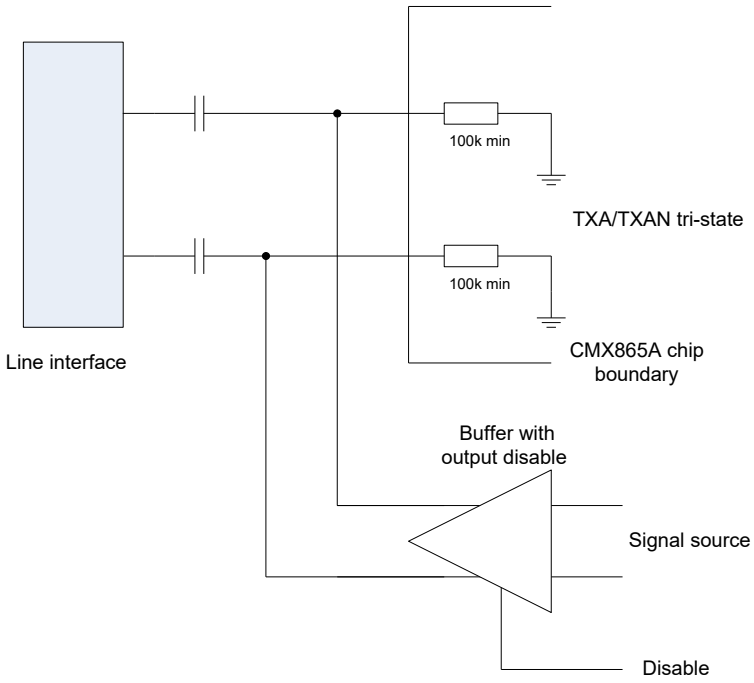


Figure 20 Mixing signals onto the line interface

Ac coupling is shown in Figure 20 above but will not be necessary if the line interface does not require it. If ac coupling is used, the capacitor values should be chosen to pass the lowest frequency components without excessive attenuation. For the CMX865A, the lowest frequency component is around 300Hz.

The device that is buffering the signal source above could be an op-amp or other device such as a speech codec. The source signal level should not exceed the maximum ratings for the CMX865A output pins. For single-ended line interfaces, use either TXA or TXAN only.

6.3. Receiving on-hook Caller-ID

When the modem is on-hook it is unable to receive signals across the line interface, thus preventing it from receiving Caller-ID signals. It is common practice to arrange a capacitive signal path across the hookswitch allowing these signals to reach the modem. This capacitor must have a low value so that the on-hook ac impedance requirement is not exceeded. Having a low-value capacitor presents a high impedance to the Caller-ID signal which is then attenuated by the transformer terminating impedance. If the termination components can be switched out of circuit the transformer presents a (theoretically) infinite impedance to the hookswitch bypass capacitor, resulting in less attenuation of the Caller-ID signal. In practice an improvement of a few dB is available. Setting either TXA or TXAN to “disconnected” effectively switches out the line termination without removing the dc bias conditions. The method is illustrated in

Figure 21 below. This method is acceptable in an on-hook state but if the swiches are opened in an off-hook state, the return loss of the interface is unacceptable and significant reflections of the received signal may occur. Opening and closing the switches may also cause unwanted transients to appear on the line.

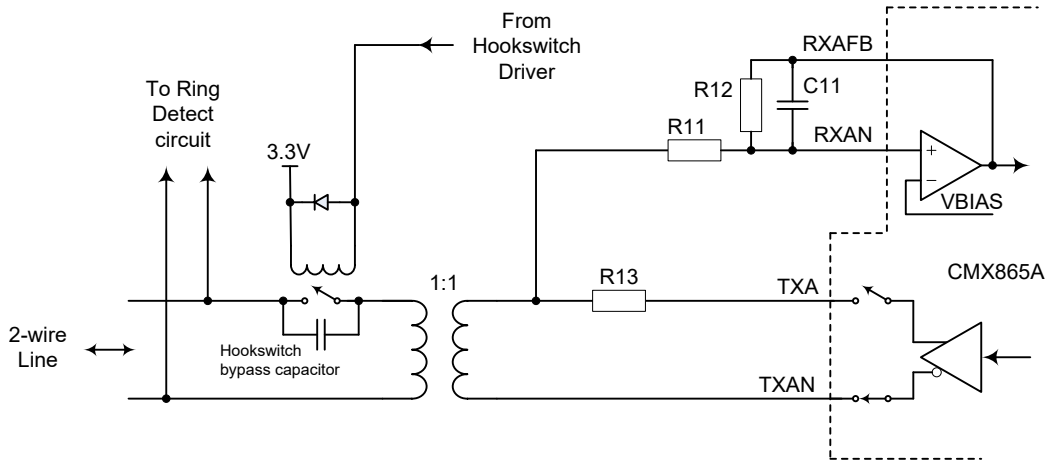


Figure 21 Using TXAN for improved Caller-ID reception

7. Performance Specification

7.1. Electrical Performance

7.1.1. Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - AV_{SS}) or (V_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin (except V_{DEC}) to V_{SS}	-0.3	V_{DD} + 0.3	V
Voltage between AV_{SS} and DV_{SS}	-50	+50	mV
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into or out of any other pin	-20	+20	mA

D4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		540	mW
... Derating		5.4	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

E4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		870	mW
... Derating		8.7	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

7.1.2. Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - AV_{SS}) and (V_{DD} - DV_{SS})		3.0	3.6	V
Supply rise time (10% to 90%)			25	ms
Operating Temperature		-40	+85	°C

7.1.3. Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 3.0V to 3.6V at Tamb = -40 to +85°C,
Xtal Frequency = 6.144MHz ± 0.03% (300ppm)
0dBm corresponds to 775mVrms.

DC Parameters	Notes	Min.	Typ.	Max.	Units
I_{DD} (Powersave mode)	1, 2	-	6.5	-	µA
(Reset but not powersave, V_{DD} = 3.3V)	1, 3	-	3.0	4.0	mA
(Running, V_{DD} = 3.3V)	1	-	4.0	7.0	mA
Logic '1' Input Level		70%	-	-	V_{DD}
Logic '0' Input Level		-	-	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 2 mA)		80%	-	-	V_{DD}
Output Logic '0' Level (I_{OL} = -3 mA)		-	-	0.4	V
IRQN O/P 'Off' State Current (Vout = V_{DD})		-	-	1.0	µA

Notes:
1. At 25°C, not including any current drawn from the CMX865A pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for CSN which is at V_{DD}.
3. General Mode Register b8-7 set to 11.

XTAL/CLOCK Input (timings for an external clock input)	Notes	Min.	Typ.	Max.	Units
'High' Pulse Width		30	-	-	ns
'Low' Pulse Width		30	-	-	ns

Transmit V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	5	–	300	–	Baud
Mark (logical 1) frequency, high band		1647	1650	1653	Hz
Space (logical 0) frequency, high band		1847	1850	1853	Hz
Mark (logical 1) frequency, low band		978	980	982	Hz
Space (logical 0) frequency, low band		1178	1180	1182	Hz

Transmit Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	5	-	300	-	Baud
Mark (logical 1) frequency, high band		2222	2225	2228	Hz
Space (logical 0) frequency, high band		2022	2025	2028	Hz
Mark (logical 1) frequency, low band		1268	1270	1272	Hz
Space (logical 0) frequency, low band		1068	1070	1072	Hz

Transmit V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	5	-	1200/75	-	Baud
Mark (logical 1) frequency, 1200 baud		1298	1300	1302	Hz
Space (logical 0) frequency, 1200 baud		2097	2100	2103	Hz
Mark (logical 1) frequency, 75 baud		389	390	391	Hz
Space (logical 0) frequency, 75 baud		449	450	451	Hz

Transmit Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	5	-	1200/150	-	Baud
Mark (logical 1) frequency, 1200 baud		1198	1200	1202	Hz
Space (logical 0) frequency, 1200 baud		2197	2200	2203	Hz
Mark (logical 1) frequency, 150 baud		386	387	388	Hz
Space (logical 0) frequency, 150 baud		486	487	488	Hz

DTMF/Single Tone Transmit	Notes	Min.	Typ.	Max.	Units
Tone frequency accuracy		-0.2	-	+0.2	%
Distortion	6	-	1.0	2.0	%

Notes:
5. Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.
6. Measured between TXA and TXAN pins with Tx Level Control gain set to 0dB, 1k2Ω load between TXA and TXAN, at V_{DD} = 3.3V (levels are proportional to V_{DD} - see section 4.1). Level measurements for all modem modes are performed with random transmitted data. 0dBm = 775mVrms.

Transmit Output Level	Notes	Min.	Typ.	Max.	Units
Modem and Single Tone modes	6	-3.2	-2.2	-1.2	dBm
DTMF mode, Low Group tones	6	-1.2	-0.2	+ 0.8	dBm
DTMF twist (level of high group tones wrt low group) setting accuracy	6	-1.0	-	+1.0	dB
Tx output buffer gain control accuracy	6	-0.25	-	+0.25	dB

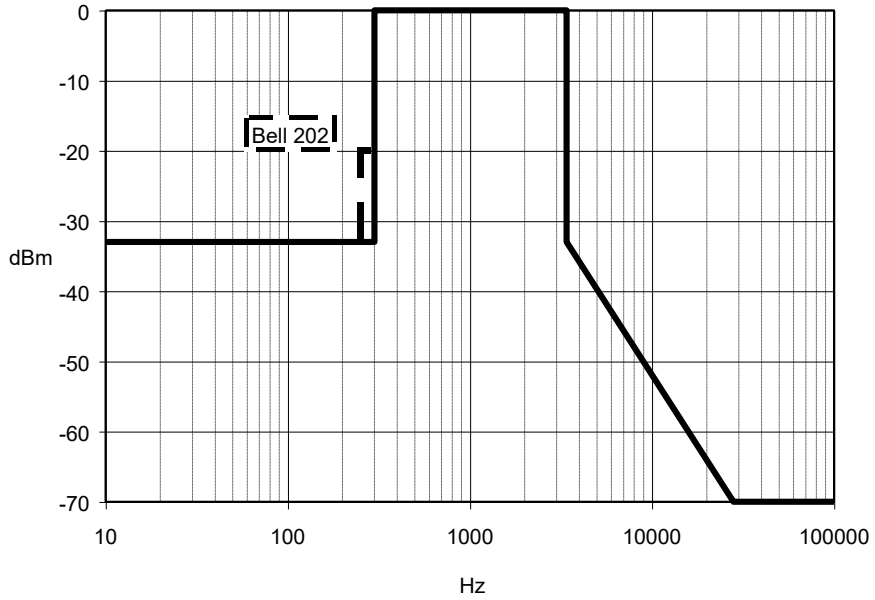


Figure 22 Maximum Out of Band Tx Line Energy Limits (see note 7)

Notes: 7. Measured on the 2 or 4-wire line using the line interface circuits described in section 4.1 with the Tx line signal level set to –9.2dBm for FSK or single tones, -5.2dBm and –7.2dBm for DTMF tones. Excludes any distortion due to external components such as the line coupling transformer.

Receive V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		1638	1650	1662	Hz
Space (logical 0) frequency, high band		1838	1850	1862	Hz
Mark (logical 1) frequency, low band		968	980	992	Hz
Space (logical 0) frequency, low band		1168	1180	1192	Hz

Receive Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		2213	2225	2237	Hz
Space (logical 0) frequency, high band		2013	2025	2037	Hz
Mark (logical 1) frequency, low band		1258	1270	1282	Hz
Space (logical 0) frequency, low band		1058	1070	1082	Hz

Receive V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1280	1300	1320	Hz
Space (logical 0) frequency		2080	2100	2120	Hz
75 baud					
Acceptable baud rate		74	75	76	Baud
Mark (logical 1) frequency		382	390	398	Hz
Space (logical 0) frequency		442	450	458	Hz

Receive Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1180	1200	1220	Hz
Space (logical 0) frequency		2180	2200	2220	Hz
150 baud					
Acceptable baud rate		148	150	152	Baud
Mark (logical 1) frequency		377	387	397	Hz
Space (logical 0) frequency		477	487	497	Hz

Rx Modem Signal	Notes	Min.	Typ.	Max.	Units
Signal level	8	-45	-	-9	dBm
Signal to Noise Ratio (noise flat 300-3400Hz)		20	-	-	dB

Notes: 8. Rx 2 or 4-wire line signal level assuming 1dB loss in line coupling transformer with Rx Gain Control block set to 0dB and external components as section 4.1.

Rx Modem Energy Detector	Notes	Min.	Typ.	Max.	Units
Detect threshold (‘Off’ to ‘On)	8, 9	-	-	-43.0	dBm
Undetect threshold (‘On’ to ‘Off’)	8, 9	-48.0	-	-	dBm
Hysteresis	8, 9	2.0	-	-	dB
Detect (‘Off’ to ‘On’) response time					
300 and 1200baud	8, 9	8.0	-	30.0	ms
150 and 75baud	8, 9	16.0	-	60.0	ms
Undetect (‘On’ to ‘Off’) response time					
300 and 1200baud	8, 9	10.0	-	40.0	ms
150 and 75baud	8, 9	20.0	-	80.0	ms

Rx Answer Tone Detectors	Notes	Min.	Typ.	Max.	Units
Detect threshold (‘Off’ to ‘On)	8, 10	-	-	-43.0	dBm
Undetect threshold (‘On’ to ‘Off’)	8, 10	-48.0	-	-	dBm
Hysteresis	8, 10	2.0	-	-	dB
Detect (‘Off’ to ‘On’) response time	8, 10	30.0	33.0	45.0	ms
Undetect (‘On’ to ‘Off’) response time	8, 10	7.0	18.0	25.0	ms
2100Hz detector					
‘Will detect’ frequency		2050	-	2160	Hz
‘Will not detect’ frequency		-	-	2000	Hz
2225Hz detector					
‘Will detect’ frequency		2160	-	2285	Hz
‘Will not detect’ frequency		2335	-	-	Hz

Rx Call Progress Energy Detector	Notes	Min.	Typ.	Max.	Units
Bandwidth (-3dB points) See Figure 8		275	-	665	Hz
Detect threshold (‘Off’ to ‘On)	8, 11	-	-	-37.0	dBm
Undetect threshold (‘On’ to ‘Off’)	8, 11	-42.0	-	-	dBm
Detect (‘Off’ to ‘On’) response time	8, 11	30.0	36.0	45.0	ms
Undetect (‘On’ to ‘Off’) response time	8, 11	6.0	8.0	50.0	ms

Notes:
9. Thresholds and times measured with continuous binary ‘1’. Fixed compromise line equaliser enabled. Signal switched between off and -33dBm.
10. ‘Typical’ value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured wrt. received line signal.
11. ‘Typical’ value refers to 400Hz signal switched between off and -33dBm.

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	8	-31.0	-	2.0	dBm
Not decode level (either tone of composite signal)	8	-	-	-38.0	dBm
Twist = High Tone/Low Tone		-10.0	-	10.0	dB
Frequency Detect Bandwidth		±2.2	-	-	%
Frequency Not Detect Bandwidth		-	-	±3.5	%
Max level of low frequency noise (i.e. dial tone)					
Interfering signal frequency <= 550Hz	12	-	-	0.0	dB
Interfering signal frequency <= 450Hz	12	-	-	10.0	dB
Interfering signal frequency <= 200Hz	12	-	-	20.0	dB
Max. noise level wrt. signal	12, 13	-	-	-10.0	dB
DTMF detect response time	15	-	40.0	-	ms
DTMF de-response time		-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms
Falsing performance	14	–	13	–	falses/ 30mins

Notes:
12. Referenced to DTMF tone of lower amplitude.
13. Flat Gaussian Noise in 300-3400Hz band.
14. Mitel CM7291 test tape, 1kHz reference tone set to 775mVrms.
15. See Figure 16. The decode time is directly affected by signal quality but, for good signals, will always be much less than the 100ms required for PSTN use.

Receive Input Amplifier	Notes	Min.	Typ.	Max.	Units
Input impedance (at 100Hz)		10.0			Mohm
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

C-BUS Timings (See Figure 23)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock-High time		100	-	-	ns
t_{CL}	Serial Clock-Low time		100	-	-	ns
t_{CDS}	Command Data Set-Up time		75.0	-	-	ns
t_{CDH}	Command Data Hold time		25.0	-	-	ns
t_{RDS}	Reply Data Set-Up time		50.0	-	-	ns
t_{RDH}	Reply Data Hold time		0.0	-	-	ns

Maximum 30pF load on each C-BUS interface line.

Note: These timings are for the latest version of the C-BUS as embodied in the CMX865A.

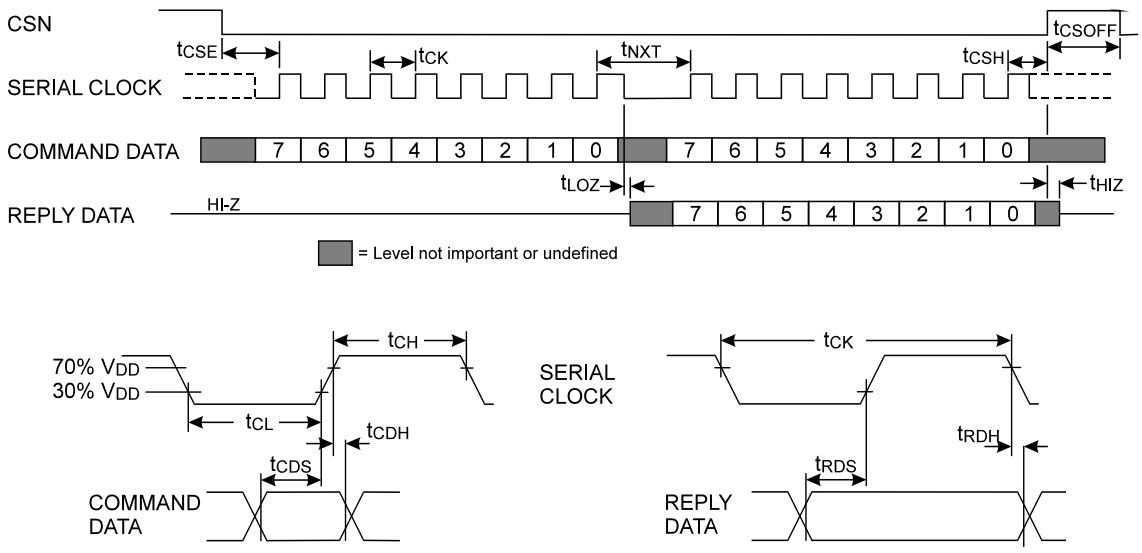
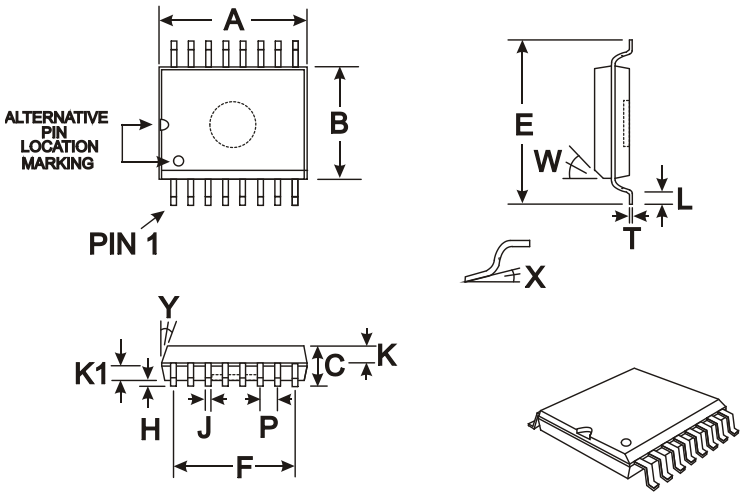


Figure 23 C-BUS Timing

7.2. Packaging



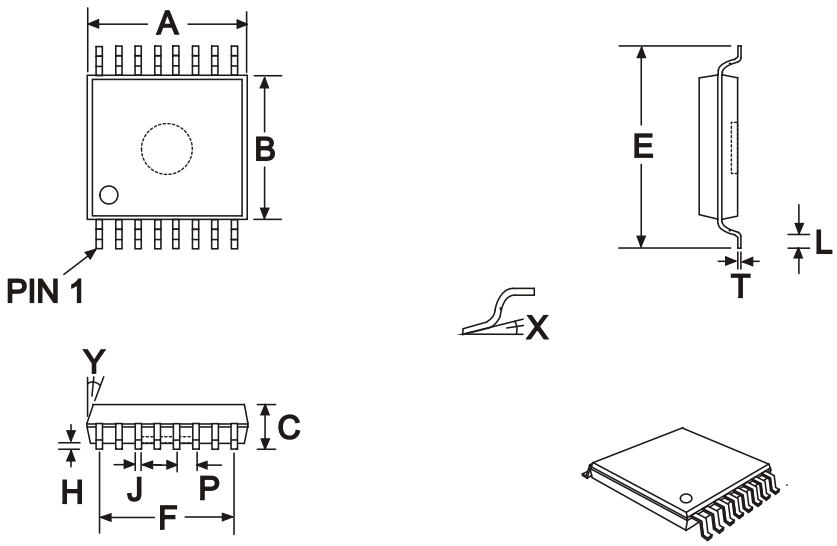
	DIM.	MIN.	TYP.	MAX.
*	A	0.395 (10.03)		0.413 (10.49)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.088 (2.24)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.350 (8.89)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.020 (0.51)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees
Co-Planarity of leads within 0.004" (0.1mm)

Figure 24 16-pin SOIC (D4) Mechanical Outline: *Order as part no. CMX865AD4*



	DIM.	MIN.	TYP.	MAX.
*	A	4.90		5.10
*	B	4.30		4.50
	C	--------		1.20
	E	6.20		6.60
	F		4.55	
	H	0.05		0.15
	J	0.17		0.30
	L	0.45		0.75
	P		0.65	
	T	0.08		0.20
	X	0°		8°
	Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 25 16-pin TSSOP (E4) Mechanical Outline: *Order as part no. CMX865AE4*

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