



ALPHA & OMEGA
SEMICONDUCTOR, LTD

AOD436

N-Channel Enhancement Mode Field Effect Transistor



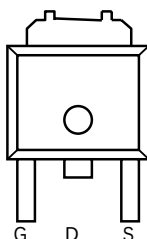
General Description

The AOD436 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. This device is ideally suited for use as a high side switch in CPU core power conversion. *Standard Product AOD436 is Pb-free (meets ROHS & Sony 259 specifications). AOD436L is a Green Product ordering option. AOD436 and AOD436L are electrically identical.*

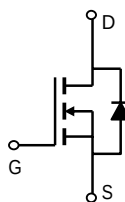
Features

V_{DS} (V) = 30V
 I_D = 60A (V_{GS} = 10V)
 $R_{DS(ON)} < 7.5m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 13m\Omega$ (V_{GS} = 4.5V)

TO-252
D-PAK



Top View
Drain Connected
to Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{B,G}	I_D	60	A
$T_C=25^\circ\text{C}$ ^G			
$T_C=100^\circ\text{C}$ ^B	I_D	43	A
Pulsed Drain Current	I_{DM}	130	
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	113	mJ
Power Dissipation ^B	P_D	50	W
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$	P_D	25	W
Power Dissipation ^A	P_{DSM}	2.5	W
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$	P_{DSM}	1.6	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14.2	20	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	39	50	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case ^C	$R_{\theta JC}$	2	3	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.8	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	85			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$ $T_J=125^{\circ}\text{C}$		5.4 8.1	7.5 9.7	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		9.8	13	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		88		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.71	1	V
I_S	Maximum Body-Diode Continuous Current				85	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=100\text{kHz}$		1520	1825	pF
C_{oss}	Output Capacitance			306		pF
C_{rss}	Reverse Transfer Capacitance			214		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.47	0.7	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$		31.9	39	nC
$Q_g(4.5\text{V})$	Total Gate Charge			16.2	20	nC
Q_{gs}	Gate Source Charge			5		nC
Q_{gd}	Gate Drain Charge			9.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$		7		ns
t_r	Turn-On Rise Time			11.6		ns
$t_{D(off)}$	Turn-Off DelayTime			24.2		ns
t_f	Turn-Off Fall Time			7.7		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		23.8	30	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		15.7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB or heatsink allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by the package current capability.

Rev 4 : July 2005

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

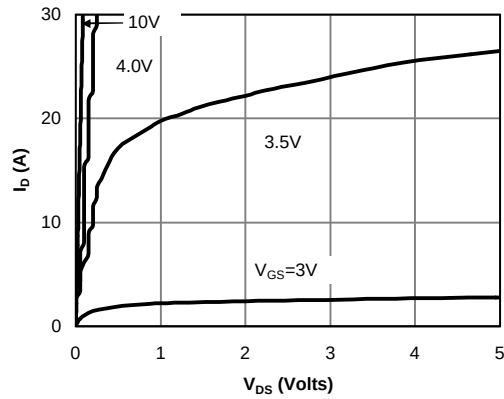


Fig 1: On-Region Characteristics

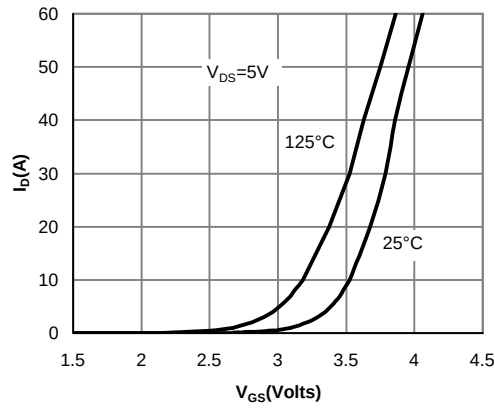


Figure 2: Transfer Characteristics

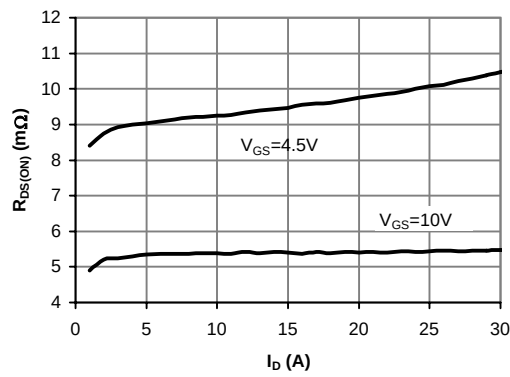


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

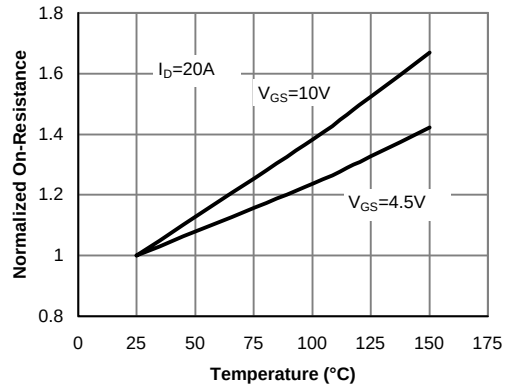


Figure 4: On-Resistance vs. Junction Temperature

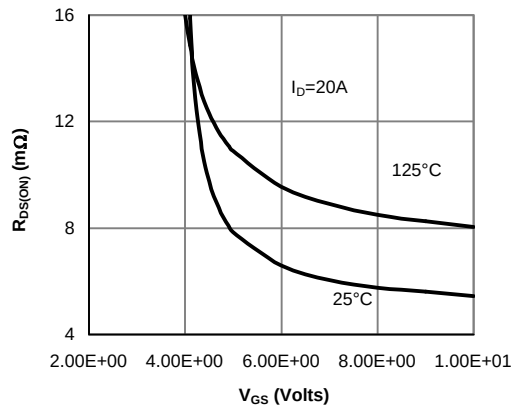


Figure 5: On-Resistance vs. Gate-Source Voltage

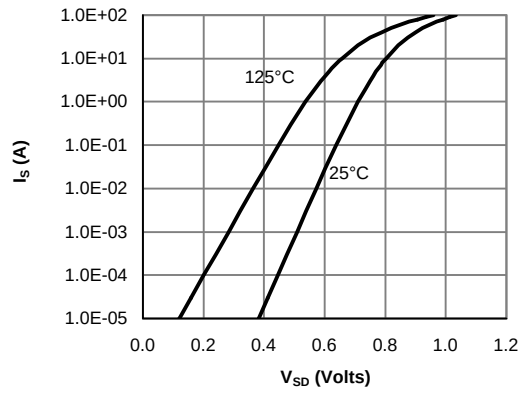


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

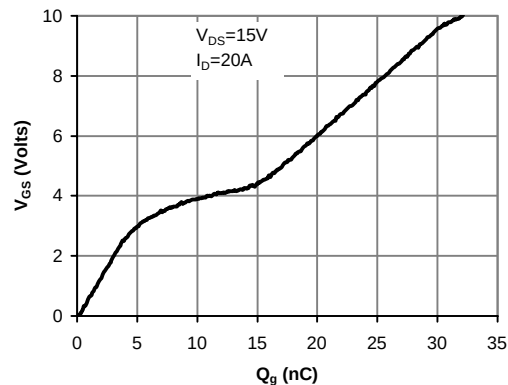


Figure 7: Gate-Charge Characteristics

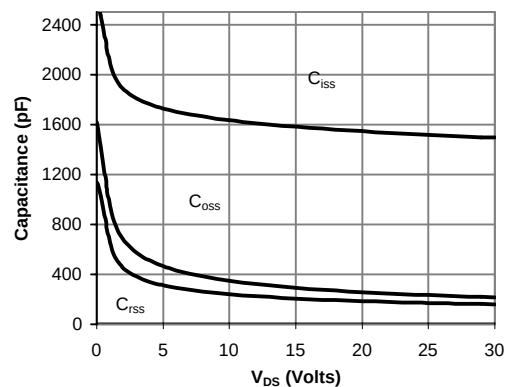


Figure 8: Capacitance Characteristics

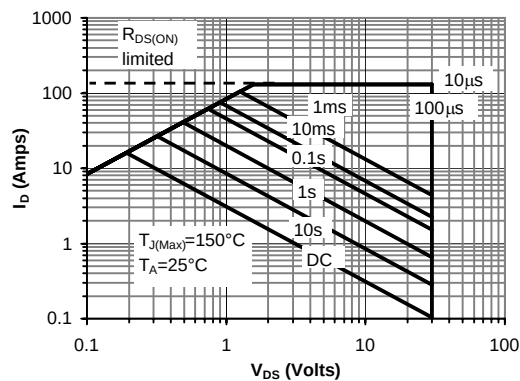


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

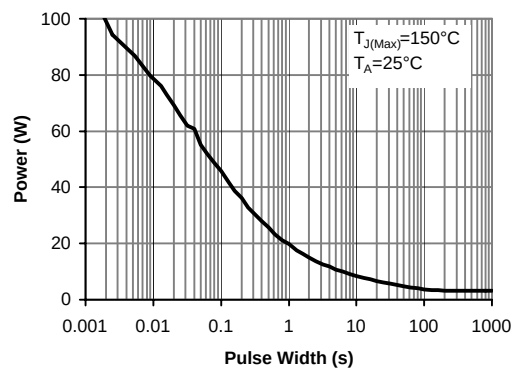


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

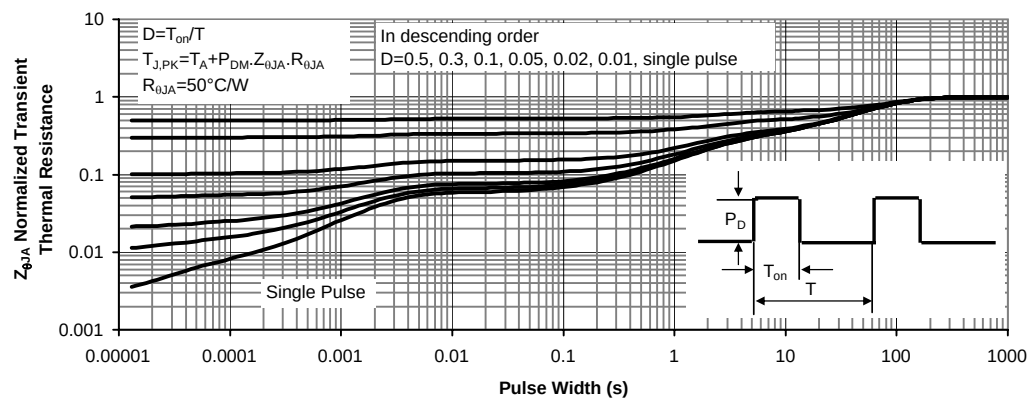


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

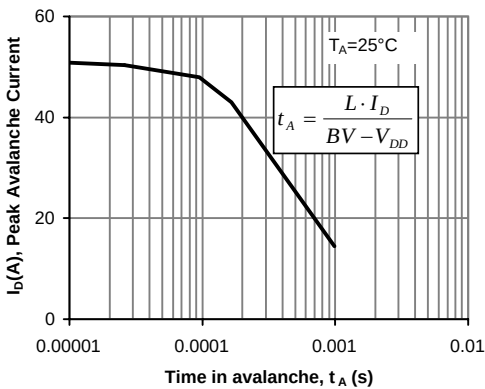


Figure 12: Single Pulse Avalanche capability

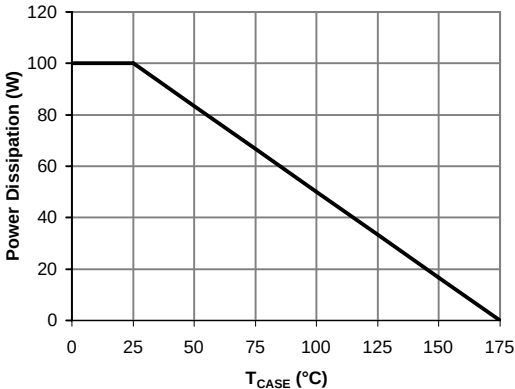


Figure 13: Power De-rating (Note B)

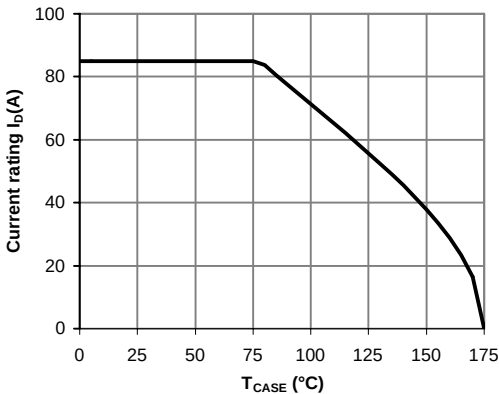


Figure 14: Current De-rating (Note B)