MAXIM

# Very Fast TTL Latched Output Comparators



## General Description

The MAX9686 (Single) and MAX9698 (Dual) are very fast latched TTL comparators manufactured with a high-frequency bipolar process ($f_T$ = 6GHz). They are capable of very short propagation delays, yet maintain the excellent DC characteristics normally found only in slower comparators. The MAX9698 is a dual version of the MAX9686.

The MAX9686 is pin compatible with the LT1016 and Am686, but exceeds the AC characteristics of these devices.

The MAX9686/MAX9698 have differential inputs and complementary outputs that are fully compatible with TTL logic levels. Extremely short propagation delays allow signal processing at frequencies in excess of 200MHz.

When the Latch Enable input goes high, the outputs go to the states defined by the inputs at the time of the latch transition. The outputs remain latched as long as the LE pin remains high. If Latch Enable is not used, LE is tied to ground.

## Applications

High-Speed A/D Converters

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

## Features

- **6ns Propagation Delay**
- **2ns Latch Setup Time**
- **±5V Power Supplies**
- **Pin Compatible to LT1016, Am686 (MAX9686)**
- **Available in Commercial and Military Temp. Ranges**
- **Available in Narrow SO Package**

## Ordering Information

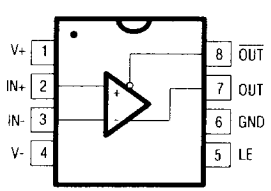
| PART | TEMP. RANGE | PIN - PACKAGE* |
|---|---|---|
| MAX9686BCPA | 0°C to +70°C | 8 Plastic DIP |
| MAX9686BCSA | 0°C to +70°C | 8 Narrow SO |
| MAX9686CJA | 0°C to +70°C | 8 CERDIP |
| MAX9686BC/D | 0°C to +70°C | Dice** |
| MAX9686CTW | 0°C to +70°C | 10 TO-100 Can |
| MAX9686MJA | -55°C to +125°C | 8 CERDIP |
| MAX9686MTW | -55°C to +125°C | 10 TO-100 Can |
| MAX9698BCPE | 0°C to +70°C | 16 Plastic DIP |
| MAX9698BCSE | 0°C to +70°C | 16 Narrow SO |
| MAX9698CJE | 0°C to +70°C | 16 CERDIP |
| MAX9698BC/D | 0°C to +70°C | Dice** |
| MAX9698MJE | -55°C to +125°C | 16 CERDIP |

** Contact factory for availability of 20-Pin LCC*
*** Contact factory for dice specifications.*

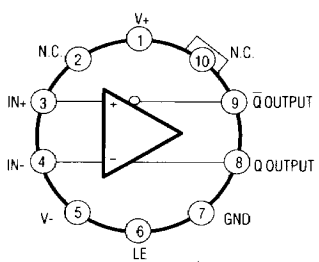


## Pin Configurations

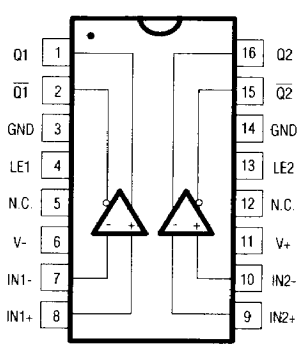
Top View




**MAX9686**
DIP/SO




**MAX9686**
TO-100 Can




**MAX9698**
DIP/SO

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## ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Input Voltages ..... ±5V
Differential Input Voltages ..... 3.5V
Output Current ..... 20mA
Operating Temperature Range:
  Commercial (MAX9686C/9698C) ..... 0°C to +70°C
  Military (MAX9686M/9698M) ..... -55°C to +125°C

Continuous Total Power Dissipation at 70°C:
  8-Pin Plastic DIP (derate 8.3mW/°C above 70°C) ... 660mW
  8-Pin SO (derate 5.9mW/°C above 70°C) ..... 470mW
  8-Pin CERDIP (derate 8.0mW/°C above 70°C) ..... 640mW
  16-Pin Plastic DIP (derate 7.4mW/°C above 70°C) .. 590mW
  16-Pin SO (derate 9.1mW/°C above 70°C) ..... 727mW
  16-Pin CERDIP (derate 10mW/°C above 70°C) ..... 800mW
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

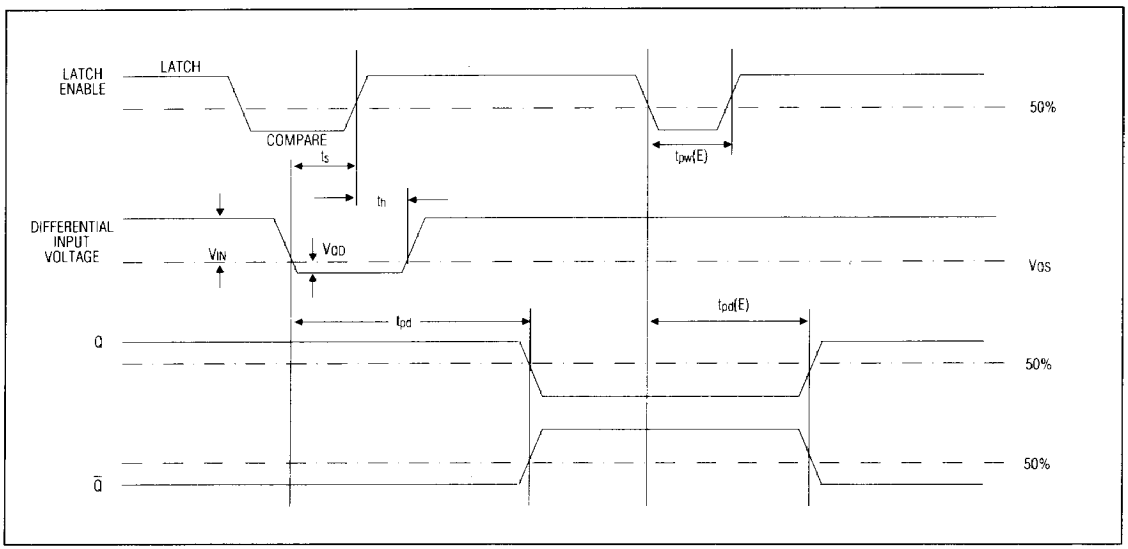
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_S$ = ±5V, $T_A$ = 25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MAX9686C/9698C | | | MAX9686M/9698M | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage<br>MAX96_ _ _J_, MAX9686_TW<br>MAX96_ _BC_ _ | $V_{OS}$ | $R_S$ = 100Ω | | ±1<br>±6 | ±3<br>±9 | | ±1<br>±6 | ±3<br>±9 | mV |
| Temperature Coefficient | $\Delta V_{OS}/\Delta T$ | | | 4 | | | 4 | | µV/°C |
| Input Offset Current | $I_{OS}$ | | | | 5.0 | | | 5.0 | µA |
| Input Bias Current | $I_B$ | | | | 25 | | | 25 | µA |
| Common-Mode Rejection Ratio | CMRR | | 80 | 96 | | 80 | 96 | | dB |
| Power-Supply Rejection Ratio<br>MAX96_ _ _J_, MAX9686_TW<br>MAX96_ _BC_ _ | PSRR | | 70<br>50 | 85<br>65 | | 70<br>50 | 85<br>65 | | dB |
| Input Voltage Range | $V_{CM}$ | | | | ±3.0 | | | ±3.0 | V |
| Latch High Input Voltage | $V_{IH}$ | | 2.0 | | | 2.0 | | | V |
| Latch Low Input Voltage | $V_{IL}$ | | | | 0.8 | | | 0.8 | V |
| Latch Low Input Current | $I_{IL}$ | $V_{LE}$ = 0V | | | -750 | | | -750 | µA |
| I/O Logic Levels<br>Output High Voltage | $V_{OH}$ | $I_{OUT}$ = -3mA | 2.4 | 3.0 | | 2.4 | 3.0 | | V |
| I/O Logic Levels<br>Output Low Voltage | $V_{OL}$ | $I_{OUT}$ = 8mA | | | 0.5 | | | 0.5 | V |
| Positive Supply Current<br>MAX9686<br>MAX9698 | $I_{CC}$ | | | 16<br>32 | 25<br>50 | | 16<br>32 | 25<br>50 | mA |
| Negative Supply Current<br>MAX9686<br>MAX9698 | $I_{EE}$ | | | 13<br>26 | 20<br>40 | | 13<br>26 | 20<br>40 | mA |
| **SWITCHING CHARACTERISTICS (Each Comparator for MAX9698)** (Note 1) | | | | | | | | | |
| Propagation Delay<br>Input to Output High | $t_{pd+}$ | $T_A$ = $T_{MIN}$ to $T_{MAX}$<br>100mV pulse;<br>10mV overdrive | | 6.0 | 9 | | 6.0 | 9 | ns |
| Propagation Delay<br>Input to Output Low | $t_{pd-}$ | $T_A$ = $T_{MIN}$ to $T_{MAX}$<br>100mV pulse;<br>10mV overdrive | | 5.7 | 8.5 | | 5.7 | 8.5 | ns |
| Propagation Delay Skew | $t_{pd+}$ - $t_{pd-}$ | | | 0.3 | | | 0.3 | | ns |
| Latch Setup | $t_S$ | | | 2 | | | 2 | | ns |

**Note 1:** Not tested, guaranteed by design.




*MAX9686 and MAX9698 Timing Diagram*

## Definition of Terms

$V_{OS}$ Input Offset Voltage

$V_{OD}$ Input Voltage Overdrive

$t_{pd+}$ Input to Output High Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.

$t_{pd-}$ Input to Output Low Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.

$t_{pd+}(E)$ Latch Enable to Output High Delay -- The propagation delay measured from the 50% point of the Latch Enable signal high to low transition to the 50% point of an output low to high transition.

$t_{pd-}(E)$ Latch Enable to Output Low Delay -- The propagation delay measured from the 50% point of the Latch Enable signal high to low transition to the 50% point of an output high to low transition.

$t_{pw}(E)$ Minimum Latch Enable Pulse Width -- The minimum time the Latch Enable signal must be low to acquire and hold an input signal.

$t_s$ Minimum Setup Time -- The minimum time, before the positive transition of the Latch Enable pulse, that an input signal must be present to be acquired and held at the outputs.

$t_h$ Minimum Hold Time -- The minimum time, after the positive transition of the Latch Enable signal, that an input signal must remain unchanged to be acquired and held at the output.

# Very Fast Latched TTL Output Comparators

## Application Information

### Layout

Because of the large gain-bandwidth characteristic of the MAX9686/MAX9698, special precautions need to be taken if the high-speed capabilities of the devices are to be realized. A PC board with ground plane is mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins. For low impedance applications, microstrip layout at the input may be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. To minimize lead inductance, chip components can be used. If Latch Enable is not used, it must be connected to ground.

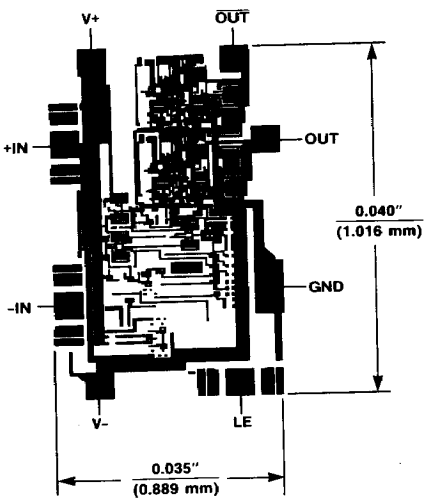
### Input Slew Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices may create oscillation problems when the input traverses through the comparator's linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. Output oscillation is best avoided with compact PC board layout and minimum input signal source impedance. Poor layout and larger source impedance will increase the minimum slew rate required to avoid oscillation.

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew rate requirement considerably. For example, the minimum slew rate can be reduced by a factor of 4 with the addition of positive feedback components Rf = 1kΩ and Cf = 100pF.

## Chip Topographies

MAX9686




MAX9698