Radiation Hardened Low Dropout Adjustable Negative Voltage Regulator

ISL72991RH

The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM) and a shutdown pin (SD) for easy on/off control.

The device incorporates unique circuitry that enables precision performance over the -55°C to +125°C temperature range and post-irradiation. Specifications over the full temperature range include an internal reference voltage of -1.25V +40mV/-50mV (max), line regulation of ±25mV (max), and load regulation of ±15mV (max). The reference voltage is the ADJ to GND voltage.

Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to Single Event Latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Applications

- Post Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Features

- Electrically Screened to DLA SMD # 5962-02503
- QML Qualified per MIL-PRF-38535 Requirements
- Latch-Up Immune DI Process
- Wide Input Voltage Range . . . . . - 3V to - 30V
- Output Voltage Range . . . . . -2.25V to -26V
- Line Regulation . . . . . ±25mV (max)
- Load Regulation . . . . . ±12mV (typ); ±15mV (max)
- Dropout Voltage (100mA) . . . . . 0.2V (typ); 0.3V (max)
- Dropout Voltage (1A) . . . . . 1V (max)
- Minimum Load Current 3.0mA
- TTL Input-Level Shutdown (SD); Low = On
- Operating Temperature Range . . . . . -55°C to +125°C
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - SEL/SEB LET_{TH} (V_S = -30V) . . . . . 86.4 MeV•cm^2/mg
  - Total Dose, High Dose Rate . . . . . 300krad(Si)

Related Literature

- TID, "Low Dose Rate Testing of the Intersil ISL72991RH Negative Low Dropout Regulator"
- SEE, "Single Effects Testing of the ISL72991RH Adjustable Voltage Regulator"

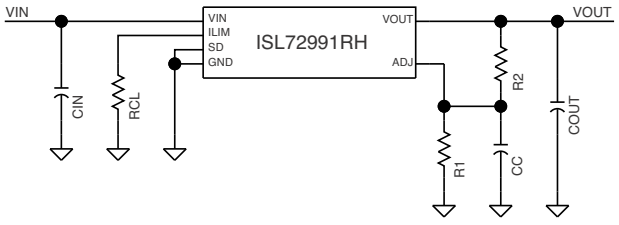


FIGURE 1. TYPICAL APPLICATION

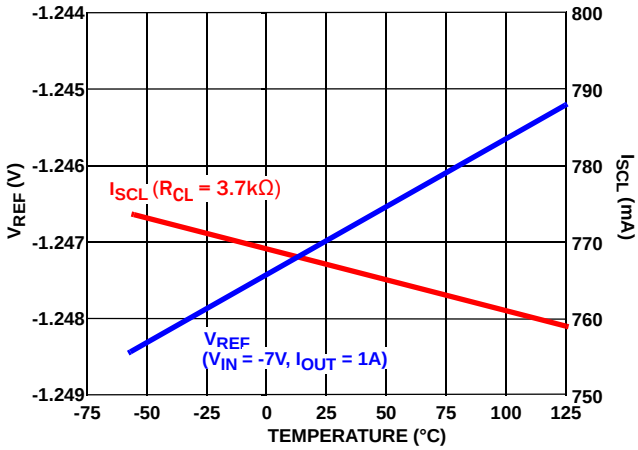


FIGURE 2. V_{REF} and I_{SCL} vs TEMPERATURE

Ordering Information

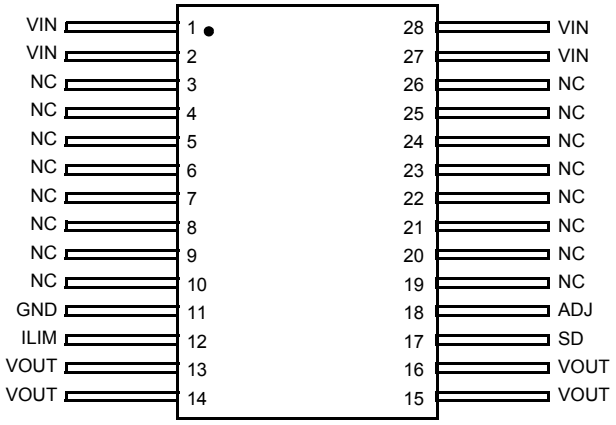
ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F0250301VXC	ISL72991RHVF	-55 to +125	28Ld Flatpack	K28.A
5962F0250301QXC	ISL72991RHQF	-55 to +125	28 Ld Flatpack	K28.A
5962F0250301V9A	ISL72991RHVX	-55 to +125	DIE	
ISL72991RHF/PROTO	ISL72991RHF/PROTO	-55 to +125	28 Ld Flatpack	K28.A

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

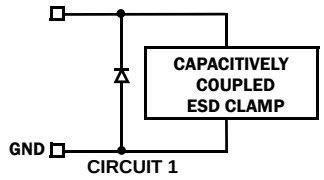
Pin Configuration

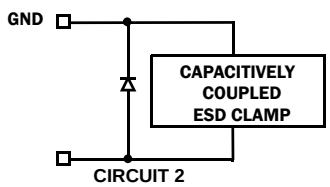
ISL72991RH
(28 LD FLATPACK)
TOP VIEW



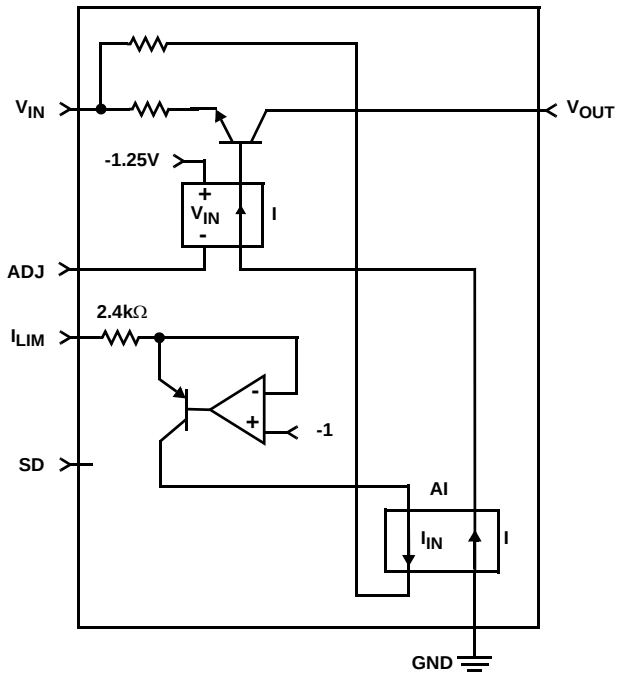
Pin Descriptions

ISL72991RH (28 LD FLATPACK)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1, 2, 27, 28	VIN	Circuit 2	Regulator Bias and Input Connection. All 4 pins must be tied together.
12	ILIM	Circuit 2	Current Limiting Set Input
13, 14, 15, 16	VOUT	Circuit 2	Regulator Output Connection. All 4 pins must be tied together.
17	SD	Circuit 1	Shut Down Input, active high.
18	ADJ	Circuit 2	Output Voltage Adjust Input
11	GND		Ground Connection
3, 4, 5, 6, 7, 8, 9, 10, 19, 20, 21, 22, 23, 24, 25, 26	NC		No Internal connections. Can be connected to ground or thermal plane.

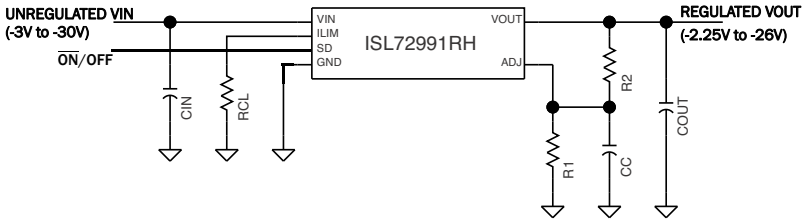




Functional Block Diagram



Typical Application



- VDC TO -VDC VOLTAGE REGULATION CIRCUIT

Absolute Maximum Ratings

Minimum Supply Voltage. . . . . -35V
Minimum Supply Voltage (Note 5) . . . . . -30V
Minimum Output Current 3mA
Output Short-Circuit Duration. Thermal Protection. . . . . Indefinite
ESD Rating
Human Body Model (HBM) (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (MM) (Tested per EIA/JESD22-A115-A) 300V
Charged Device Model (CDM) (Tested per JESD22-C101D) 200V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld Flatpack (Notes 3, 4).	60	5

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Supply Voltage . . . . . -3V to -30V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.
5. The minimum supply limit specified is for operation in a heavy ion environment at an LET = 86.4MeV*cm^2/mg.

Electrical Specifications

$V_O \leq$ VIN -1.5V, I_O = 100mA, C_O = 47µF, SD = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{REF}	Reference Voltage	I_O = 3mA to 1A	-1.279	-1.25	-1.231	V
			-1.300		**-1.210**	V
V_{Omin}	Minimum Output Voltage	V_{IN} = -3V, I_O = 3mA to 100mA	**-**		**-2.25**	V
V_{Omax}	Maximum Output Voltage	V_{IN} = -30V, I_O = 3mA to 100mA	**-26**		**-**	V
V_{LDR}	Output Voltage Load Regulation	V_{IN} = -7V, V_O = -5V I_O = 3mA to 1A	-12		12	mV
			-15		**15**	mV
V_{LNR}	Output Voltage Line Regulation	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 100mA	**-25**		**25**	mV
V_{DOL}	0.1A Drop Out Voltage	$dV_O \leq$ 50mV, I_O = 0.1A			0.2	V
					0.3	V
V_{DOH}	1A Drop Out Voltage (Pulse Tested)	$dV_O \leq$ 50mV, I_O = 1A			**1**	V
I_{ADJ}	Adjust Current	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 500mA		1.7	**5**	µA
I_{QDO}	Drop Out Quiescent Current	V_O - V_{IN} = 0.2V, I_O = 500mA			25	mA
		V_O - V_{IN} = 0.3V, I_O = 500mA			**25**	mA
V_{SD}	SD Input Voltage	V_O = ON			**0.8**	V
		V_O = OFF	**2.4**			V
I_{SD}	SD Input Current	V_{SD} = 0.8V			**50**	µA
		V_{SD} = 2.4V			100	µA
					150	µA
I_{SCL}	Output Short Circuit Current Limit	V_{IN} = - 7V, V_O = 0V, R_{CL} = 3.7kΩ	**0.6**	0.75	**0.9**	A
I_{GND}	GND Quiescent Current	-3V≤ V_{IN} ≤ -30V, I_O < 1A		6		mA
PSRR	Power Supply Rejection Ratio	Frequency = 1MHz		-49		dB
OT_{PROT}	Thermal Protection			150		°C
OT_{HYS}	Thermal Hysteresis			20		°C

Post Radiation Electrical Specifications

$V_O \leq VIN$ -1.5V, I_O = 100mA, C_O = 47µF, SD = 0V, T_A = +25°C, over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300rad(Si)/s.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{REF}	Reference Voltage	I_O = 3mA to 1A	-1.279		-1.231	V
V_{Omin}	Minimum Output Voltage	V_{IN} = -3V, I_O = 3mA to 100mA	-		-2.25	V
V_{Omax}	Maximum Output Voltage	V_{IN} = -30V, I_O = 3mA to 100mA	-26		-	V
VLDR	Output Voltage Load Regulation	V_{IN} = -7V, V_O = -5V I_O = 3mA to 1A	-12		12	mV
VLNR	Output Voltage Line Regulation	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 100mA	-25		25	mV
VDO_L	0.1A Drop Out Voltage	$dV_O \leq$ 50mV, I_O = 0.1A			0.2	V
VDO_H	1A Drop Out Voltage (Pulse Tested)	$dV_O \leq$ 50mV, I_O = 1A			1	V
I_{ADJ}	Adjust Current	$V_O \leq V_{IN}$ -1V to V_{IN} = -30V, I_O = 500mA			5	µA
I_{QDO}	Drop Out Quiescent Current	V_O - V_{IN} = 0.3V, I_O = 500mA			25	mA
V_{SD}	SD Input Voltage	V_O = ON			0.8	V
		V_O = OFF	2.4			V
I_{SD}	SD Input Current	V_{SD} = 0.8V			50	µA
		V_{SD} = 2.4V			100	µA
I_{CL}	Output Short Circuit Current Limit	V_{IN} = - 7V, V_O = 0V, R_{CL} = 3.7kΩ	0.6		0.9	A

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Total Dose Radiation Characteristics This data is typical mean test data post total dose radiation exposure at a high dose rate (HDR) of 50 to 300rad(Si)/s to 300krads. This data is intended to show typical parameter shifts due to total dose rate radiation. These are not limits nor are they guaranteed.

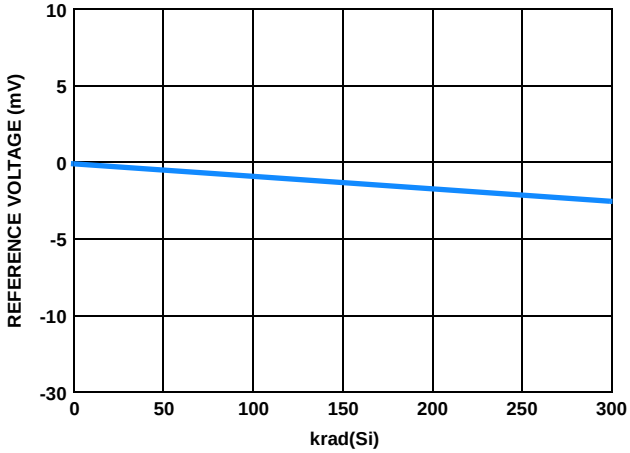


FIGURE 3. REFERENCE VOLTAGE CHANGE vs TOTAL DOSE RADIATION

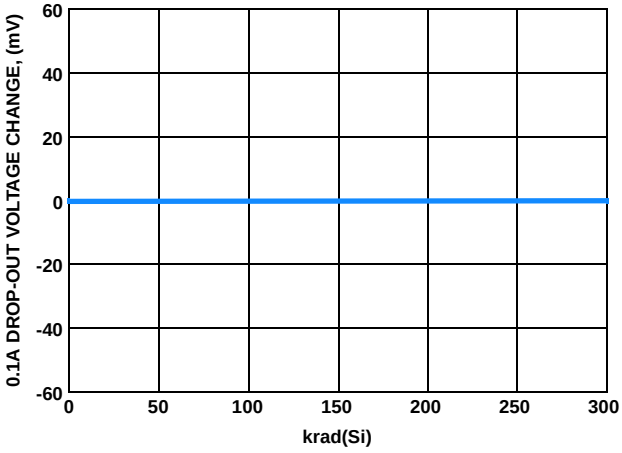


FIGURE 4. 0.1A DROP-OUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

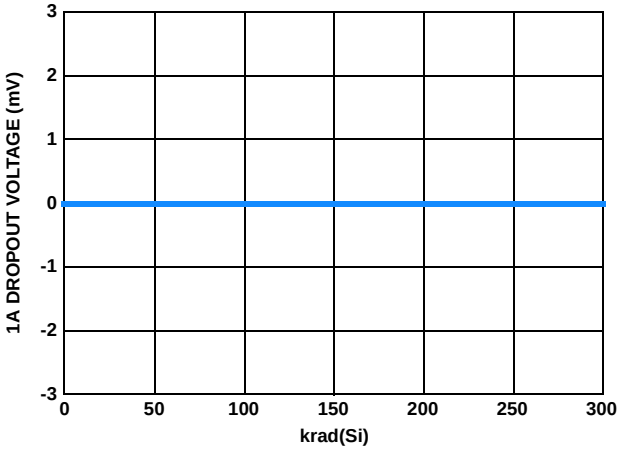


FIGURE 5. 1A DROP-OUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

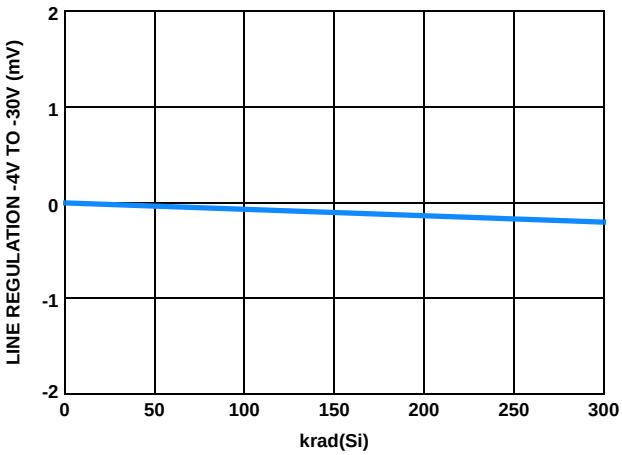


FIGURE 6. OUTPUT VOLTAGE LINE REGULATION CHANGE vs TOTAL DOSE RADIATION

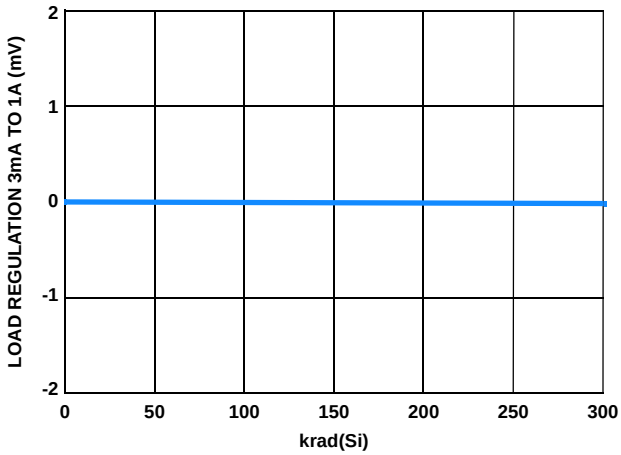


FIGURE 7. OUTPUT VOLTAGE LOAD REGULATION CHANGE vs TOTAL DOSE RADIATION

Typical Performance Curves

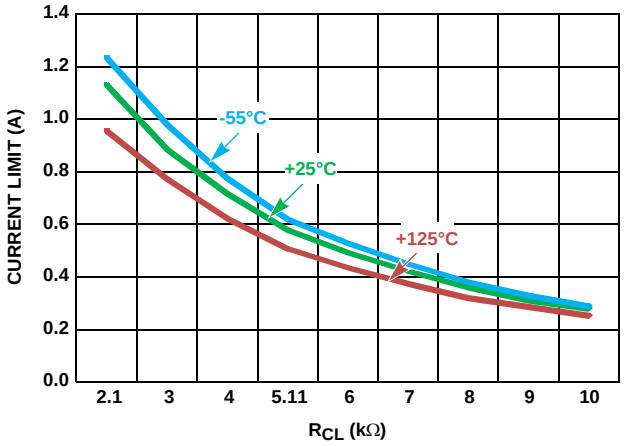


FIGURE 8. $-7V_{IN}$, $-5V_{OUT}$

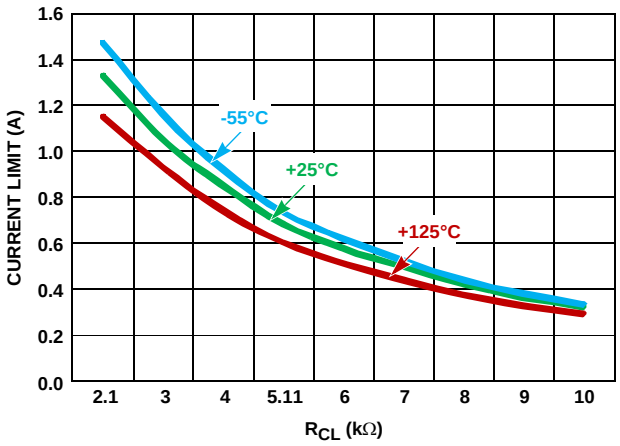


FIGURE 9. $-12V_{IN}$, $-5V_{OUT}$

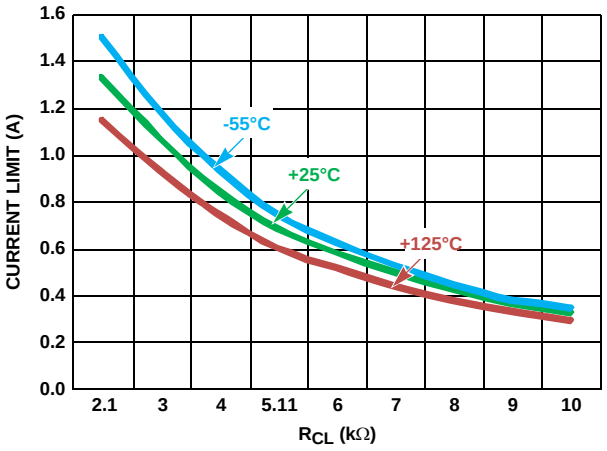


FIGURE 10. $-12V_{IN}$, $-10V_{OUT}$

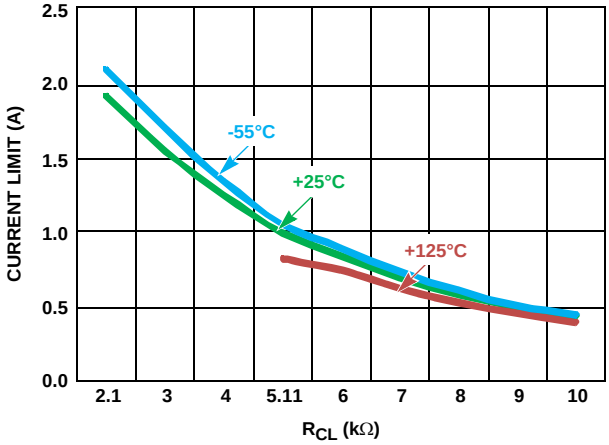


FIGURE 11. $-20V_{IN}$, $-10V_{OUT}$

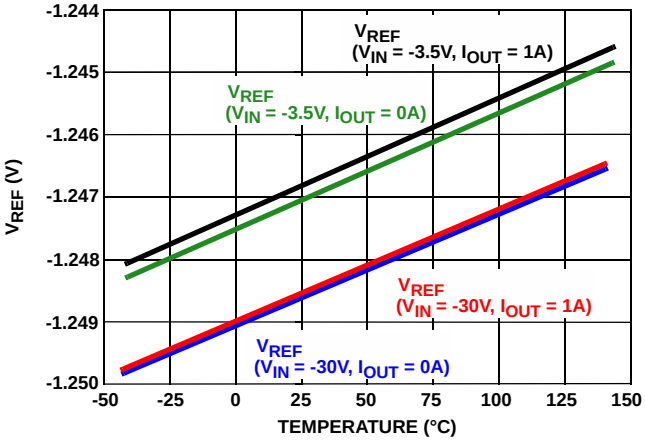


FIGURE 12. V_{REF} vs TEMPERATURE

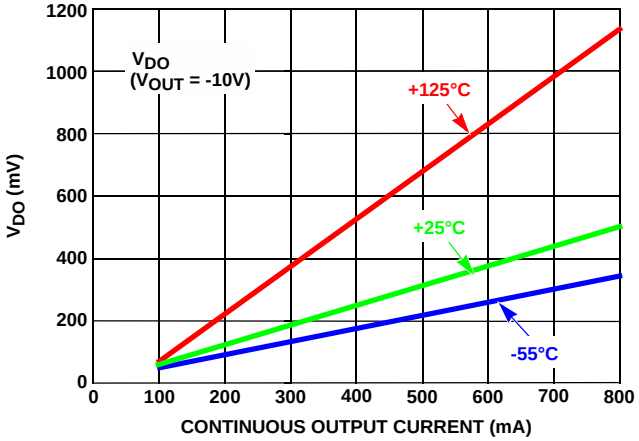


FIGURE 13. DROP_OUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

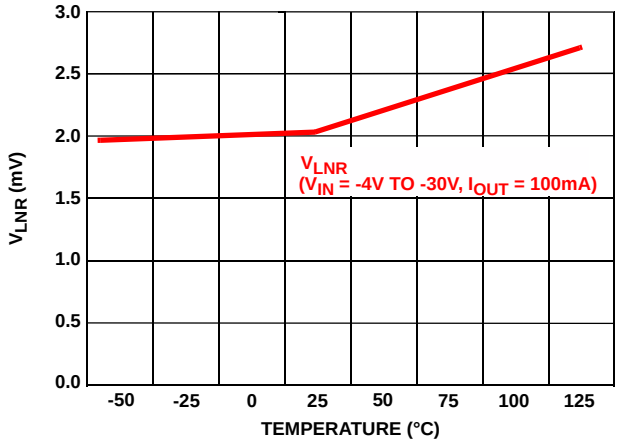


FIGURE 14. LINE REGULATION vs TEMPERATURE

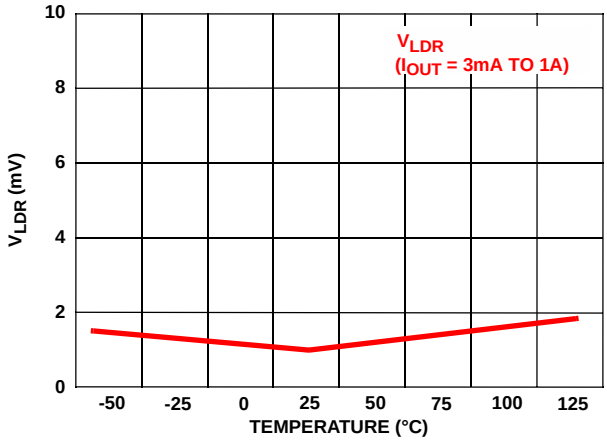


FIGURE 15. LOAD REGULATION vs TEMPERATURE

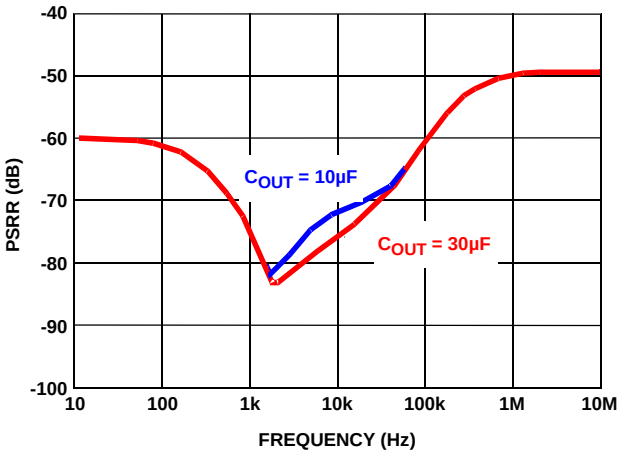


FIGURE 16. PSRR vs FREQUENCY (V_{IN} = -20V, V_{OUT} = -18V)

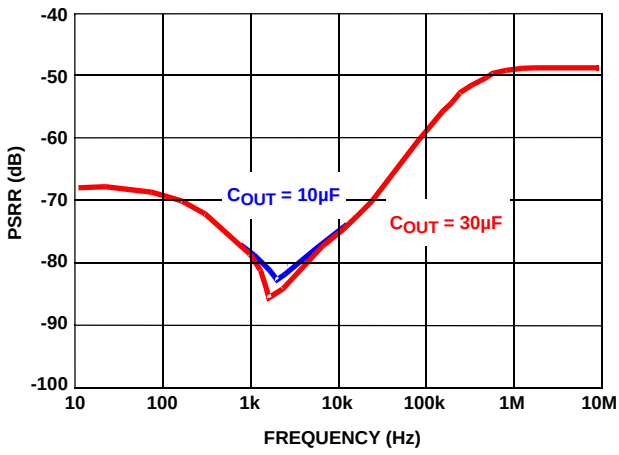


FIGURE 17. PSRR vs FREQUENCY (V_{IN} = -7V, V_{OUT} = -5V)

Functional Description

Functional Overview

The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM) and a shutdown pin (SD) for easy on/off control. The part is constructed using the Intersil dielectrically isolated, complimentary bipolar RSG process. It is immune to single-event latch-up and has been specifically designed to provide reliable performance in harsh radiation environments.

Application Information

Output Voltage Programming

The output voltage of the regulator can be programmed with two external resistors and is described by Equation 1:

$$V_{OUT} = -1.25 \times (1 + R2/R1) - (I_{ADJ} \times R2) \quad \text{(EQ. 1)}$$

Output Current Limit Programming

The output current limit threshold of the regulator is set with a single external resistor (R_{CL}) connected from I_{LIM} to ground.

The effective current limit at any single R_{CL} value is influenced by the V_{IN} to V_{OUT} difference, temperature and V_{IN} amplitude. Figures 18 through 20 illustrate these effects.

Figure 18 shows that for a given V_{OUT} (-5V) and temperature (+25°C) the effect of V_{IN} to V_{OUT} differential on the current limit level is significant.

Figure 19 shows the effect of temperature at a single V_{IN} to V_{OUT} voltage condition across the R_{CL} range of 2.1kΩ to 10kΩ.

Figure 20 shows that for a given differential voltage (V_{IN} to V_{OUT}) and temperature the effect of V_{IN} amplitude is less significant than seen in Figure 18.

Because of these numerous variables, there is no one formula relating R_{CL} to I_{CL} that will suffice for the range of likely possible conditions. Figures 8 through 11 provide guidance in setting the R_{CL} value for a limited number of possible conditions. Users are advised to evaluate their specific condition for satisfactory performance.

Capacitor Selection

An input capacitor is required if the regulator is located more than 6 inches from the power supply filter capacitors. A 10µF solid tantalum capacitor is recommended.

An output capacitor of at least 10µF must be used to insure stability of the regulator. Additional capacitance may be added as required to improve the dynamic response of the regulator. Solid tantalum or ceramic capacitors are recommended.

Loop Compensation

The output capacitor and ESR comprise a zero in the loop transfer function that must be compensated with a pole to insure loop stability in accordance with Equation 2:

$$C_C \times R2 = C_{OUT} \times ESR \quad \text{(EQ. 2)}$$

The compensating capacitor should be a low ESR ceramic type.

Layout Guidelines

The stability of the regulator is sensitive to layout. It is strongly recommended that a continuous copper ground plane (1 ounce or greater) be used. In addition, component lead lengths and interconnects should be minimized, but should not exceed 1/2 inch. Finally, the return lead of the compensation capacitor (C_C) should be connected as close as possible to the GND pin of the IC.

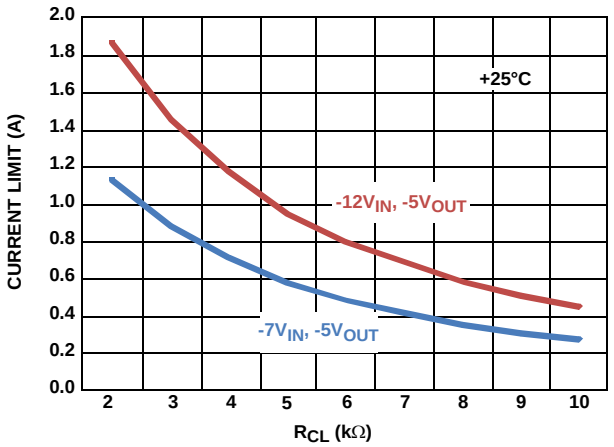


FIGURE 18. I_{CL} vs R_{CL} and V_{IN} AMPLITUDE

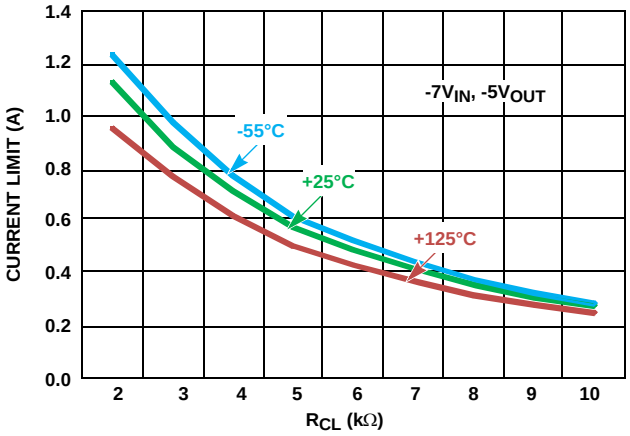


FIGURE 19. I_{CL} vs R_{CL} and TEMPERATURE

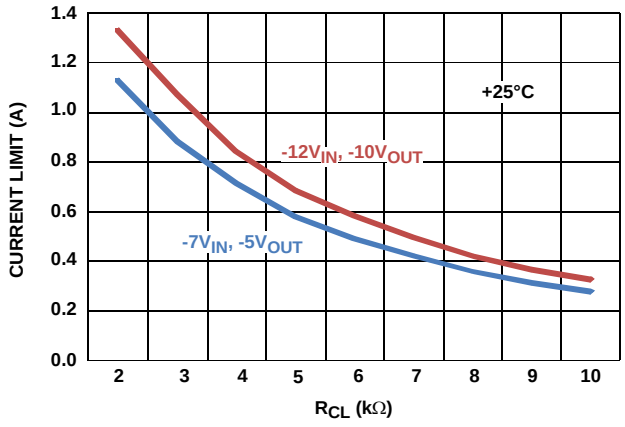


FIGURE 20. I_{CL} vs R_{CL} and V_{IN} TO V_{OUT} DIFFERENTIAL

Package Characteristics

Weight of Packaged Device

2.2 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased
Case Isolation to Any Lead: 20 x 10^9 Ω (min)

Die Characteristics

Die Dimensions

5870µm x 5210µm (231.1mils x 205.1mils)
Thickness: 483µm ± 25.4µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type:PSG (Phosphorous Silicon Glass
Thickness: 8.0kÅ ± 1.0kÅ

TOP METALLIZATION

Type: AlSiCu (Si 0.75-1%/Cu 0.5%)
Thickness: 16.0kÅ ± 2kÅ

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Floating

ADDITIONAL INFORMATION

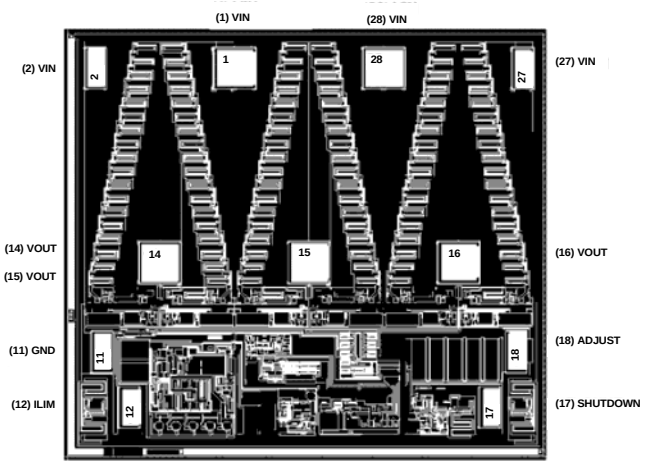
Worst Case Current Density

< 2 x 10^5 A/cm^2

PROCESS

Dielectrically Isolated Radiation Hardened Silicon Gate

Metallization Mask Layout



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

DATE	REVISION	CHANGE
March 26, 2014	FN9054.2	Added Related Literature on page 1. Added significant relevant content throughout the document, expanding from 3 to 12 pages.
June, 28, 2004	FN9054.1	Updated file.
July 9, 2001	FN9054.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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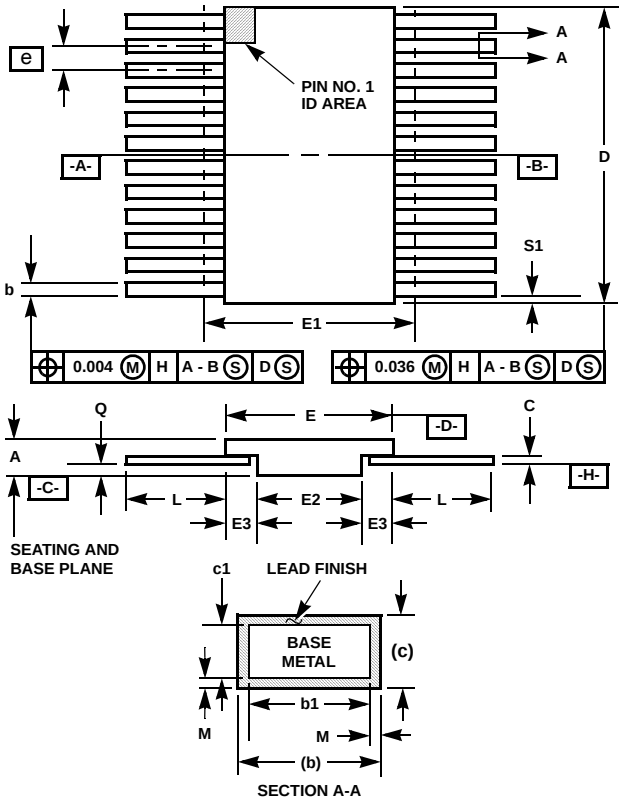
Package Outline Drawing

Ceramic Metal Seal Flatpack Packages (Flatpack)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.