TOSHIBA Bi−CMOS INTEGRATED CIRCUIT   SILICON MONOLITHIC

TB62701AN

16BIT SHIFT REGISTER, LATCH & CONSTANT CURRENT DRIVERS

The TB62701AN is specifically designed for LED and
LED−DISPLAY constant current drivers.
This constant current output circuit is able to set up external
resister (I_{OUT} = 5 to 50mA).
This IC is monolithic integrated circuit designed to be used
together with Bi−CMOS process.
The devices consist of 16bit Shift Register, Latch, AND−GATE
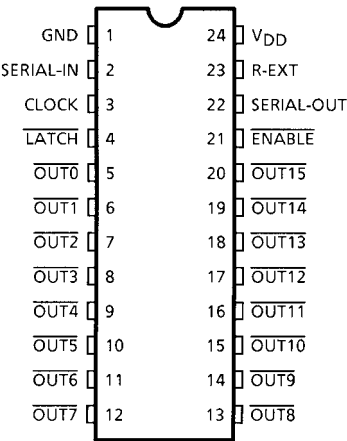and Constant Current Driver.

SDIP24-P-300-1.78
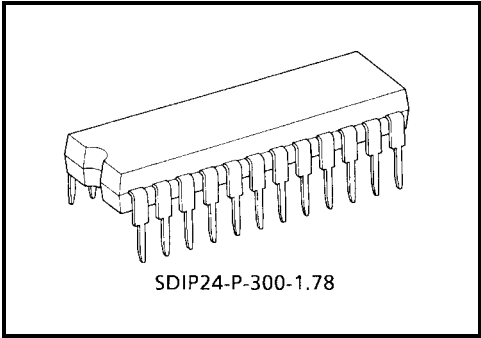
Weight: 1.22 g (typ.)

FEATURES

- OUTPUT CURRENT： Set−up at 50mA maximum with an
  external resister.
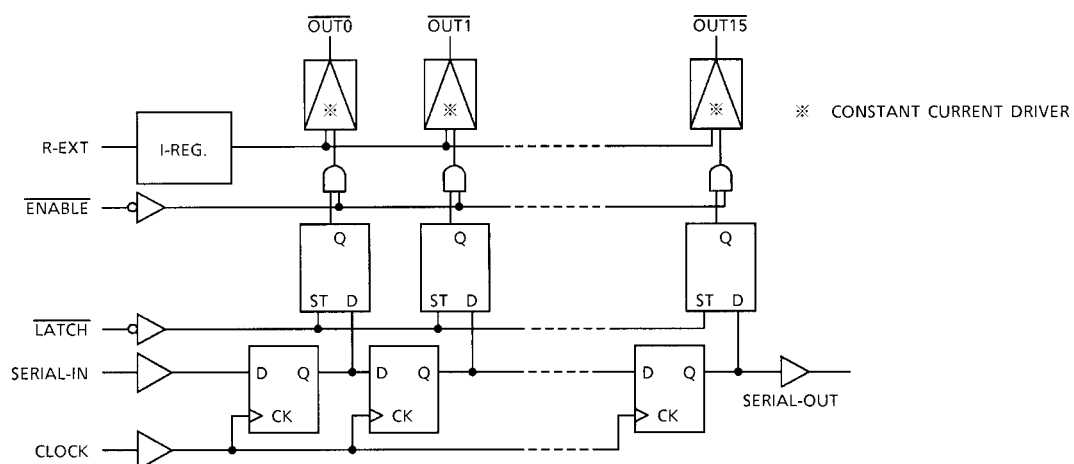- A LITTLE CHANGE OF OUTPUT CURRENT (Ta = 25°C, V_{DD} = 5.0 V)

OUTPUT−GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	I_{OUT} [mA]
≥ 0.4 V	± 7 %	5 ~ 50 mA
≥ 0.7 V		

- 5V CMOS Compatible Input
- PACKAGE   ：   SDIP−24 (SDIP24−P−300)
- MAXIMUM CLOCK FREQUENCY   ： f_{MAX} = 2.5 MHz (cascade operation, Ta = 25°C)
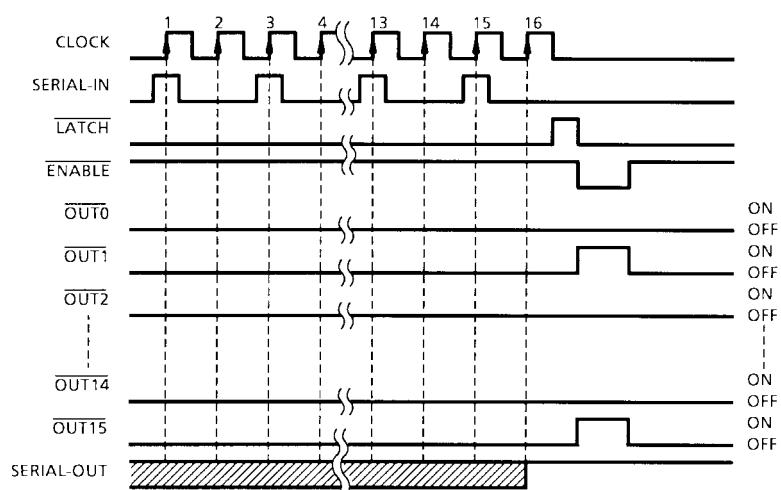
PIN CONNECTION (TOP VIEW)

GND	1	24	V_{DD}
SERIAL-IN	2	23	R-EXT
CLOCK	3	22	SERIAL-OUT
$\overline{\text{LATCH}}$	4	21	$\overline{\text{ENABLE}}$
$\overline{\text{OUT0}}$	5	20	$\overline{\text{OUT15}}$
$\overline{\text{OUT1}}$	6	19	$\overline{\text{OUT14}}$
$\overline{\text{OUT2}}$	7	18	$\overline{\text{OUT13}}$
$\overline{\text{OUT3}}$	8	17	$\overline{\text{OUT12}}$
$\overline{\text{OUT4}}$	9	16	$\overline{\text{OUT11}}$
$\overline{\text{OUT5}}$	10	15	$\overline{\text{OUT10}}$
$\overline{\text{OUT6}}$	11	14	$\overline{\text{OUT9}}$
$\overline{\text{OUT7}}$	12	13	$\overline{\text{OUT8}}$

BLOCK DIAGRAM

TIMING DIAGRAM

TERMINAL DESCRIPTION

| PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL−IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up−edge
4	$\overline{\text{LATCH}}$	"H" Level : data through, "L" Level : data hold
24	V_{DD}	Supply voltage terminal
5~12 13~20	$\overline{\text{OUTn}}$	Output terminals
21	$\overline{\text{ENABLE}}$	"H" Level output off, "L" Level : latch data = "H" Level then output on, latch data = "L" Level then output off
22	SERIAL−OUT	Serial data output terminal for shift register
23	R−EXT	The register which connects between R−EXT and GND sets the constant output current.

TRUTH TABLE

INPUT				OUTPUT $\overline{\text{OUTn}}$ (t = n)			
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL−IN	$\overline{\text{OUT0}}$ ···	$\overline{\text{OUT7}}$ ···	$\overline{\text{OUT15}}$	SERIAL−OUT
⌐_	H	L	D_n	D_n	D_{n-7}	D_{n-15}	D_{n-15}
⌐_	L	L	D_n	No change			D_{n-15}
⌐_	(Note)	H	D_n	OFF	OFF	OFF	D_{n-15}
‾⌐	(Note)	(Note)	D_n	No change			No change

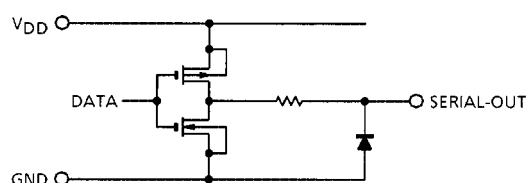Note: $D_n \sim D_{n-15}$ = "H" then OUTn is ON, "L" then OUTn is OFF.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. $\overline{\text{ENABLE}}$ terminal
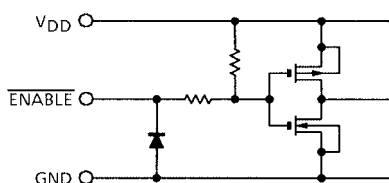
2. $\overline{\text{LATCH}}$ terminal
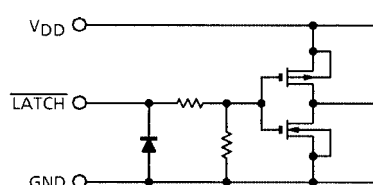
3. CLOCK, SERIAL−IN terminal
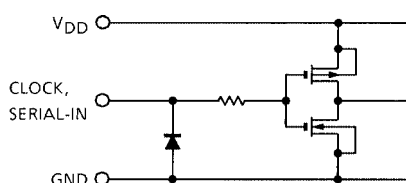
4. SERIAL−OUT terminal

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Output Voltage	V_{CE}	−0.5~30	V
Output Current	I_{OUT}	50	mA
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
GND Terminal Current	I_{GND}	800	mA
Clock Frequency	f_{CK}	2.5	MHz
Power Dissipation (Note)	P_D	1.78	W
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note: Ambient temperature delated above 25°C in the proportion of 14.2 mW / °C.

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C unless otherwise noted)

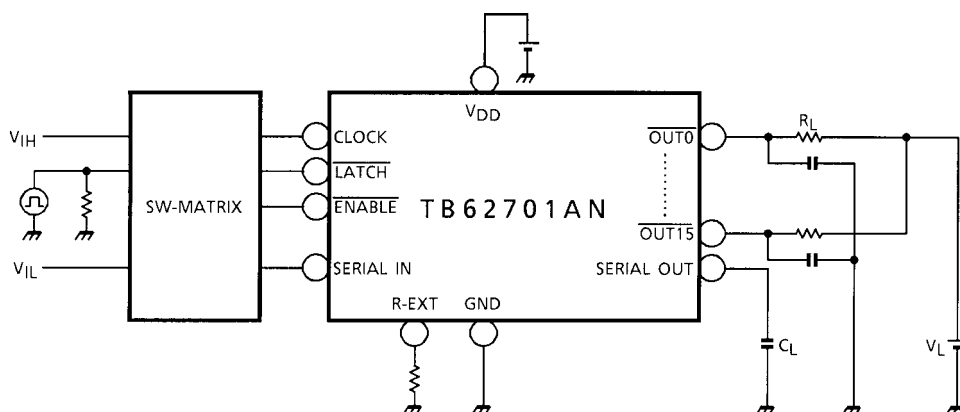| CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V_{DD}	—	4.5	5.0	5.5	V
Output Voltage		V_{OUT}	—	—	—	30.0	V
Output Current	$\overline{OUTn}$	I_{OUT}	DC 1 circuit	—	—	45	mA
	S−OUT	I_{OH}	—	—	—	−1.0	
		I_{OL}	—	—	—	1.0	
Input Voltage		V_{IN}	—	0	—	V_{DD}	V
Data Set Up Time		$t_{setup (D)}$	—	100	—	—	ns
Data Hold Time		$t_{hold (D)}$	—	20	—	—	ns
Data Set Up Time		$t_{setup (L)}$	—	300	—	—	ns
Data Hold Time		$t_{hold (L)}$	—	100	—	—	ns
Clock Pulse Width		$t_{W\ CLK}$	—	100	—	—	ns
		$t_{W\ \overline{CLK}}$	—	100			ns
Latch Pulse Width		$t_{W\ LAT}$	—	300	—	—	ns
		$t_{W\ \overline{LAT}}$	—	300			ns
Clock Frequency		f_{CK}	Cascade operation	—	—	2.0	MHz
Power Dissipation		P_D	Ta = 85°C	—	—	0.72	W

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR–CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Leakage Current	"H" level	V_{IH}	—	—		70% V_{DD}	—	V_{DD}	V
	"L" level	V_{IL}	—	—		GND	—	30%V_{DD}	
Output Leakage Current		I_{OH}	—	V_{OH} = 30V		—	—	10	µA
Output Votltage	S–OUT	V_{OL}	—	I_{OL} = +1.0 mA		—	—	0.4	V
		V_{OH}	—	I_{OH} = −1.0 mA		4.6	—	—	
Output Current 1		I_{OL1}	—	V_{CE} = 0.7 V	R_{EXT} = 560 Ω (included ΔI_{OL1})	35.2	41.5	47.7	mA
		I_{OL2}	—	V_{CE} = 0.4 V		33.1	39.0	44.9	
	Delta I_{OUT}	ΔI_{OL1}	—	R_{EXT} = 560 Ω I_{OUT} = 40 mA, V_{CE} = 0.4 V		—	±3.0	±7.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 560 Ω		—	18	—	% / V
Reference Voltage		V_{ref}	—	R_{EXT} = 560 Ω, Ta = −40~85°C		—	1.26	—	V
Pull Up / Down Resister		R_{IN}	—	—		100	200	400	kΩ
Supply Current	"OFF"	$I_{DD (off) 1}$	—	R_{EXT} = OPEN, OUTn = Off		—	0.4	0.6	mA
		$I_{DD (off) 2}$	—	R_{EXT} = 560 Ω, OUTn = Off		—	6.5	10.0	
	"ON"	$I_{DD (on)}$	—	R_{EXT} = 560 Ω, All output on		—	13.5	20.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK−S−OUT	t_{pLH}	V_{DD} = 5.0 V V_{CE} = 1.0 V V_{IH} = V_{DD} V_{IL} = GNK f_{CK} = 2 MHz R_{EXT} = 560 Ω I_{OUT} = 30 mA	—	95	500	ns
	CLK- $\overline{OUTn}$			—	130	500	
	$\overline{LATCH}$ - $\overline{OUTn}$			—	130	500	
	$\overline{EN}$ - $\overline{OUTn}$			—	130	500	
Propagation Delay Time ("H" to "L")	CLK−S−OUT	t_{pHL}		—	95	720	ns
	CLK- $\overline{OUTn}$			—	130	500	
	$\overline{LATCH}$ - $\overline{OUTn}$			—	130	500	
	$\overline{EN}$ - $\overline{OUTn}$			—	130	500	
Maximum Clock Frequency		f_{MAX} (Note 1)		2.0	—	2.5	MHz
Minimum Pulse Width	CLK	$t_{W\ CLK}$		—	45	80	ns
	$\overline{LATCH}$	$t_{W\ \overline{LAT}}$		—	10	50	
Data Set Up Time		$t_{setup\ (D)}$		—	17	50	ns
Data Hold Time		$t_{hold\ (D)}$		—	−7	10	
Latch Set Up Time	LH	$t_{\overline{LAT}\ setup}$		—	70	200	ns
	HL			—	70	200	
Latch Hold Time	LH	$t_{\overline{LAT}\ hold}$		—	−70	50	ns
	HL			—	−70	50	
Maximum Clock Rise Time		t_r		—	—	10	µs
Maximum Clock Fall Time		t_f		—	—	10	
Maximum Output Rise Time		t_{or}		—	35	80	ns
Maximum Output Fall Time		t_{of}		—	40	80	

Note 1: Cascade operation

DC CHARACTERISTIC TEST CIRCUIT
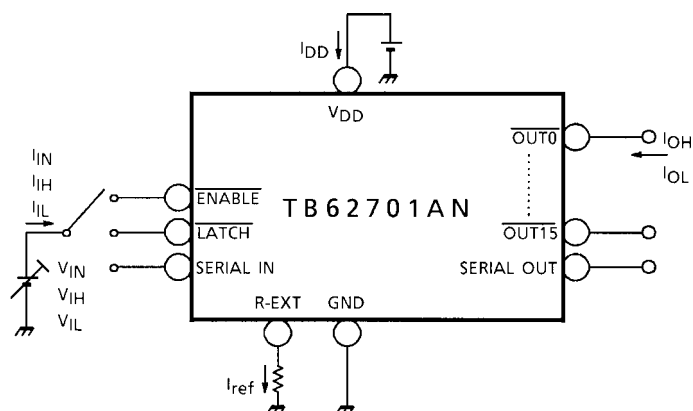
AC CHARACTERISTIC TEST CIRCUIT

TIMING WAVE FORM

1. CLOCK–SERIAL OUT, OUTn

2. CLOCK–$\overline{\text{LATCH}}$

3. $\overline{\text{ENABLE}}$

Ta – I_OUT

I_OUT – Duty Cycle

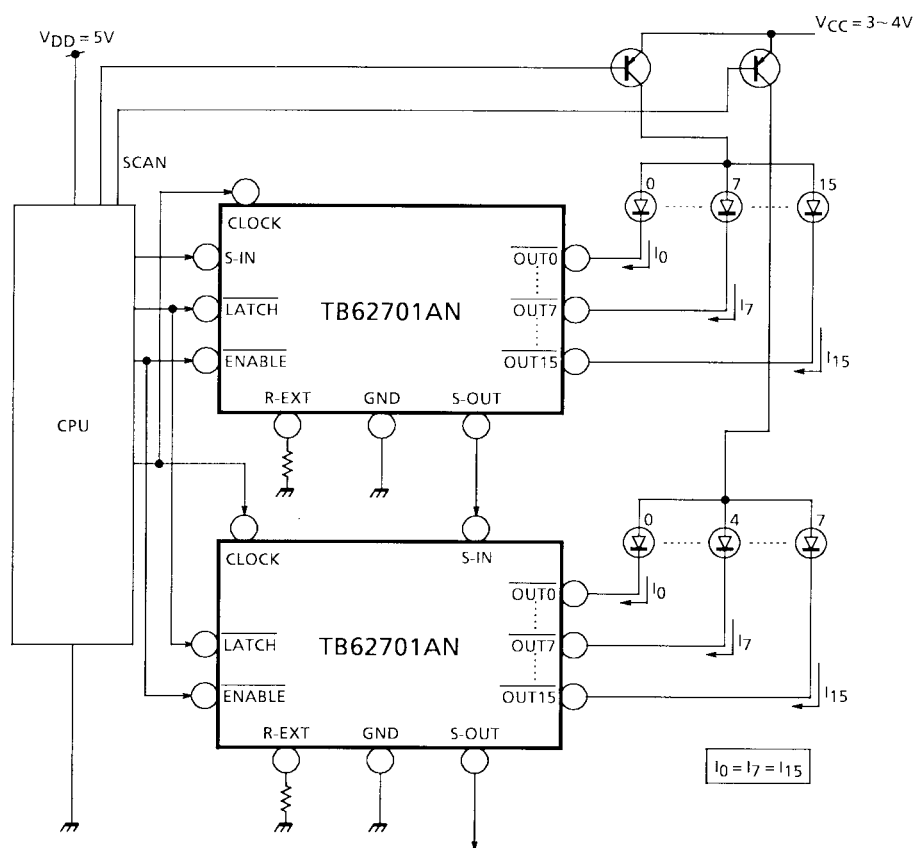
I_OUT – Duty Cycle

I_OUT – Duty Cycle

R_EXT – I_OUT
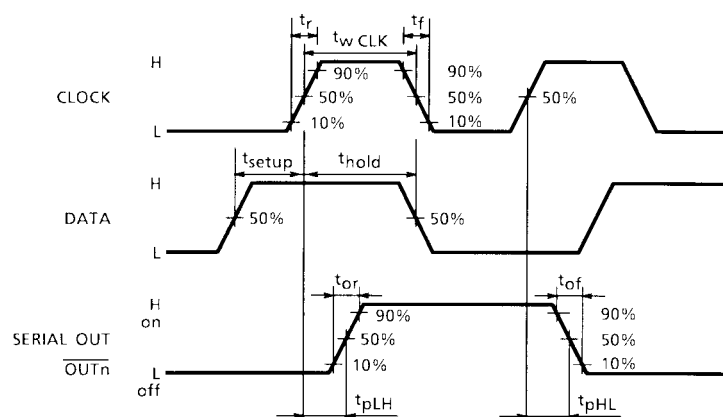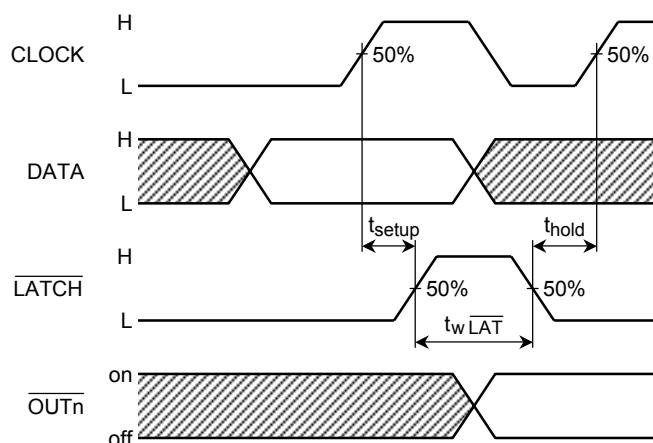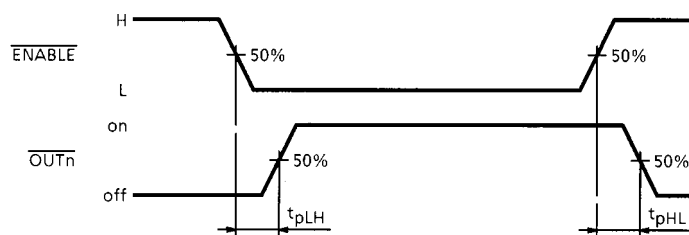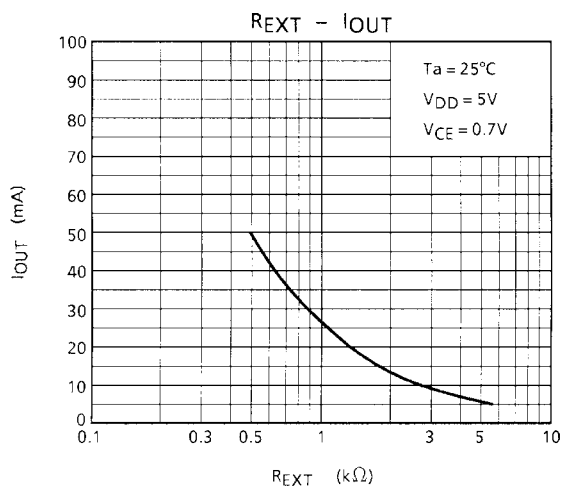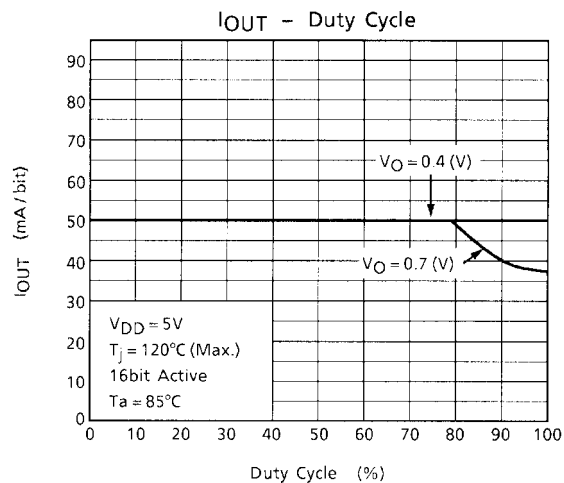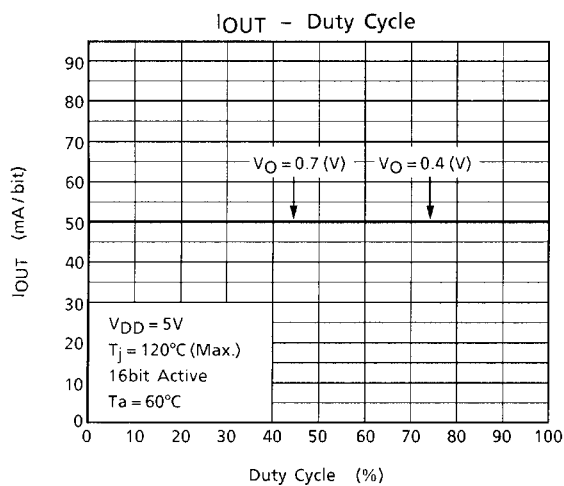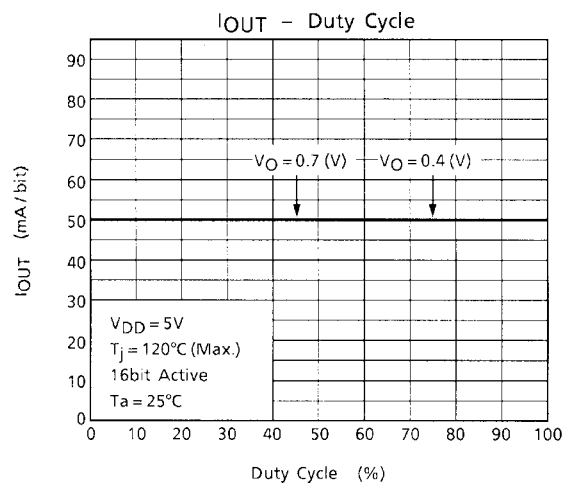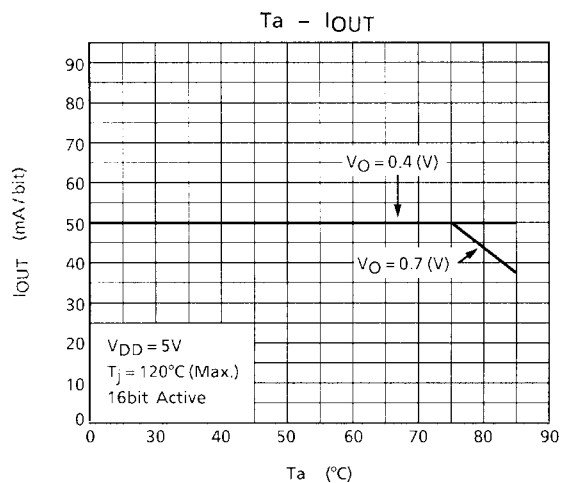
$$I_{OUT} \text{ (mA)} = \{1.26 \text{ (V)}/R_{EXT} \text{ (}\Omega\text{)}\} \times 18.4$$
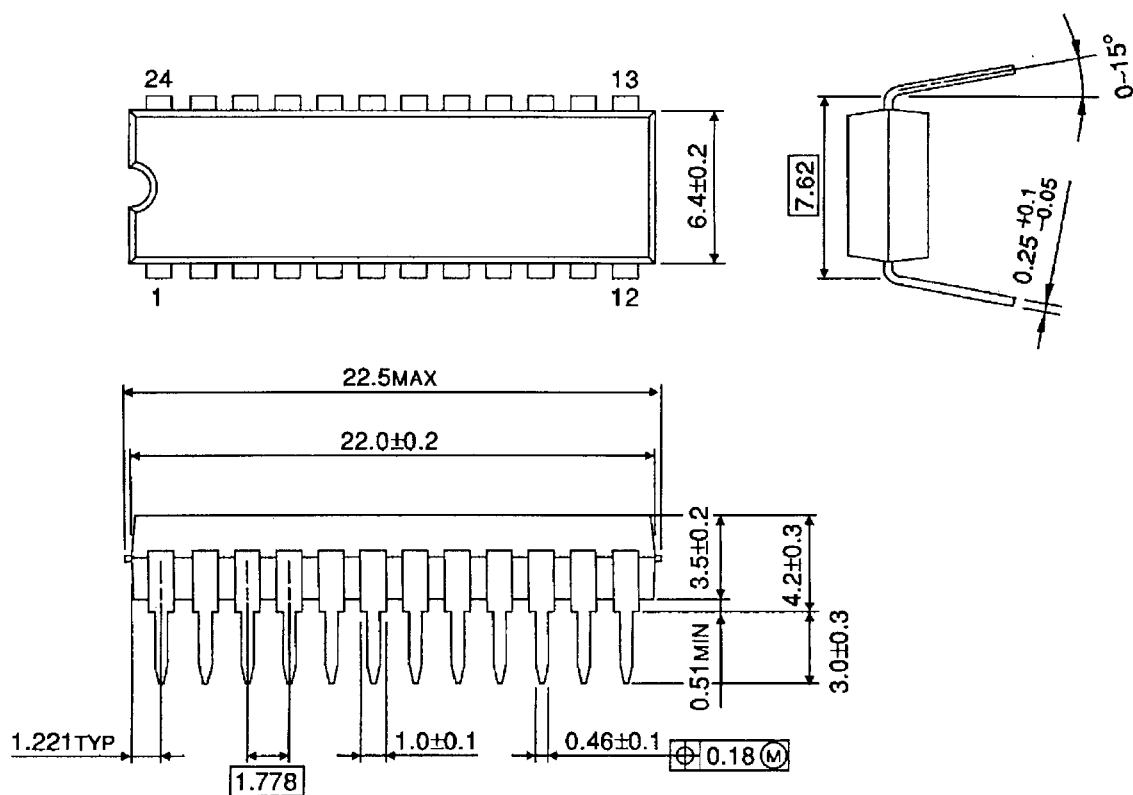
APPLICATION CIRCUIT

PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

SDIP24-P-300-1.78   Unit : mm

Weight: 1.22 g (typ.)

RESTRICTIONS ON PRODUCT USE