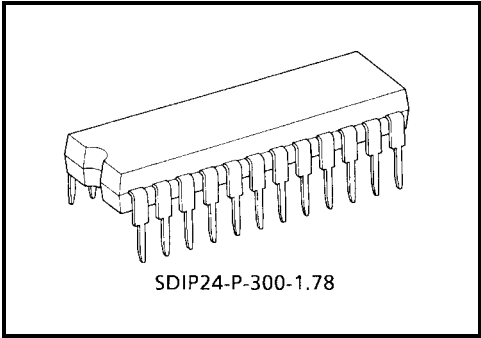


TB62701AN

16BIT SHIFT REGISTER, LATCH & CONSTANT CURRENT DRIVERS

The TB62701AN is specifically designed for LED and LED-DISPLAY constant current drivers.
This constant current output circuit is able to set up external resistor ($I_{OUT} = 5$ to 50mA).
This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of 16bit Shift Register, Latch, AND-GATE and Constant Current Driver.



Weight: 1.22 g (typ.)

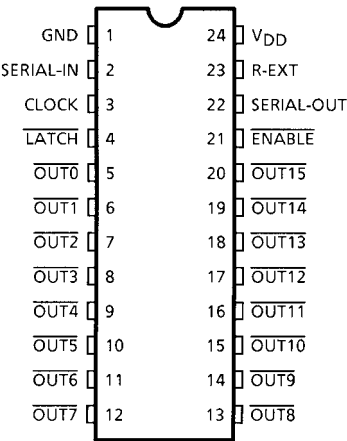
FEATURES

- OUTPUT CURRENT : Set-up at 50mA maximum with an external resistor.
- A LITTLE CHANGE OF OUTPUT CURRENT ($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{ V}$)

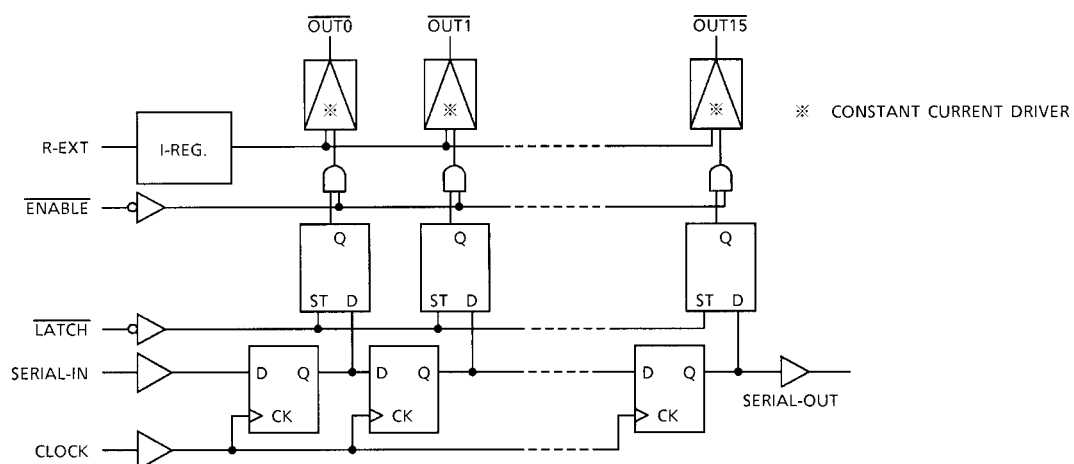
OUTPUT-GND VOLTAGE	A LITTLE CHANGE OF CHANNEL	I_{OUT} [mA]
$\geq 0.4\text{ V}$	$\pm 7\%$	$5 \sim 50\text{ mA}$
$\geq 0.7\text{ V}$		

- 5V CMOS Compatible Input
- PACKAGE : SDIP-24 (SDIP24-P-300)
- MAXIMUM CLOCK FREQUENCY : $f_{MAX} = 2.5\text{ MHz}$ (cascade operation, $T_a = 25^\circ\text{C}$)

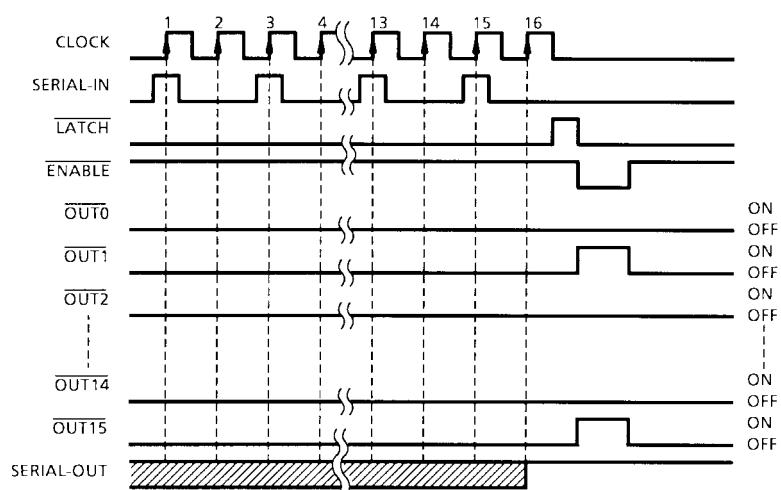
PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



TIMING DIAGRAM



TERMINAL DESCRIPTION

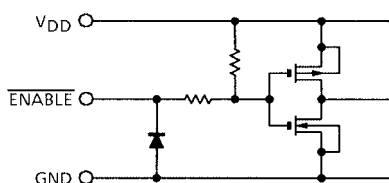
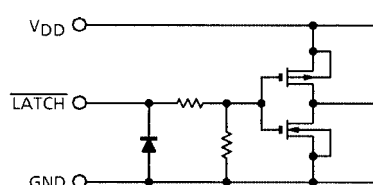
PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic driver
2	SERIAL-IN	Serial data input terminal for shift register
3	CLOCK	Clock input terminal for data shift to up-edge
4	$\overline{\text{LATCH}}$	"H" Level : data through, "L" Level : data hold
24	V_{DD}	Supply voltage terminal
5~12 13~20	$\overline{\text{OUTn}}$	Output terminals
21	$\overline{\text{ENABLE}}$	"H" Level output off, "L" Level : latch data = "H" Level then output on, latch data = "L" Level then output off
22	SERIAL-OUT	Serial data output terminal for shift register
23	R-EXT	The register which connects between R-EXT and GND sets the constant output current.

TRUTH TABLE

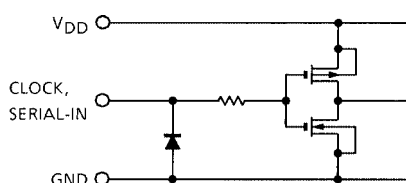
INPUT				OUTPUT $\overline{\text{OUTn}}$ (t = n)	
CLOCK	$\overline{\text{LATCH}}$	ENABLE	SERIAL-IN	$\overline{\text{OUT0}} \dots \overline{\text{OUT7}} \dots \overline{\text{OUT15}}$	SERIAL-OUT
	H	L	D_n	$D_n \quad D_{n-7} \quad D_{n-15}$	D_{n-15}
	L	L	D_n	No change	D_{n-15}
	(Note)	H	D_n	OFF OFF OFF	D_{n-15}
	(Note)	(Note)	D_n	No change	No change

Note: $D_n \sim D_{n-15}$ = "H" then OUTn is ON, "L" then OUTn is OFF.

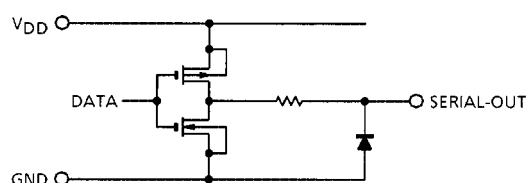
EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. $\overline{\text{ENABLE}}$ terminal2. $\overline{\text{LATCH}}$ terminal

3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	0~7.0	V
Output Voltage	V _{CE}	-0.5~30	V
Output Current	I _{OUT}	50	mA
Input Voltage	V _{IN}	-0.4~V _{DD} + 0.4	V
GND Terminal Current	I _{GND}	800	mA
Clock Frequency	f _{CK}	2.5	MHz
Power Dissipation (Note)	P _D	1.78	W
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

Note: Ambient temperature delated above 25°C in the proportion of 14.2 mW / °C.

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V _{DD}	—	4.5	5.0	5.5	V
Output Voltage		V _{OUT}	—	—	—	30.0	V
Output Current	$\overline{\text{OUTn}}$	I _{OUT}	DC 1 circuit	—	—	45	mA
	S-OUT	I _{OH}	—	—	—	−1.0	
		I _{OL}	—	—	—	1.0	
Input Voltage		V _{IN}	—	0	—	V _{DD}	V
Data Set Up Time		t _{setup} (D)	—	100	—	—	ns
Data Hold Time		t _{hold} (D)	—	20	—	—	ns
Data Set Up Time		t _{setup} (L)	—	300	—	—	ns
Data Hold Time		t _{hold} (L)	—	100	—	—	ns
Clock Pulse Width	t _W CLK	—	100	—	—	—	ns
	t _W $\overline{\text{CLK}}$	—	100				ns
Latch Pulse Width	t _W LAT	—	300	—	—	—	ns
	t _W $\overline{\text{LAT}}$	—	300				ns
Clock Frequency		f _{CK}	Cascade operation	—	—	2.0	MHz
Power Dissipation		P _D	Ta = 85°C	—	—	0.72	W

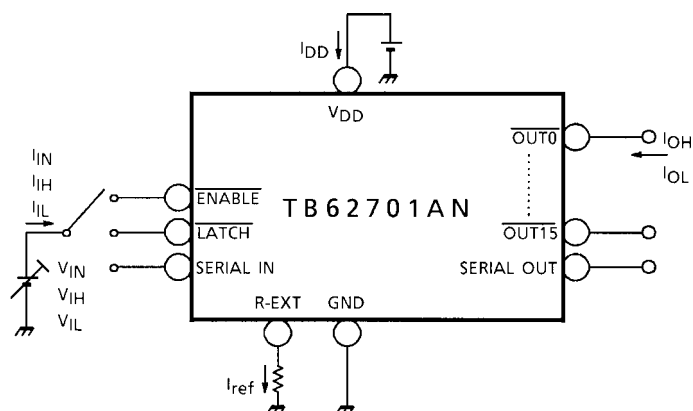
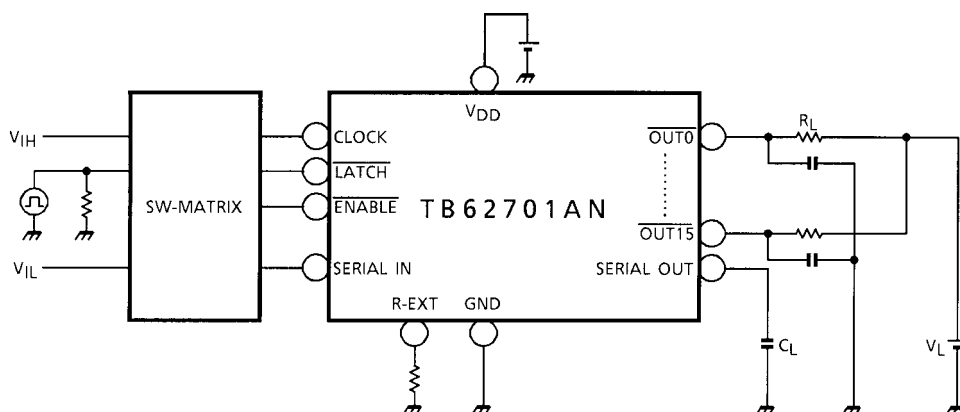
ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0\text{ V}$, $T_a = 25^\circ\text{C}$ unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Input Leakage Current	“H” level	V _{IH}	—	—	70% V _{DD}	—	V _{DD}	V	
	“L” level	V _{IL}	—	—	GND	—	30%V _{DD}		
Output Leakage Current		I _{OH}	—	V _{OH} = 30V	—	—	10	μA	
Output Vottlage	S-OUT	V _{OL}	—	I _{OL} = +1.0 mA	—	—	0.4	V	
		V _{OH}	—	I _{OH} = -1.0 mA	4.6	—	—		
Output Current 1		I _{OL1}	—	V _{CE} = 0.7 V	R _{EXT} = 560 Ω (included ΔI _{OL1})	35.2	41.5	47.7	mA
		I _{OL2}	—	V _{CE} = 0.4 V		33.1	39.0	44.9	
	Delta I _{OUT}	ΔI _{OL1}	—	R _{EXT} = 560 Ω I _{OUT} = 40 mA, V _{CE} = 0.4 V		—	±3.0	±7.0	%
Supply Voltage Regulation		% / V _{DD}	—	R _{EXT} = 560 Ω		—	18	—	% / V
Reference Voltage		V _{ref}	—	R _{EXT} = 560 Ω, Ta = -40~85℃		—	1.26	—	V
Pull Up / Down Resister		R _{IN}	—	—		100	200	400	kΩ
Supply Current	“OFF”	I _{DD} (off) 1	—	R _{EXT} = OPEN, OUTn = Off		—	0.4	0.6	mA
		I _{DD} (off) 2	—	R _{EXT} = 560 Ω, OUTn = Off		—	6.5	10.0	
	“ON”	I _{DD} (on)	—	R _{EXT} = 560 Ω, All output on		—	13.5	20.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

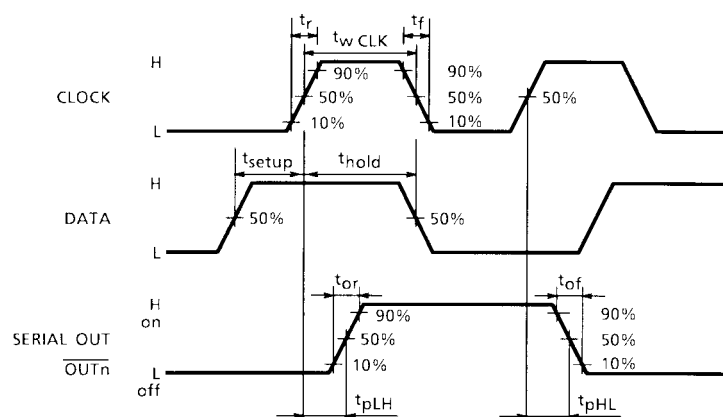
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK-S-OUT	t _{pLH}	V _{DD} = 5.0 V V _{CE} = 1.0 V V _{IH} = V _{DD} V _{IL} = GNK f _{CK} = 2 MHz R _{EXT} = 560 Ω I _{OUT} = 30 mA	—	95	500	ns
	CLK-OUT _n			—	130	500	
	LATCH - OUT _n			—	130	500	
	EN - OUT _n			—	130	500	
Propagation Delay Time ("H" to "L")	CLK-S-OUT	t _{pHL}		—	95	720	ns
	CLK-OUT _n			—	130	500	
	LATCH - OUT _n			—	130	500	
	EN - OUT _n			—	130	500	
Maximum Clock Frequency		f _{MAX} (Note 1)		2.0	—	2.5	MHz
Minimum Pulse Width	CLK	t _{W CLK}		—	45	80	ns
	LATCH	t _{W LATCH}		—	10	50	
Data Set Up Time		t _{setup} (D)		—	17	50	ns
Data Hold Time		t _{hold} (D)		—	−7	10	
Latch Set Up Time	LH	t _{LATCH setup}		—	70	200	ns
	HL			—	70	200	
Latch Hold Time	LH	t _{LATCH hold}		—	−70	50	ns
	HL		—	−70	50		
Maximum Clock Rise Time		t _r	—	—	10	μs	
Maximum Clock Fall Time		t _f	—	—	10		
Maximum Output Rise Time		t _{or}	—	35	80	ns	
Maximum Output Fall Time		t _{of}	—	40	80		

Note 1: Cascade operation

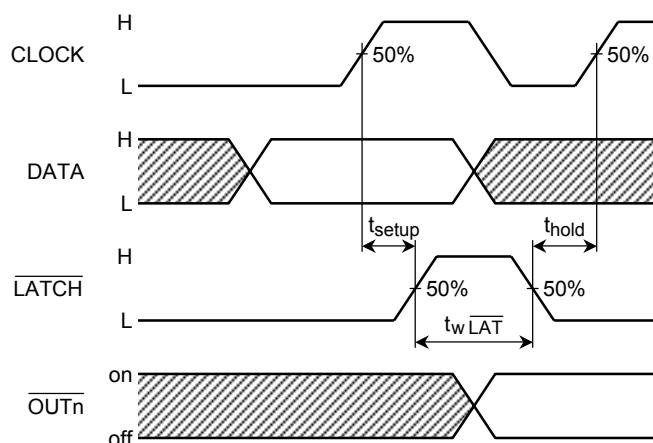
DC CHARACTERISTIC TEST CIRCUIT

AC CHARACTERISTIC TEST CIRCUIT


TIMING WAVE FORM

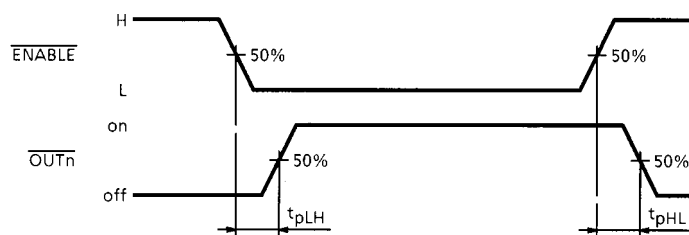
1. CLOCK-SERIAL OUT, OUTn

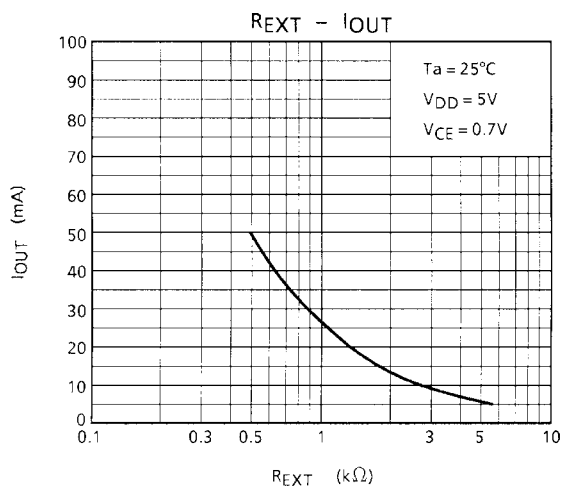
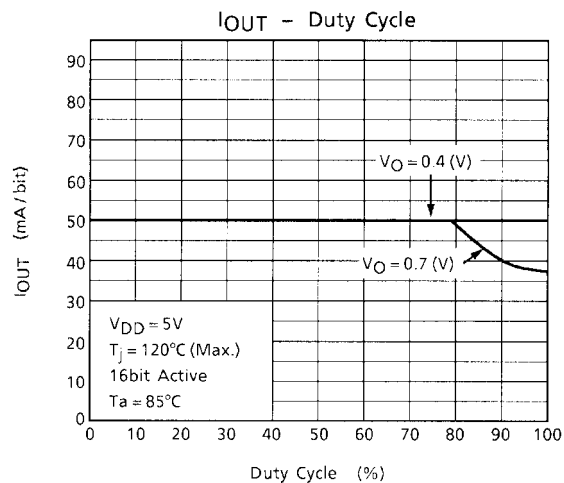
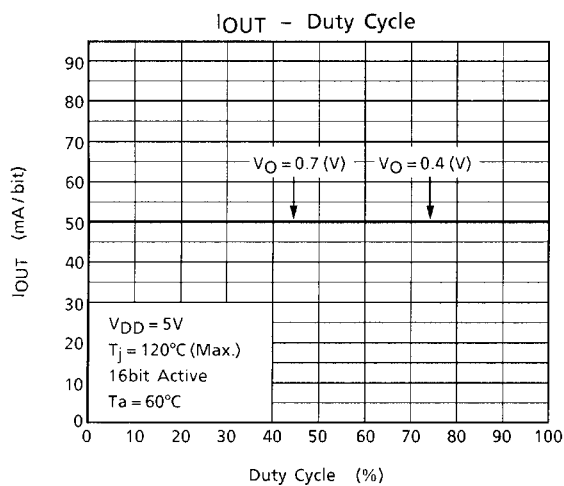
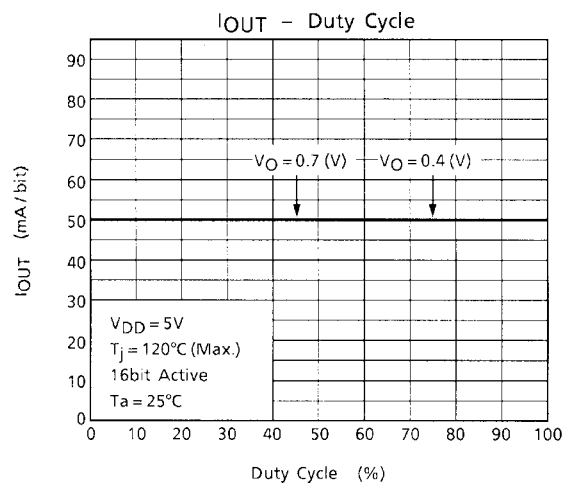
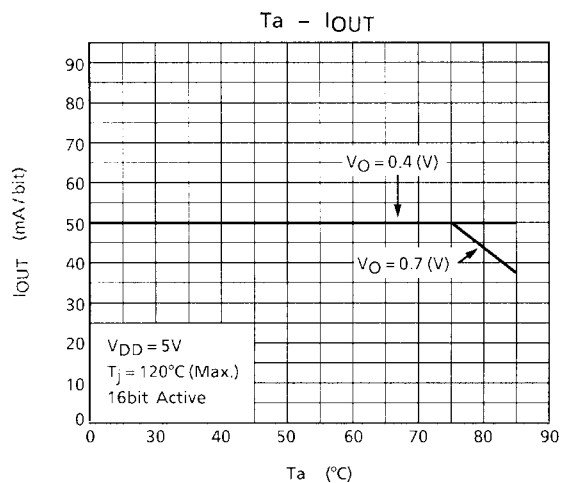


2. CLOCK-LATCH



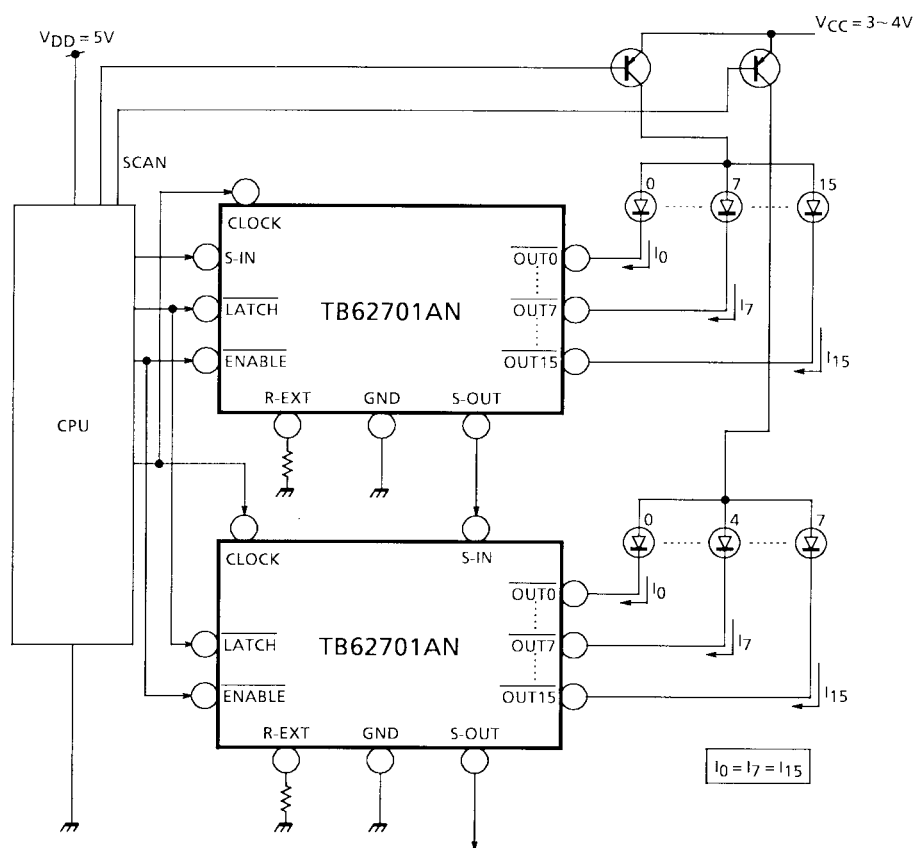
3. ENABLE





$$I_{OUT} \text{ (mA)} = \{1.26 \text{ (V)} / R_{EXT} \text{ (}\Omega\text{)}\} \times 18.4$$

APPLICATION CIRCUIT



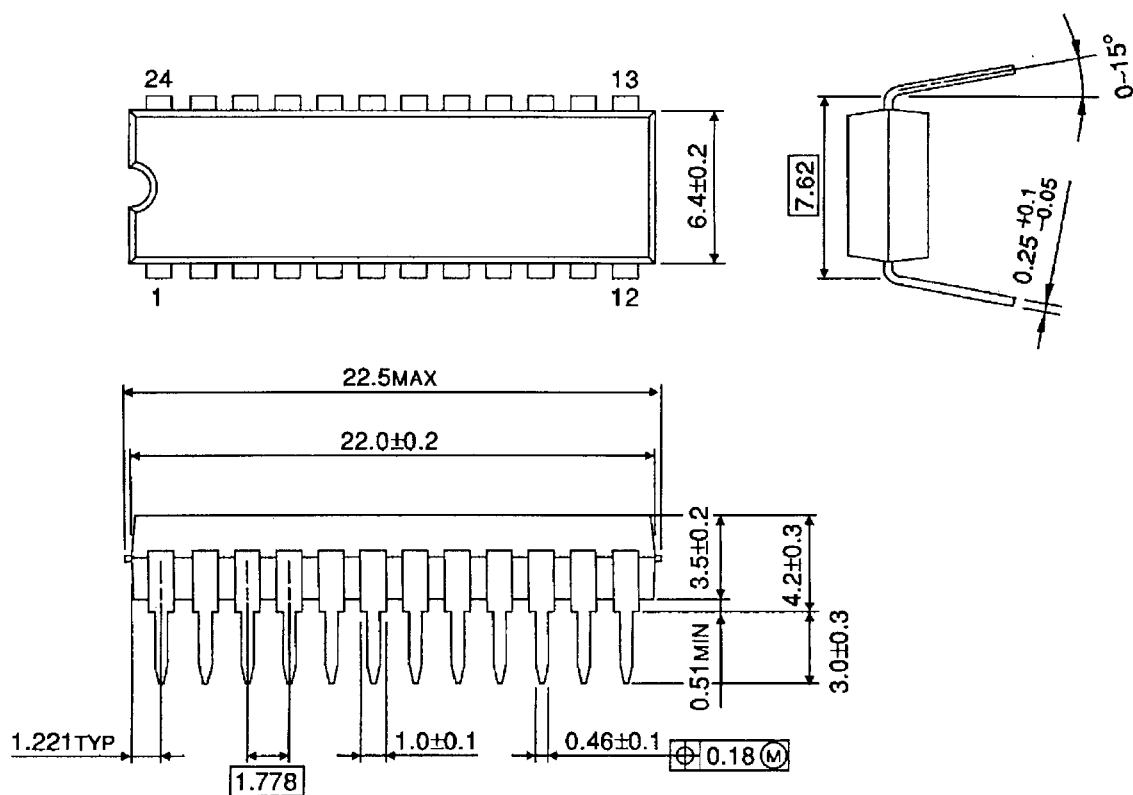
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, VCC (VDD) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

SDIP24-P-300-1.78

Unit : mm



Weight: 1.22 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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