SN75DP119 DisplayPort 1:1 Signal Repeater and Signal Conditioner

1 Features

- DP signal repeater
- Supports Data Rates up to 2.7Gbps
- Fixed Equalizer With 3 Selectable Settings
- 12kV ESD HBM
- Temperature Range: –40 to 85°C
- 14 Pin 3.50 x 3.50mm RGY Package or 36-Pin 6.00 x 6.00mm RHH Package

2 Applications

- eDP
- Desktop PC
- Notebook PC
- PC Docking Station
- PC Standalone Video Card

3 Description

The SN75DP119 is a 1-lane or 2-lane embedded DisplayPort (eDP) repeater that regenerates the DP high speed digital link. The device compensates for pcb related frequency loss and signal reflections. This is especially helpful in designs with long pcb traces or when there is a FET switch in the signal path.

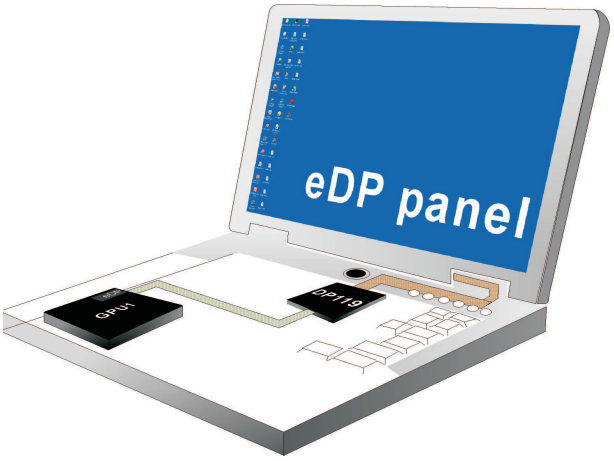
Four levels of differential output voltage swing (V_{OD}) and any combination of pre-emphasis using these V_{OD} levels are supported. The output swing and pre-emphasis are configured through device control inputs. The available output swing levels are $300mV_{PP}$, $400mV_{PP}$, $600mV_{PP}$ or $750mV_{PP}$. Therefore, the output pre-emphasis level can be configured to 0dB, 2.0dB, 2,5dB, 3.5dB, 5.5dB, 6dB, or 8dB. This is a good solution for embedded link applications, such as the connection from the GPU to the notebook internal panel. To adjust the output signal level adaptively during link training, the implementation needs to control the device control inputs.

The SN75DP119 supports programmable integrated receiver equalization circuitry. This equalization circuitry can be used to help improve signal integrity in applications where the input link has a high level of insertion loss. The equalizer can be set to 3dB or 6dB equalization. The equalizer can also be turned off.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75DP119	VQFN (14)	3.50mm x 3.50mm
	VQFN (36)	6.00mm x 6.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

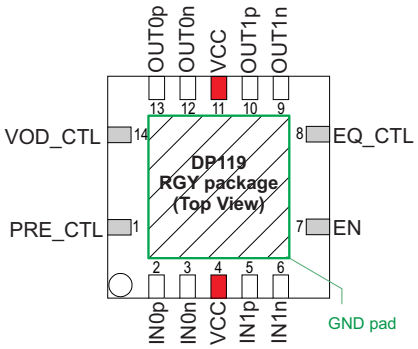
Changes from Original (November 2009) to Revision A	Page
• Changed the data sheet to the new TI standard format	1
• Changed Feature From: Temperature Range: 0..85°C To: Temperature Range: –40 to 85°C	1
• Changed the Description text From: "extended operational temperature range from 0°C to 85°C." To: "extended operational temperature range from –40°C to 85°C."	2
• Added the Handling Ratings table	5
• Changed the Operating free-air temperature MIN value in the ROC table From: 0 To –40	5
• Added the Thermal Information table	6

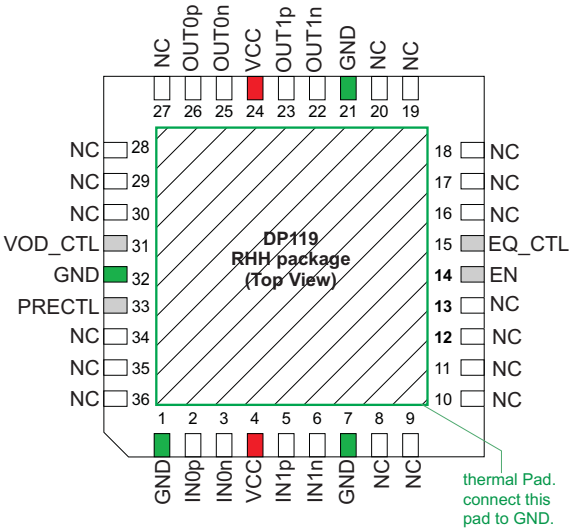
5 Description (continued)

The device is characterized for an extended operational temperature range from –40°C to 85°C.

The SN75DP119 consumes between 64mW and 175mW depending on the selected mode of operation. The device also supports an ultra low power standby mode. In this mode, the outputs are disabled and the device draws less then 700µW of power.

6 Pin Configuration and Functions





Pin Functions, RGY Package

PIN			DESCRIPTION
NAME	NUMBER	I/O	
MAIN LINK INPUT PINS			
IN0p	2	I [100Ω diff]	DisplayPort Main Link Channel 0 Differential Input
IN0n	3		
IN1p	5		DisplayPort Main Link Channel 1 Differential Input
IN1n	6		
MAIN LINK OUTPUT PINS			
OUT0p	13	O [100Ω diff]	DisplayPort Main Link Channel 0 Differential Output
OUT0n	12		
OUT1p	10		DisplayPort Main Link Channel 1 Differential Output
OUT1n	9		
CONTROL PINS			
EN	7	3-level Input [CMOS]	Enable. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the device for 1-channel mode, 2-channel mode or power down mode. EN = HIGH: Device in Normal Mode, both outputs OUT1 and OUT2 are enabled; EN = VCC/2 (input left floating): Device in Normal mode, 2nd output is disabled; EN = LOW: Device in Power Down mode. All outputs are high-impedance; Inputs are ignored
PRE_CTL	1	3-level Input [CMOS]	Configures the output pre-emphasis level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. See Table 1 for configuration details.
VOD_CTL	14	3-level Input [CMOS]	Configures the output amplitude VOD level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure 3 different output swing amplitudes. See Table 1 for configuration details.
EQ_CTL	8	3-level Input [CMOS]	Configures the EQ input setting for both differential inputs. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. EQ_CTL = LOW: 0dB (EQ turned off) EQ_CTL = VCC/2 (input left floating): 3dB fixed EQ EQ_CTL = HIGH (input tied to VCC): 6dB fixed EQ
SUPPLY AND GROUND PINS			
VCC	4, 11	pwr	3.3V Supply
GND	thermal pad	pwr	Ground
Note: (H) Logic High: (L) Logic Low			

Pin Functions, RHH Package

PIN			DESCRIPTION
NAME	NUMBER	I/O	
MAIN LINK INPUT PINS			
IN0p	2	I [100Ω diff]	DisplayPort Main Link Channel 0 Differential Input
IN0n	3		
IN1p	5		DisplayPort Main Link Channel 1 Differential Input
IN1n	6		
MAIN LINK OUTPUT PINS			
OUT0p	26	O [100Ω diff]	DisplayPort Main Link Channel 0 Differential Output
OUT0n	25		
OUT1p	23		DisplayPort Main Link Channel 1 Differential Output
OUT1n	22		
CONTROL PINS			
EN	14	3-level Input [CMOS]	Enable. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the device for 1-channel mode, 2-channel mode or power down mode. EN = HIGH: Device in Normal Mode, both outputs OUT1 and OUT2 are enabled; EN = VCC/2 (input left floating): Device in Normal mode, 2nd output is disabled; EN = LOW: Device in Power Down mode. All outputs are high-impedance; Inputs are ignored
PRECTL	33	3-level Input [CMOS]	Configures the output pre-emphasis level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. See Table 1 for configuration details.
VOD_CTL	31	3-level Input [CMOS]	Configures the output amplitude VOD level. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure 3 different output swing amplitudes. See Table 1 for configuration details.
EQ_CTL	15	3-level Input [CMOS]	Configures the EQ input setting for both differential inputs. This input is a 3-level input. If the input is left open, the internal input biasing pulls the input level to VCC/2. The input can also be pulled high or low externally. This allows to configure the pre-emphasis for 3 different levels. EQ_CTL = LOW: 0dB (EQ turned off) EQ_CTL = VCC/2 (input left floating): 3dB fixed EQ EQ_CTL = HIGH (input tied to VCC): 6dB fixed EQ
SUPPLY AND GROUND PINS			
VCC	4, 24	pwr	3.3V Supply
GND	1, 7, 21, 32 thermal pad	pwr	Ground
NC	8-13,16-20, 27-30, 34-36		Not Connected
Note: (H) Logic High: (L) Logic Low			

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range(2)	V_{CC}	–0.3	4	V
Voltage Range	Main Link I/O (OUTx, INx) Differential Voltage	–0.3	VCC + 0.3	V
	Control Inputs	–0.3	5.5	V
Continuous power dissipation		See the Thermal Information Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–12	12	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	-40		85	°C
3-LEVEL CONTROL PINS (EN, VOD_CTL, PRE_CTL, EQ_CTL)					
V_{IH}	High-level input voltage	V_{CC}–0.5			V
V_{IM}	Mid-level input voltage	V_{CC}/2–0.3		V_{CC}/2+0.3	V
V_{IL}	Low-level input voltage			0.5	V
MAIN LINK DIFFERENTIAL INPUT AND OUTPUT PINS IN[4:1] AND OUT[4:1]					
V_{ID}	Peak-to-peak input differential voltage – HBR (high bit rate)	0.15		1.4	V_{PP}
V_{ID}	Peak-to-peak input differential voltage – LBR (low bit rate)	0.15		1.4	V_{PP}
d_R	Data rate			2.7	Gbps
C_{AC}	AC coupling capacitance (each input and each output line)	1×75		2×200	nF
R_{tdiff}	Differential output termination resistance	80	100	120	Ω
V_{Oterm}	Output termination voltage (AC coupled)	0		2	V
$t_{SK(inHBR)}$	Intra-pair skew at the input package pins using 2.7 Gbps input data rate			100	ps
$t_{SK(inLBR)}$	Intra-pair skew at the input package pins using 1.62 Gbps input data rate			300	ps
$t_{R/F}$	Input rise and fall time			160	ps

7.4 Thermal Information

THERMAL METRIC[1]		RGY	RHH	UNIT
		14 PINS	36 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	34	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20	20	
$R_{\theta JB}$	Junction-to-board thermal resistance	16	17	
ψ_{JT}	Junction-to-top characterization parameter	n/a	n/a	
ψ_{JB}	Junction-to-board characterization parameter	n/a	n/a	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12	12	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCDP1max}$	Supply current 1 DP lane selected	WorstCase: EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; V_{ID} = 400 mV_{PP}; V_{OD} = 300 mVpp, 8.5 dB pre-emp (PRE_CTL=V_{CC}; V_OD_CTL=GND); EQ_CTL = V_{CC} (6 dB); V_{CC} = 3.3 V (for typ) and V_{CC} = 3.6 V (for max), [1]		16.2	21.3	mA
$I_{CCDP2max}$	Supply current 2 DP lanes selected			31.7	41.4	mA
$I_{CCDP3max}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or VCC (2-lane selected); 2.7Gbps PRBS; V_{ID} = 400 mV_{PP}; V_{OD} = 300 mV_{PP}, 0 dB pre-emp (PRE_CTL = GND); VOD_CTL = VCC/2); EQ_CTL=GND (0 dB); V_{CC} = 3.3 V (for typ) and V_{CC} = 3.6 V (for max),		12.9	17.6	mA
$I_{CCDP4max}$	Supply current 2 DP lanes selected			24.9	34.1	mA
$I_{CCDP1typ}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; IN/OUT; V_{ID} = 600 mV_{PP}; (PRE_CTL=GND); VOD_CTL = V_{CC}); V_{CC} = 3.3 V, EQ_CTL = GND (no EQ) [2]		14.5		mA
$I_{CCDP2typ}$	Supply current 2 DP lanes selected			28.2		mA
$I_{CCDP3typ}$	Supply current 1 DP lane selected	EN = V_{CC}/2 (1-lane) or V_{CC} (2-lane selected); 2.7Gbps PRBS; no pre-emp; IN/OUT; V_{ID} = 800 mV_{PP}; (PRE_CTL= VOD_CTL = V_{CC}); V_{CC} = 3.3 V, EQ_CT L = GND (no EQ) [3]		14.5		mA
$I_{CCDP4typ}$	Supply current 2 DP lanes selected			28.2		mA
IPWRDN	Shutdown current (PWRDN mode)	EN = GND;		25	100	µA
3-LEVEL CONTROL PINS (EN, VOD_CTL, PRE_CTL, EQ_CTL)						
I_L	Low-level input current	V_I = 0.5 V; V_{CC} = 3.6 V	–30		30	µA
I_H	High-level input current	V_I = V_{CC} – 0.5 V; Vcc = 3.6V	–30		30	µA
I_M	Mid-level input current	V_I = V_{CC} /2 – 0.3V and V_I = V_{CC} /2 + 0.3 V; V_{CC} = 3.6 V	–30		30	µA
R_{bias}	Input bias resistance	See Figure 6	105	125	145	kΩ
R_{ESD}	input series resistance to biasing network	See Figure 6		2	2.4	kΩ

(1) This current consumption also applies to VOD = 400mV with 5.5 dB pre-emphasis or VOD = 600mV output swing and 2dB pre-emphasis
(2) This current consumption also applies to VOD = 300mV with 2 dB pre-emphasis
(3) This current consumption also applies to VOD = 300mV with 6dB pre-emphasis or VOD = 400mV output swing and 3.5dB pre-emphasis

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN[1:0], OUT[1:0] (4)						
[$V_{OD(0.3)}$]	Output differential voltage swing	V_{PRE} = $V_{PRE(0.0)}$; 675 Mbps D10.2 test pattern; V_{ID} = 300 mVpp; EQ = 3 dB	300mV setting only used with pre-emphasis			
				[300]		mV_{pp}
$V_{OD(0.4)}$				400		mV_{pp}
$V_{OD(0.6)}$				600		mV_{pp}
$V_{OD(0.75)}$				800		mV_{pp}
$V_{Eyemask}$	Eyemask compliance	V_{OD} = 800 mVpp test pattern measured in compliance with PHY CTS1.1 section 3.1 at test point TP2; V_{ID}= 300mV_{PP} ; EQ=3dB	pass			
$V_{PRE(0.0)}$	Driver output pre-emphasis	V_{OD} = $V_{OD(0.4)}$, $V_{OD(0.6)}$, or $V_{OD(0.8)}$ at 2.7Gbps only		0		dB
$V_{PRE(2.5)}$		V_{OD} = $V_{OD(0.3)}$ or $V_{OD(0.6)}$ at 2.7Gbps only		2.7		dB
$V_{PRE(3.5)}$		V_{OD} = $V_{OD(0.4)}$ at 2.7Gbps only; EQ=3dB	0.9	3.5		dB
$V_{PRE(6.0)}$		V_{OD} = $V_{OD(0.3)}$ or $V_{OD(0.4)}$ at 2.7Gbps only; EQ=3dB	3.3	6.0		dB
$V_{PRE(8.5)}$		V_{OD} = $V_{OD(0.3)}$ at 2.7Gbps only; EQ=3dB	7	8.5		dB
R_{OUT}	Driver output impedance (single ended)			100		Ω
R_{IN}	Differential input termination impedance		80	100	120	Ω
V_{Item}	Input termination voltage (AC coupled)	Self-biased	0	1.7	2	V
V_{OCM}	Output common mode voltage		0	1.55	2	V
V_{TXACCM}	Output AC common mode voltage	Verified through statistical measurements only using 1.62Gbps and 2.7Gbps PRBS7 data pattern measured at TP2; EQ = 3dB			20	mVrms
$I_{TXSHORT}$	Output short circuit current limit	OUT[1:0] shorted to GND; single-ended current			50	mA
$I_{RXSHORT}$	Input short circuit current limit	IN[1:0] shorted to GND (single ended)			50	mA

(4) The SN75DP119 is designed to support the DisplayPort high speed differential main link with three levels of output voltage swing and three levels of pre-emphasis. The main link I/Os of the SN75DP119 are designed to be compliant with the DisplayPort 1.1a specification

7.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Differential output edge rate (20%–80%)	All VOD options, Measured at TP1, PRBS7; V_{ID} = 300 mV_{PP}; EQ = 3dB; C_{LOAD} = 1 pF	50		155	ps
t_{PD}	Propagation delay time			325	550	ps
t_{skpp}	Part-to-Part skew	With identical voltage and temperature		0	160	ps
$t_{SK(1)}$	Intra-pair output skew	Signal input skew = 0ps; d_R = 2.7Gbps, No Pre-emphasis, 800 mVp-p , D10.2 pattern			20	ps
$t_{SK(2)}$	Inter-pair output skew				100	ps
$\Delta t_{DPJIT(PP)}$	Peak-to-peak output residual jitter at package pins	$V_{OD(0.4)}$; $V_{PRE(0.0)}$; Δt_{jit} = t_{jit}(output) – t_{jit}(input); verified through design simulation and statistical measurements only using 1.62Gbps and 2.7Gbps PRBS7 data pattern.			15	ps

7.7 Typical Characteristics

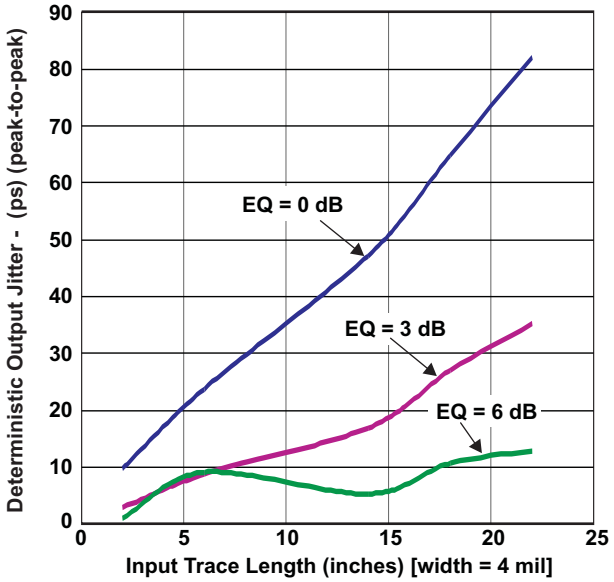


Figure 1. Deterministic Output Jitter vs Input Trace Length

8 Parameter Measurement Information

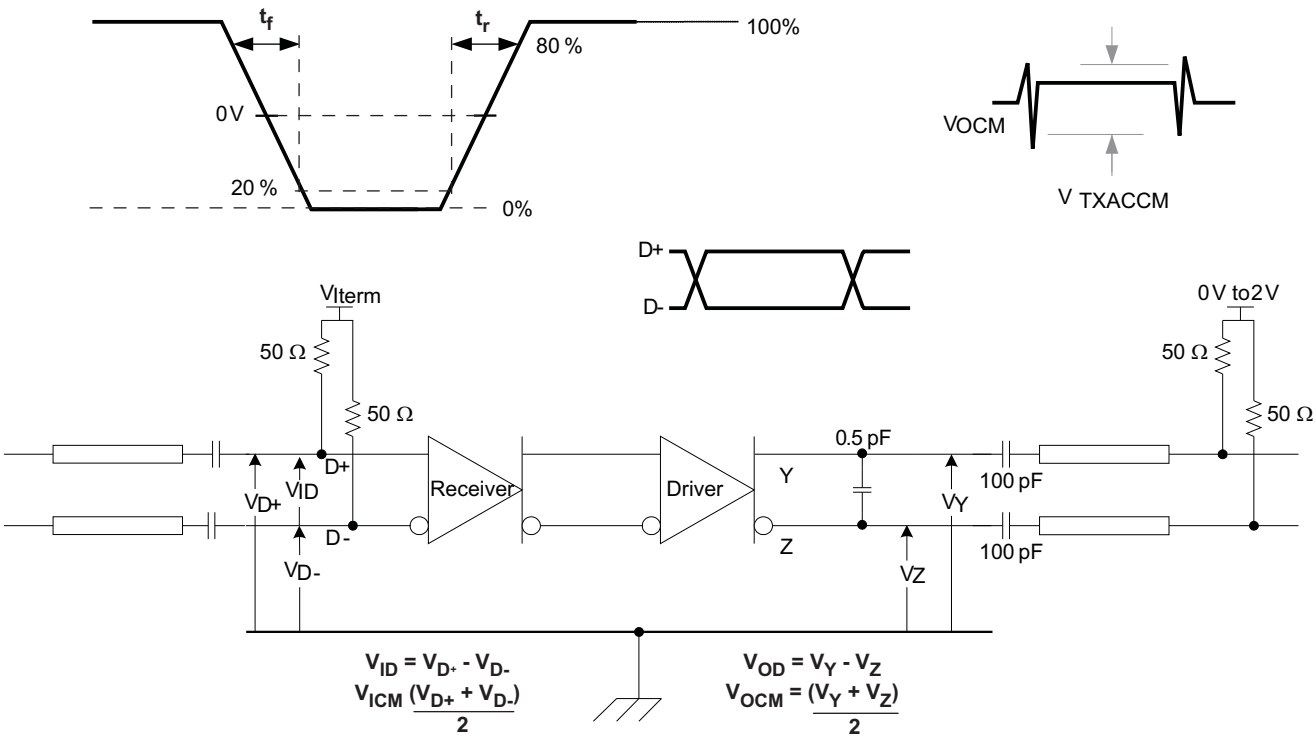


Figure 2. Main Link Test Circuit

Parameter Measurement Information (continued)

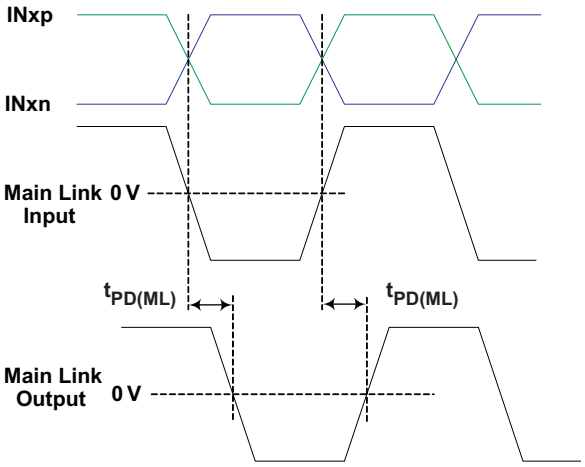


Figure 3. Main Link Delay Measurments

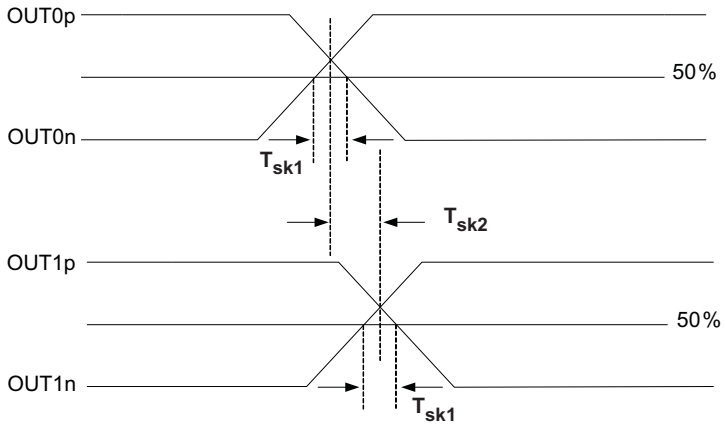


Figure 4. Main Link Skew Measurements

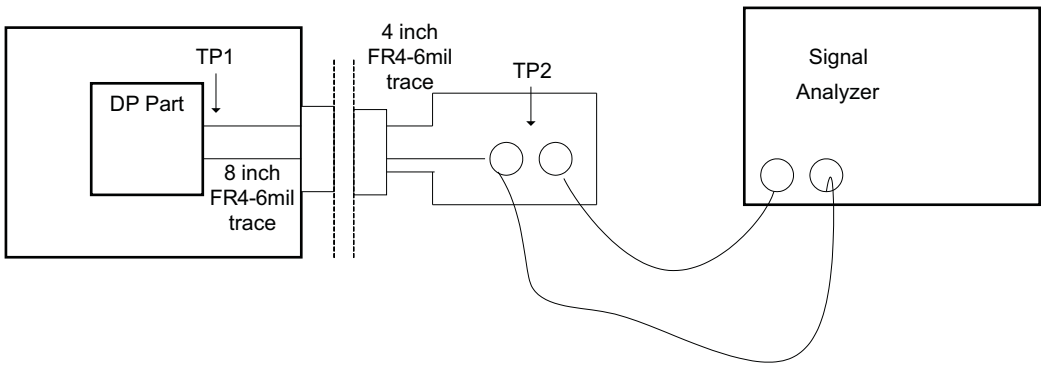


Figure 5. Display Port Compliance Setup

Parameter Measurement Information (continued)

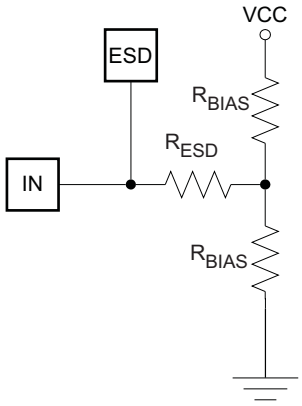


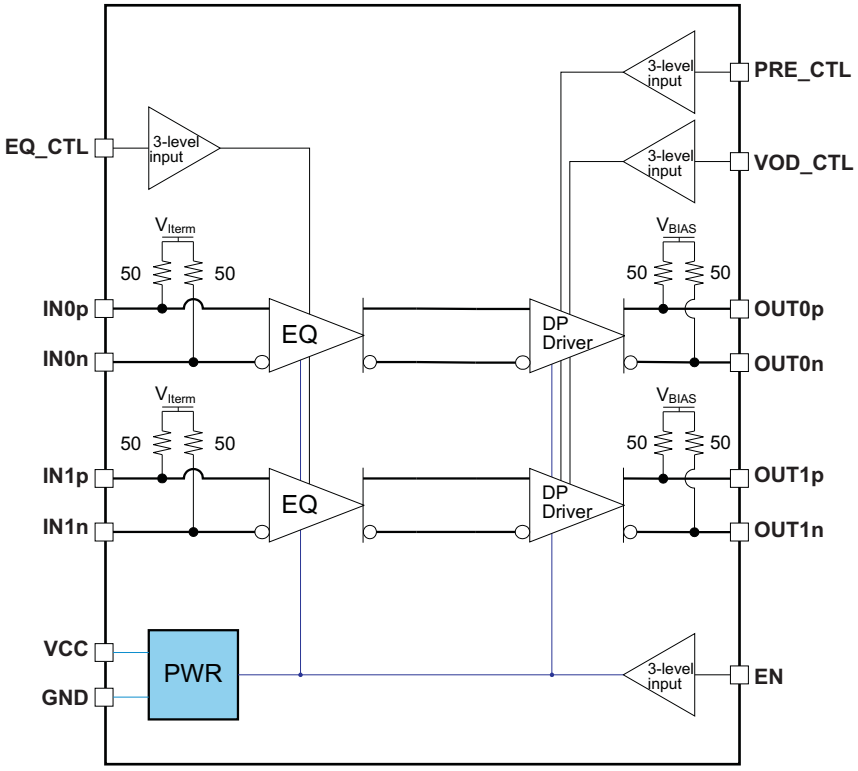
Figure 6. 3-Level Input Biasing Network

9 Detailed Description

9.1 Overview

The SN75DP119 is a 1-lane or 2-lane embedded DisplayPort (eDP) repeater that regenerates the DP high speed digital link. The device compensates for pcb related frequency loss and signal reflections. This is especially helpful in designs with long pcb traces or when there is a FET switch in the signal path.

9.2 Functional Block Diagram



Functional Block Diagram (continued)

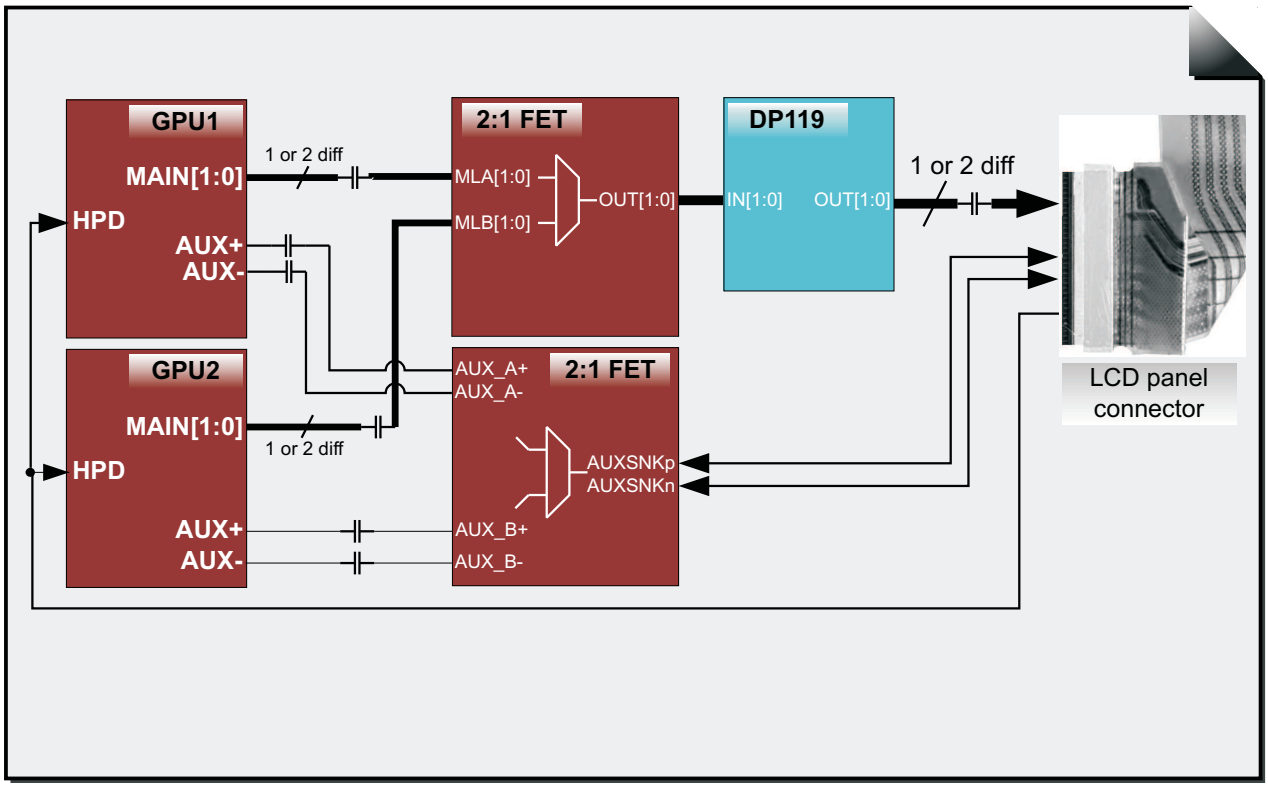


Figure 7. Typical Implementation Showing Two GPU Sources, a 2:1 FET Switch, and the DP119 as Signal Conditioner

9.3 Feature Description

9.3.1 Pre-Emphasis and VOD Output Swing Setings

The SN75DP119 allows configuring output pre-emphasis and output swing through the external control inputs. The following options are valid:

Table 1. Pre-Emphasis and VOD Output Swing Configuration

	PRE_CTL = LOW	PRE_CTL = VCC/2 (INPUT LEFT FLOATING)	PRE_CTL = HIGH
VOD_CTL = LOW	V_{OD} = 300 mV_{PP}; 2.5 dB pre-emphasis (lowest power consumption)	V_{OD} = 300 mV_{PP}; 6 dB pre-emphasis	V_{OD} = 300 mV_{PP}; 8.5 dB pre-emphasis
VOD_CTL = VCC/2 (input left floating)	V_{OD} = 400 mV_{PP}; no pre-emphasis	V_{OD} = 400 mV_{PP}; 3.5 dB pre-emphasis	V_{OD} = 400 mV_{PP}; 5.5 dB pre-emphasis
VOD_CTL = HIGH	V_{OD} = 600 mV_{PP}; no pre-emphasis	V_{OD} = 600 mV_{PP}; 2.5 dB pre-emphasis	V_{OD} = 800 mV_{PP}, no pre-emphasis

9.4 Device Functional Modes

9.4.1 Status Detect and Operating Modes Flow Diagram

The SN75DP119 switches between the power saving and the active modes in the following way:

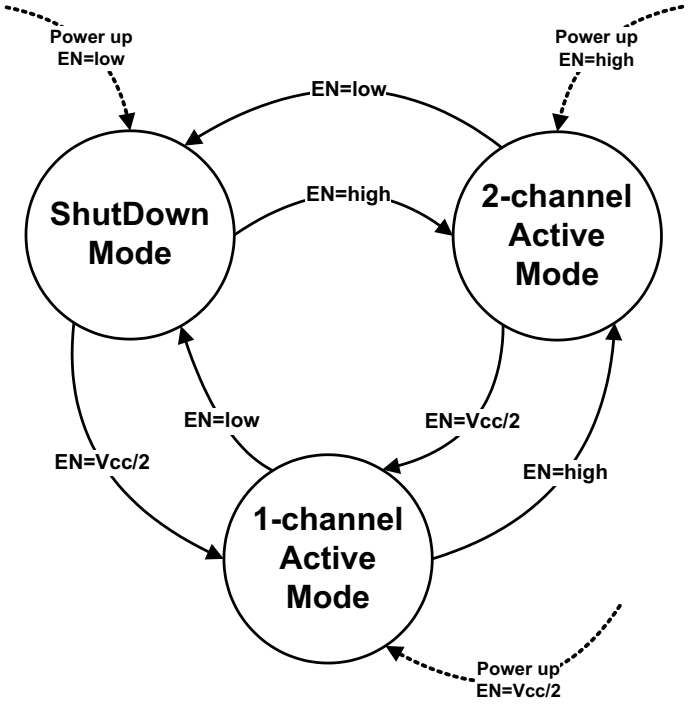


Figure 8. SN75DP119 Operational Modes Flow Chart

Table 2. Description of SN75DP119 Modes

MODE	CHARACTERISTICS	CONDITIONS
ShutDown Mode	Least amount of power consumption (all circuitry turned off); outputs are high-impedance	EN is low
2- channel Active Mode	Data transfer (normal operation); The device outputs OUTx represents the data received on the input INx. The input EQ and output pre-emphasis and output swing voltage level are controlled through the external control pins.	EN is high (both main link outputs enabled)
1-channel Active Mode	Data transfer (normal operation); The device output OUT0 represents the data received on the input IN0. The 2nd channel (IN1 and OUT1) are disabled. The input EQ and output pre-emphasis and output swing voltage level are controlled through the external control pins.	EN is VCC/2 (only main link channel 0 enabled)

10 Application and Implementation

10.1 Application Information

Figure 9 provides a simple schematic reference for the 14-pin package. In addition to this schematic sufficient VCC decoupling for the 3.3V power supply is necessary.

10.2 Typical Application

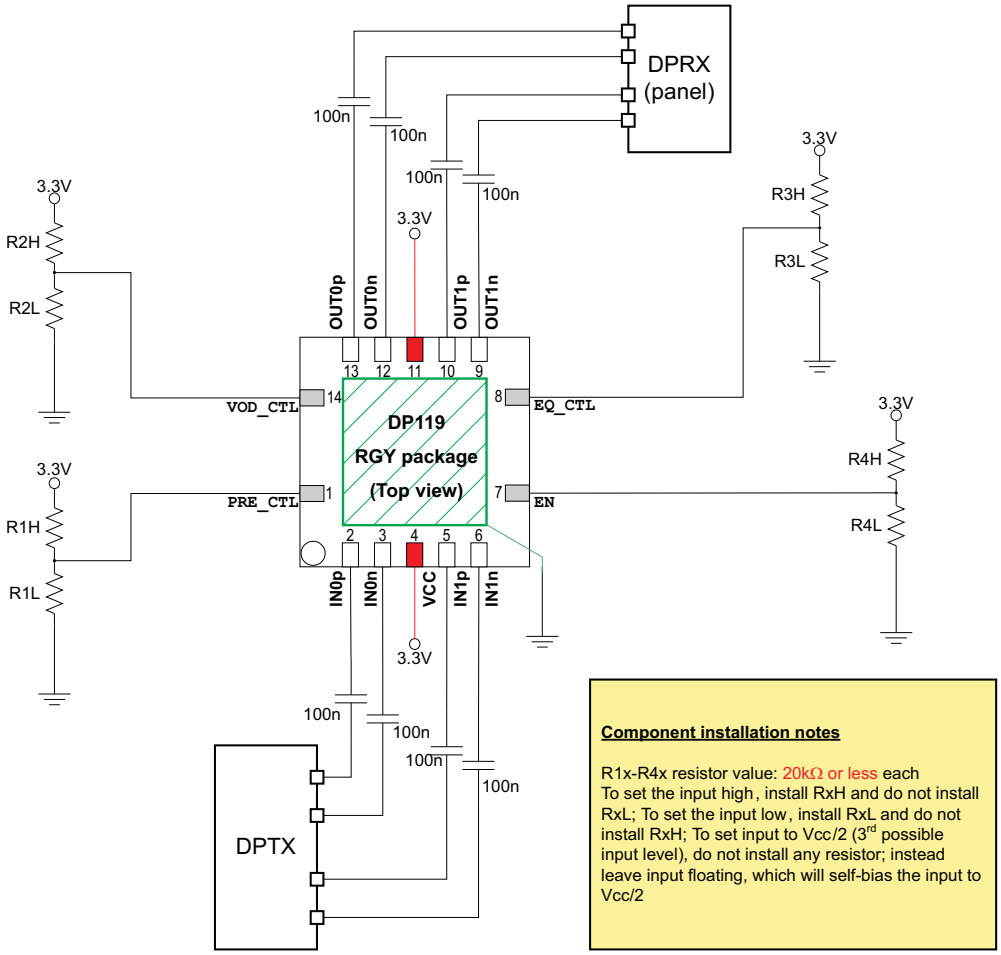


Figure 9. Simplified Schematic drawing

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

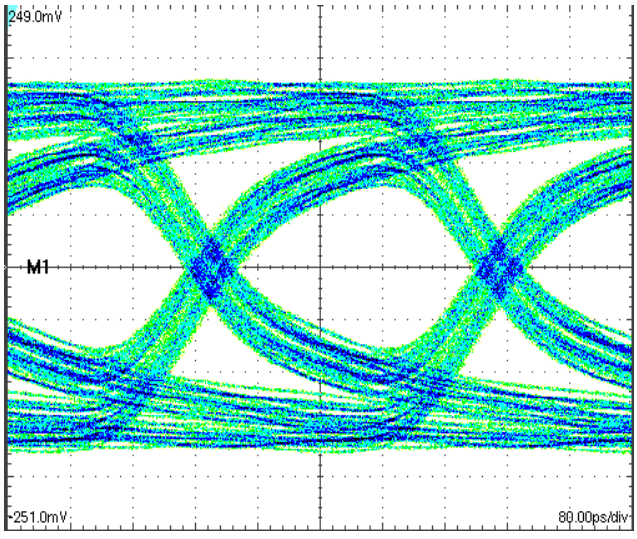
Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	3.3 V
Main Link Input Voltage	V_{ID} = 0.15 to 1.4 Vpp
Control Pin Max Voltage for Low	0.5 V
Control Pin Voltage Range Mid	Min (V_{CC}/2) - 0.3 V to Max of (V_{CC}/2) + 0.3 V
Control Pin Min Voltage for High	Min V_{CC} - 0.5 V
Main Link AC Decoupling Cap	75 nF to 200 nF Recommend 100 nF

10.2.2 Detailed Design Procedure

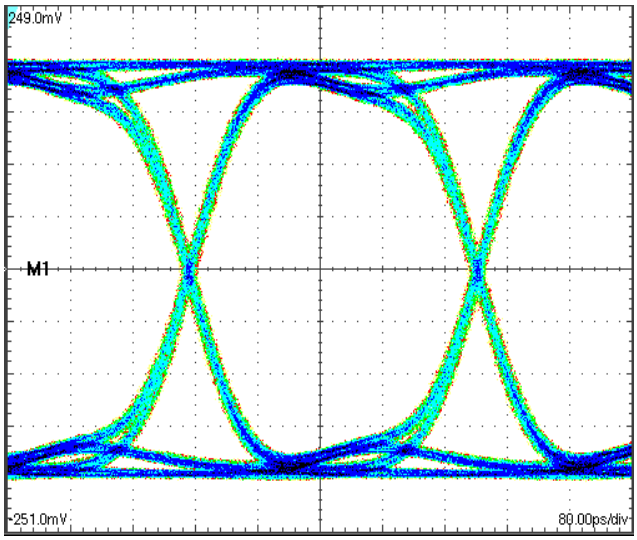
- Determine the output swing of the Graphic Processing Unit (GPU) .
- Determine the loss profile between the GPU and the LCD display connector.
- Determine the loss profile between the mother board LCD display connector and the DisplayPort receiver.
- Determine the DisplayPort receiver capabilities, acceptable VID along with its receive equalizer capability.
- Based upon this loss profile and signal swing determine optimal location for the SN75DP119, close to the connector, midway, or close to GPU.
- Use the typical application drawing, Figure 9, for information on using the AC coupling caps and control pin resistors.
- Set the DP119 Input equalizer appropriately to support the loss profile and signal swing for the link between the GPU and connector by using the EQ_CTL control pin.
- Set the DP119 VOD and Pre-emphasis level appropriately to support the Connector to DisplayPort receiver link by using the PRE_CTL and VOC_CTL control pins.
- The thermal pad must be connected to ground.
- Use a 1 µF and 0.1 µF decouple caps from VCC pins to Ground.

10.2.3 Application Curves



Trace Length = 16 (inches) [width = 4 mil]
DR = 2.7 Gbps V_{OD} = 400 mVpp PRE = 0 dB

Figure 10. Eye Pattern Output To DP119



Trace Length = 16 (inches) [width = 4 mil]
DR = 2.7 Gbps V_{OD} = 400 mVpp PRE = 0 dB

Figure 11. Eye Pattern Output To DP119

11 Power Supply Recommendations

SN75DP119 is designed to run from a single supply voltage of 3.3V.

12 Layout

12.1 Layout Guidelines

- Data rates of 2.7Gbps require fast edge rate, which can cause EMI radiation if the pcb is not designed carefully.
- Decoupling with small current loops is recommended.
- It is recommended to place the de-coupling cap as close as possible to the device and on the same side of the pcb (see Figure 12).
- Choose the capacitor such that the resonant frequency of the capacitor does not align closely with 2.7GHz.
- Also provide several GND vias to the thermal pad to minimize the area of current loops.

12.2 Layout Example

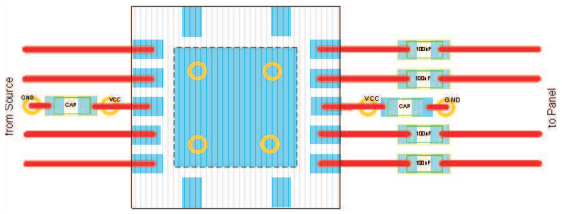


Figure 12. De-Coupling Layout Recommendation

13 Device and Documentation Support

13.1 Trademarks

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75DP119RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DP119	Samples
SN75DP119RGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DP119	Samples
SN75DP119RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DP119	Samples
SN75DP119RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DP119	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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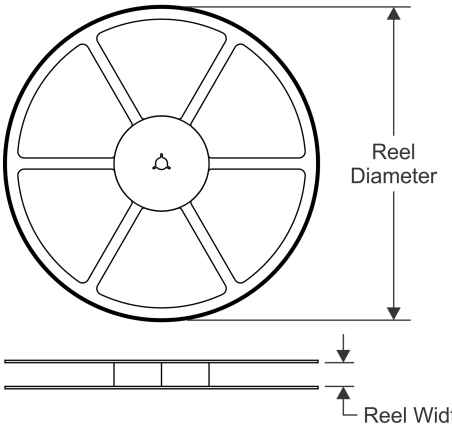
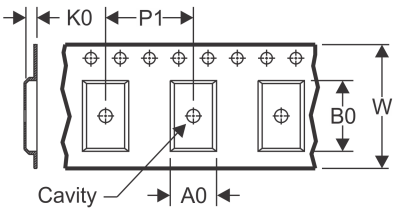
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

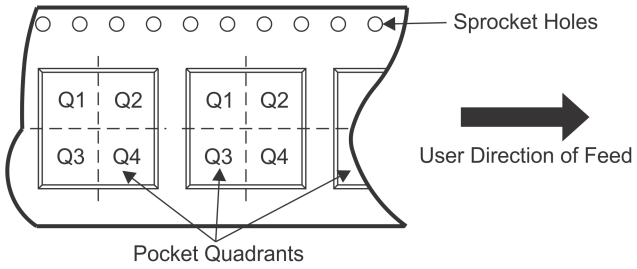


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

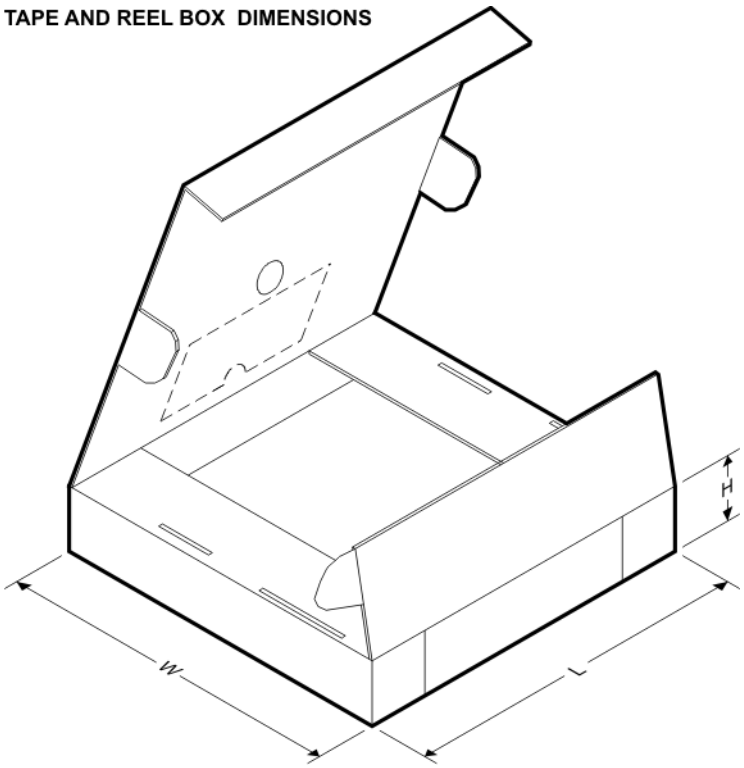
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP119RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN75DP119RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN75DP119RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
SN75DP119RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

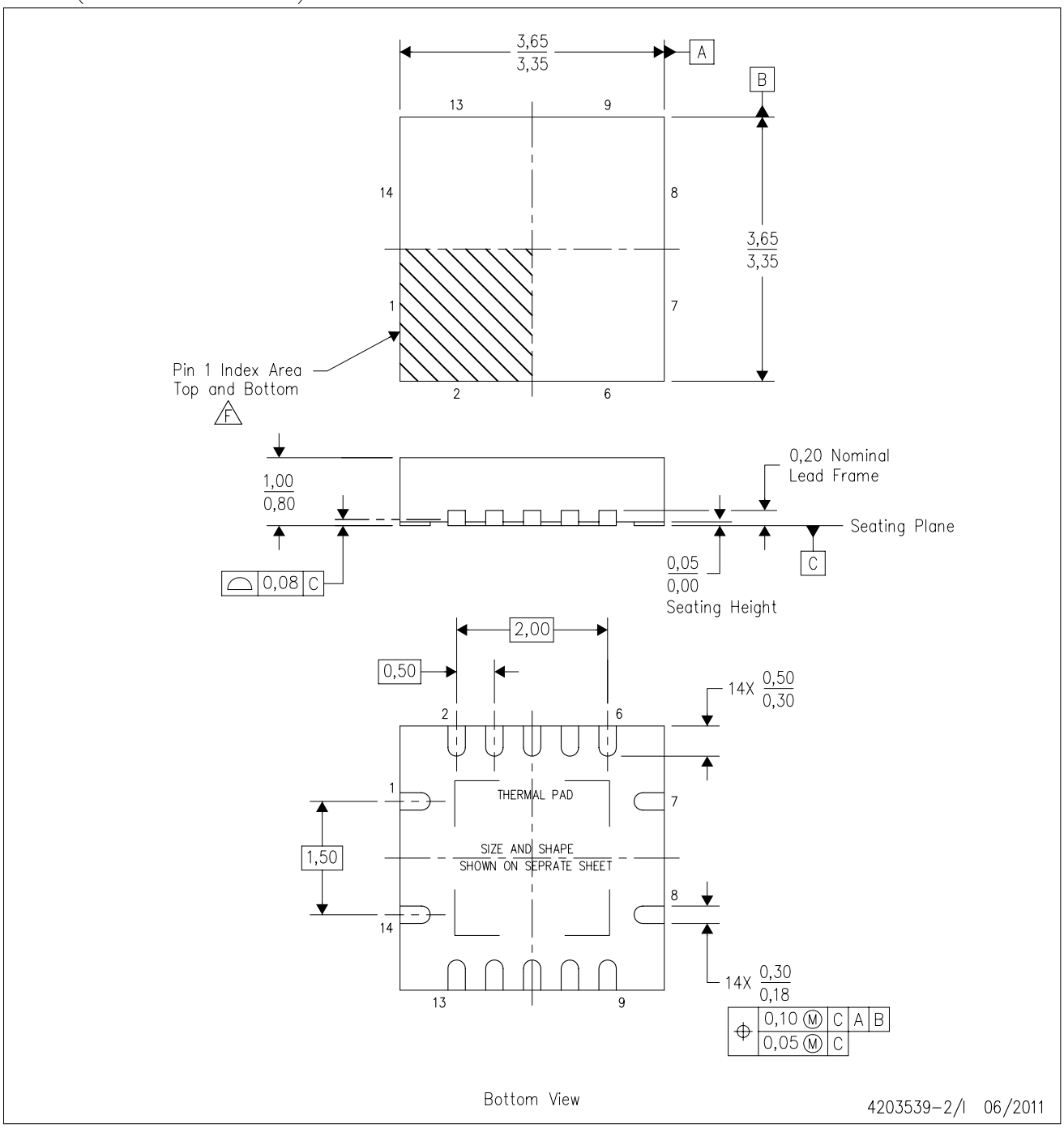
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP119RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
SN75DP119RGYT	VQFN	RGY	14	250	210.0	185.0	35.0
SN75DP119RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
SN75DP119RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

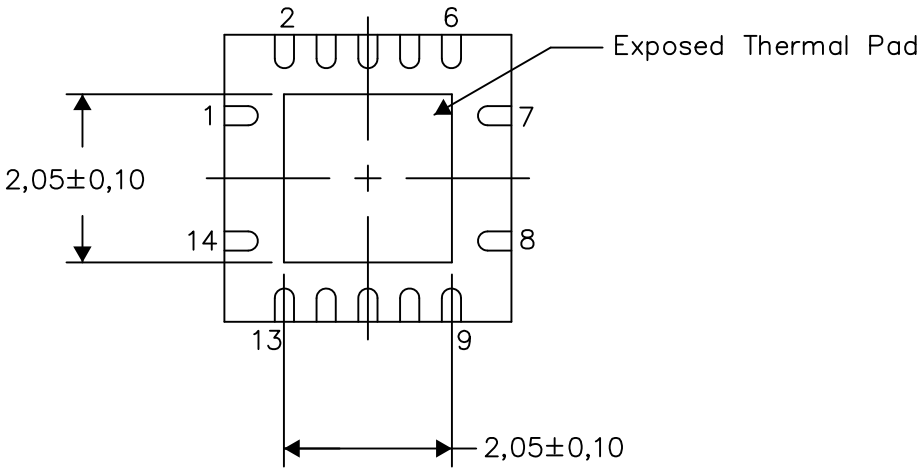
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



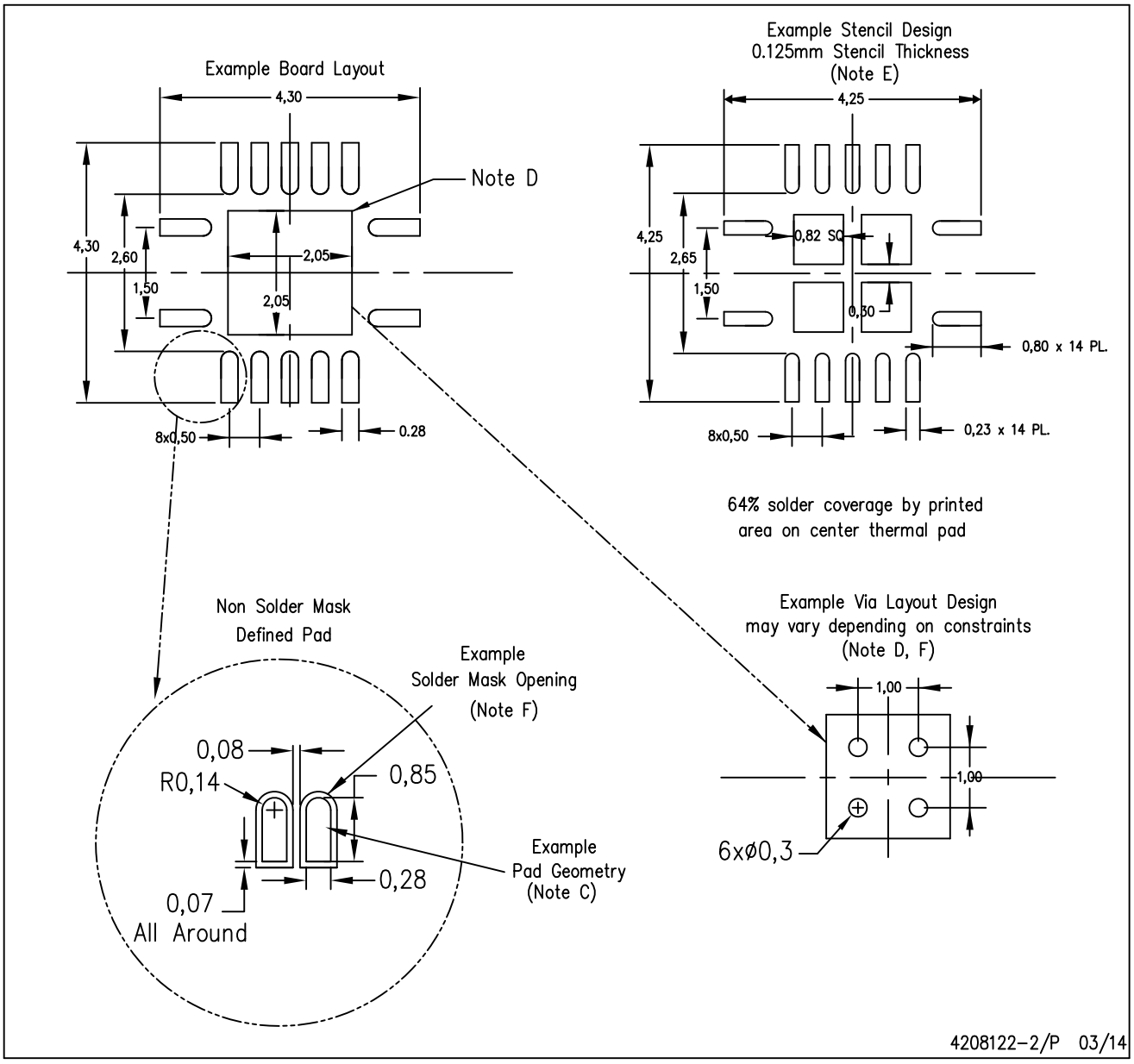
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

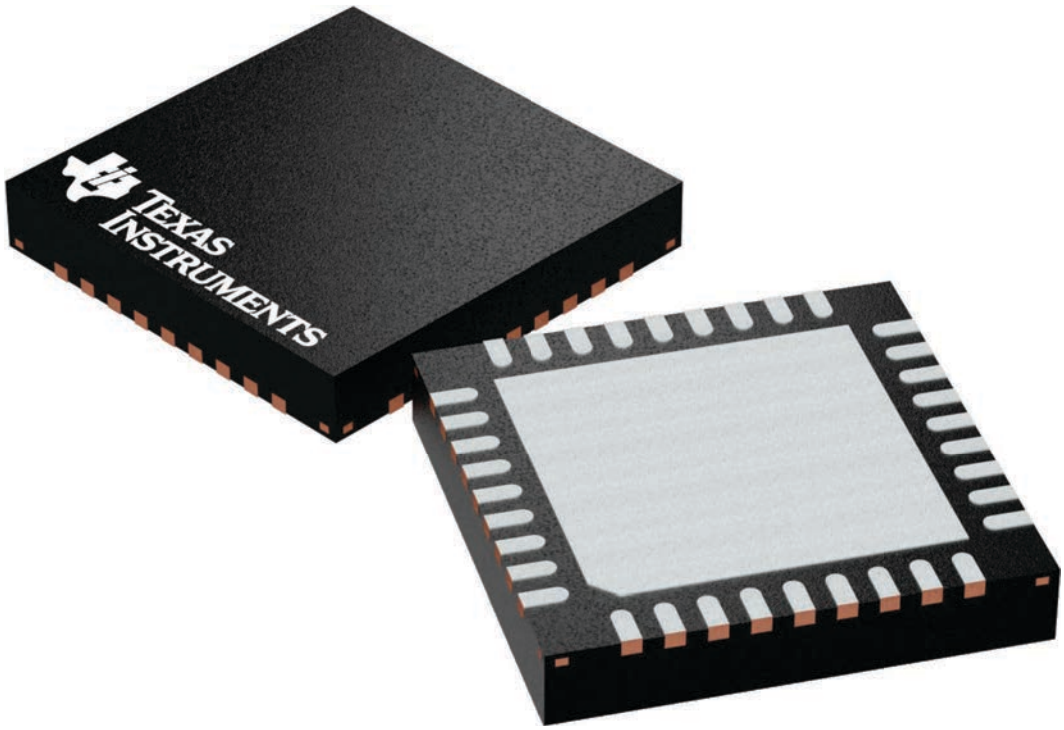
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



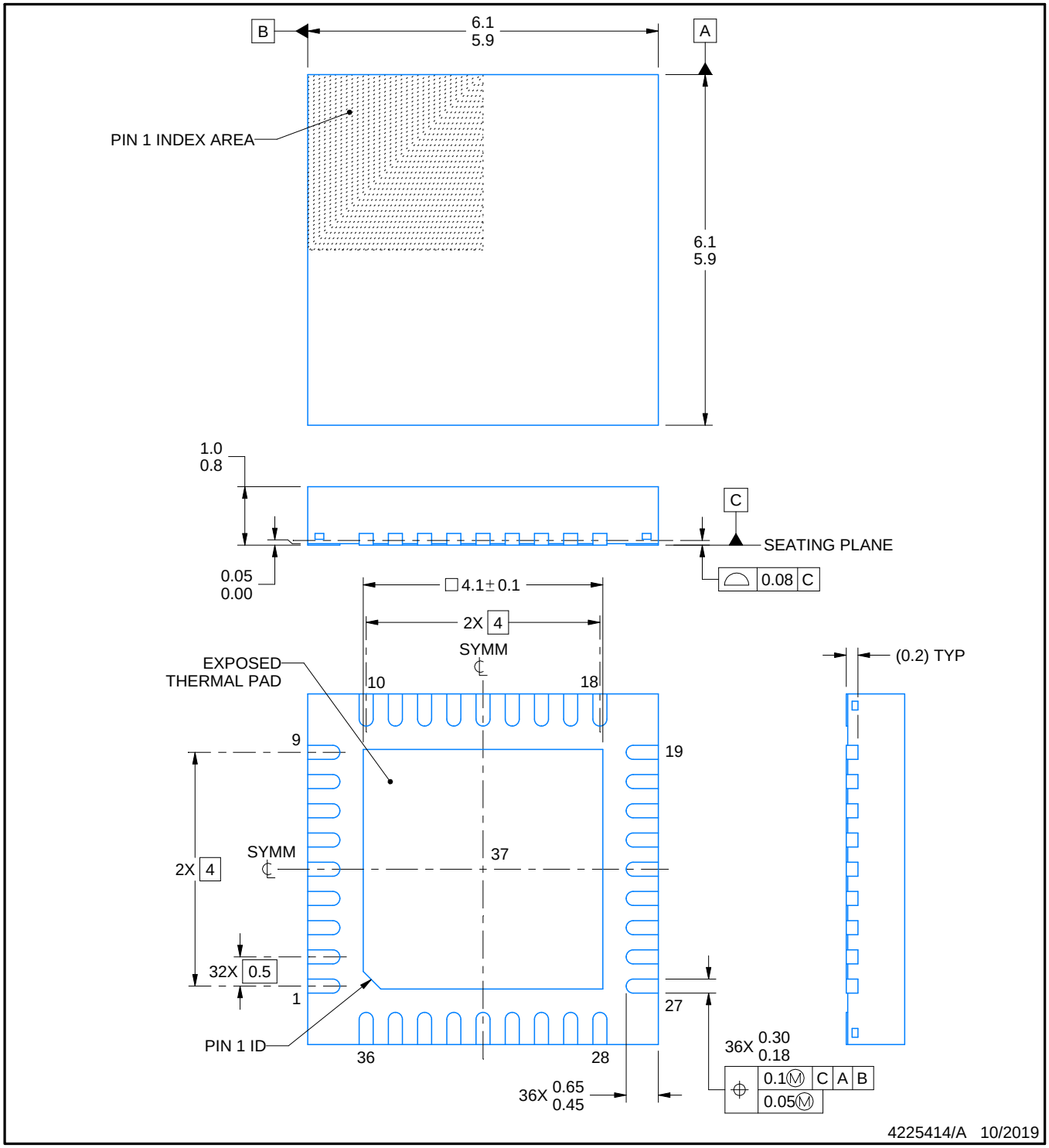
4225440/A

RHH0036B

PACKAGE OUTLINE

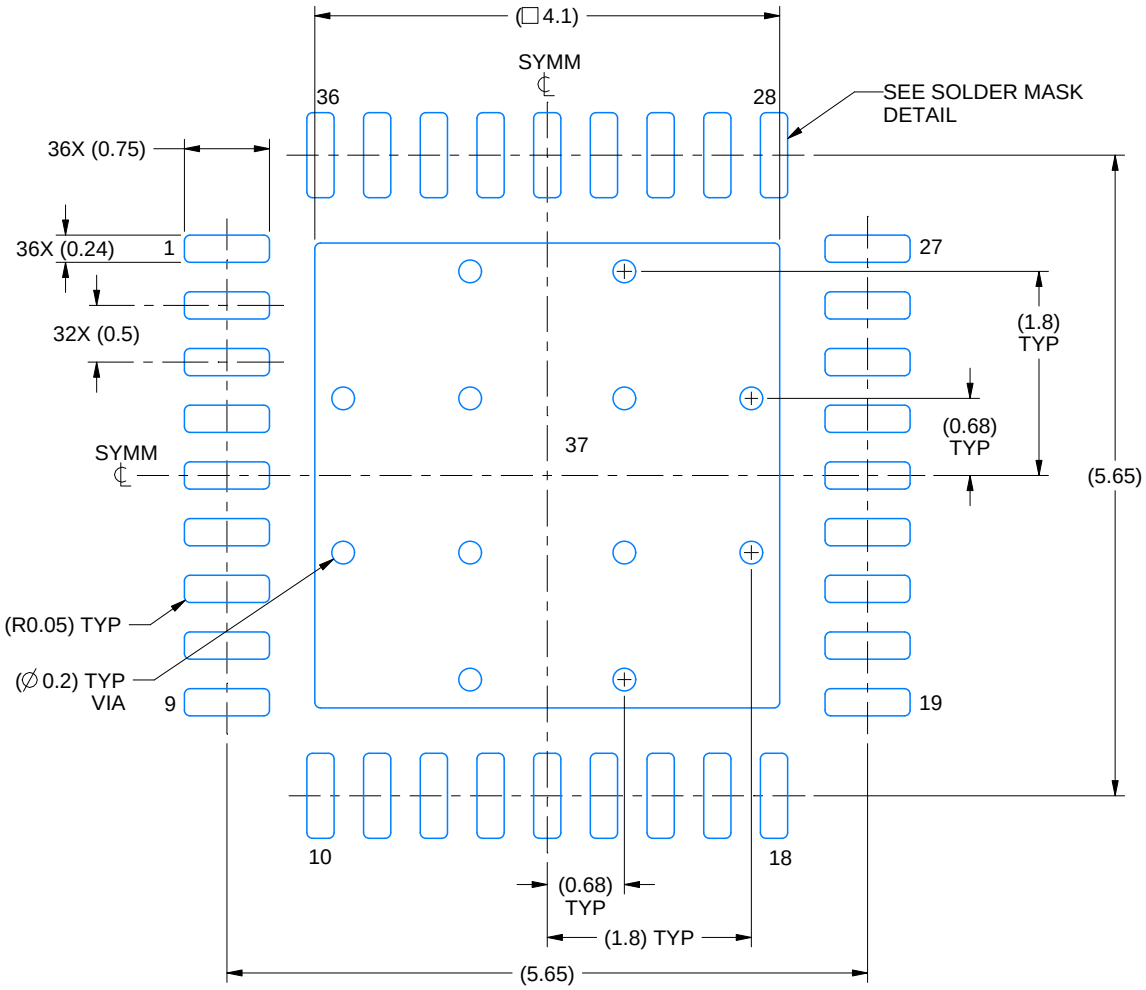
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

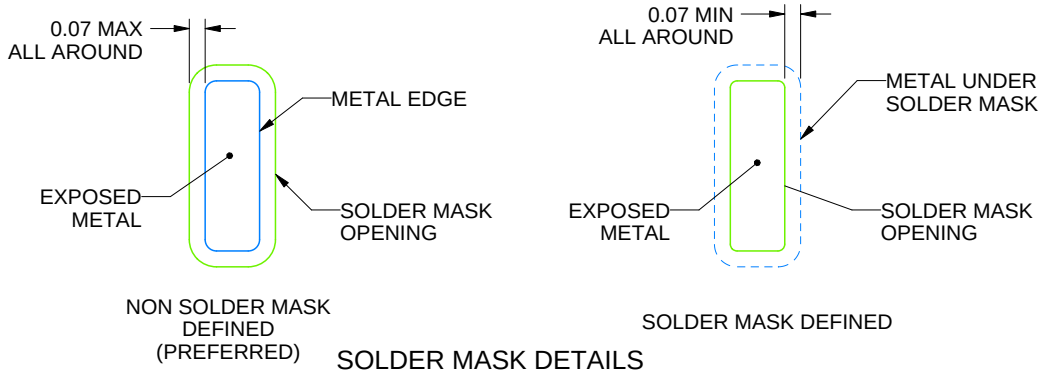


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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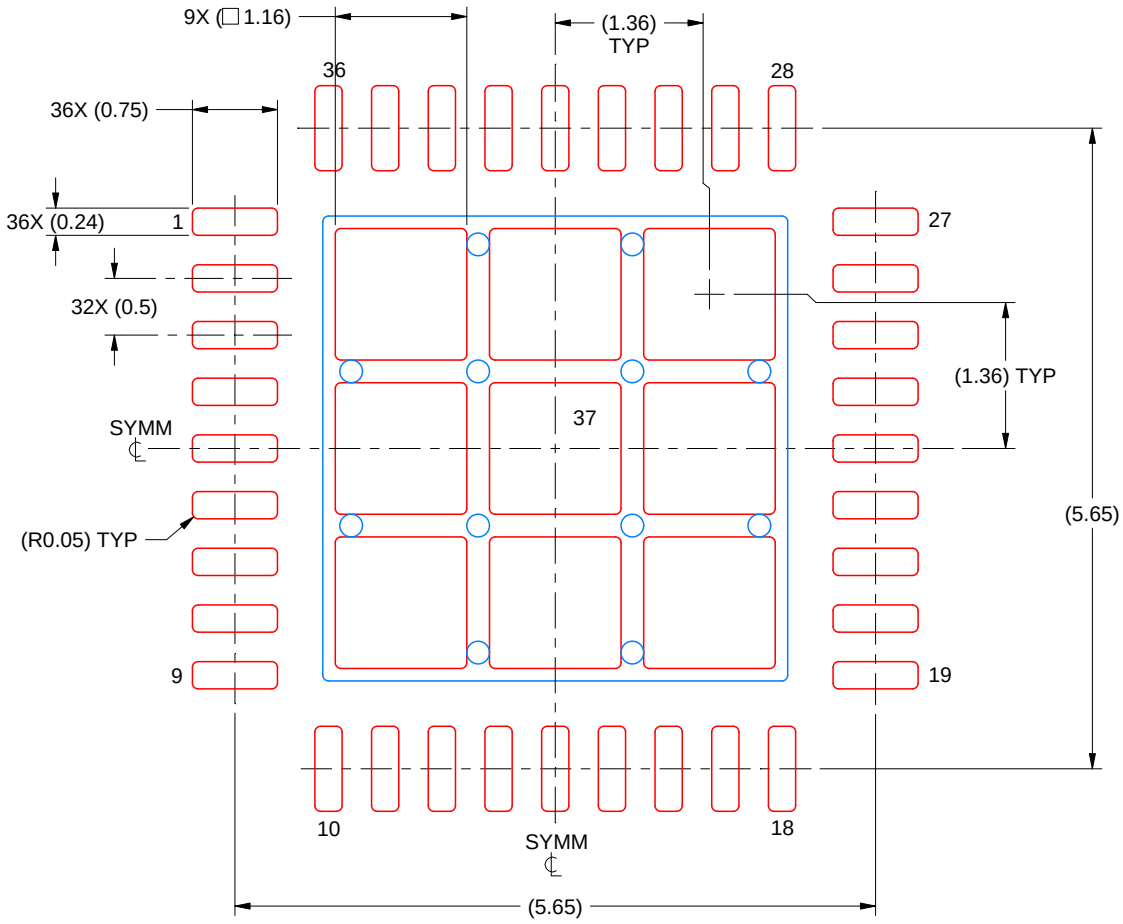
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225414/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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