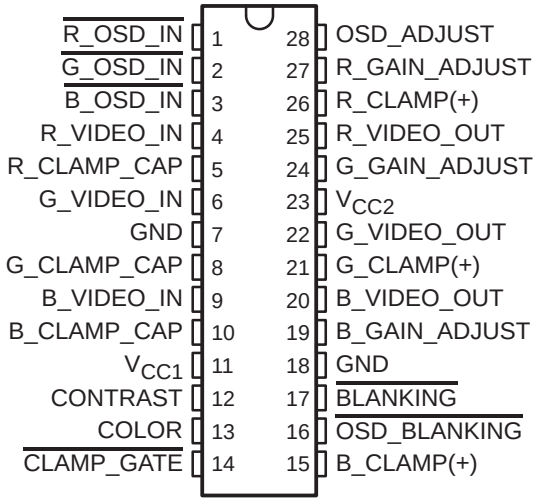
- **Wide Bandwidth . . . Typ 100 MHz at –3 dB**
- **Color Saturation Control Features**
- **Digital Level Control (0 V to 4 V) for Contrast, Color, and Brightness**
- **Mixer Function for OSD Applications**
- **Blanking Function for On-Screen Display (OSD) Applications**
- **Fewer Peripheral Components Required**
- **Low-Impedance Output Driver**

N PACKAGE
(TOP VIEW)



description

The TLS1255 is a wide-band video preamplifier system intended for high-resolution red-green-blue (RGB) color monitors with color-saturation control features. The saturation of a color refers to the degree of chroma or purity, or the degree of freedom from admixture with white. In addition to the RGB preamplifier function, the TLS1255 provides color-saturation control and gain control at the video system outputs. Each video amplifier (R, G, and B) contains a gain set for adjusting maximum system gain (A_V = 6 dB). The TLS1255 provides a digital level-operated contrast, brightness, color, and gain adjustment. The video-output stages from TLS1255 directly drive CRT power amplifiers.

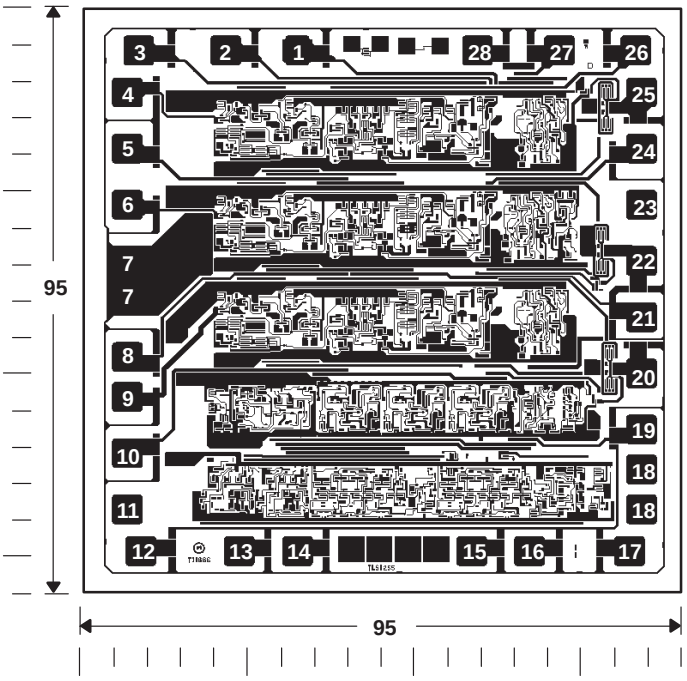
The system has been designed to operate from a 12-V supply with all digital level controls operating over a 0-V to 4-V range to make the interface to serial digital buses possible. The TLS1255 also contains a blanking circuit that clamps the video output voltage to within 0.2 V of ground. The mixer circuit required for the OSD application is also integrated into the TLS1255, which makes the design of video boards and other applications easier.

The TLS1255 is characterized for operation from 0°C to 70°C.

TLS1255Y chip information

This chip, when properly assembled, displays characteristics similar to the TLS1255. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NO BACKSIDE METALIZATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	13.5 V
Input voltage range, V_I (see Note 1)	0 V to V_{CC}
Video output current, I_O (per channel)	28 mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2.37 W
Operating virtual junction temperature range, T_J	150°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All V_{CC} terminals must be externally wired together to prevent internal damage during V_{CC} power-on/-off cycles.
2. For operation above 25°C free-air temperature, derate linearly to 1.52 W at the rate of 19 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1} and V_{CC2}		11	12	13	V
High-level input voltage range, $\overline{\text{CLAMP GATE}}$, V_{IH}	Clamp comparators off	2.4		5	V
Low-level input voltage range, $\overline{\text{CLAMP GATE}}$, V_{IL}	Clamp comparators on	0		0.8	V
High-level input voltage range, $\overline{\text{BLANKING}}$, V_{IH}	Blanking circuit inactive	2.4		5	V
Low-level input voltage range, $\overline{\text{BLANKING}}$, V_{IL}	Blanking circuit active	0		0.8	V
High-level input voltage range, $\overline{\text{OSD BLANKING}}$, V_{IH}	OSD Blanking circuit inactive	2.4		5	V
Low-level input voltage range, $\overline{\text{OSD BLANKING}}$, V_{IL}	OSD Blanking circuit active	0		0.8	V
Operating free-air temperature, T_A		0		70	°C

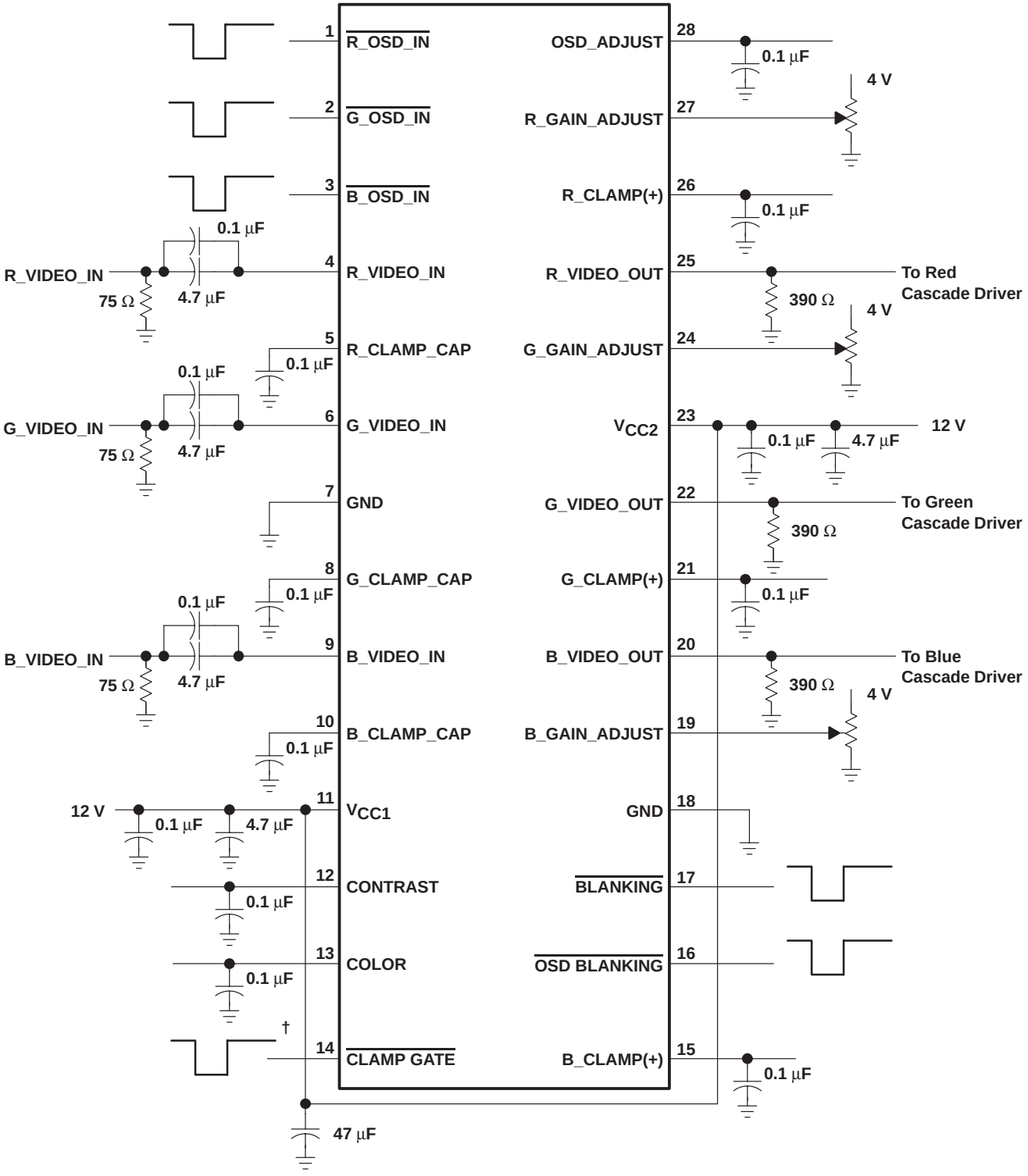
electrical characteristics at 25°C free-air temperature range, $\overline{\text{CLAMP GATE}}$ = COLOR = 0 V; R,G,B CLAMP(+) = 2 V; $\overline{\text{BLANKING}}$ = $\overline{\text{OSD BLANKING}}$ = 4 V; CONTRAST = R, G, B GAIN ADJUST = 4 V; $V_{CC1} = V_{CC2}$ = 12 V (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current		$V_{CC1} + V_{CC2}$		110	130	mA
V_{ref}	Video input reference voltage		Measure R,G,B VIDEO_IN voltage	1.6	1.8	2.1	V
I_{IL}	$\overline{\text{CLAMP GATE}}$ low input current		$\overline{\text{CLAMP GATE}}$ = 0 V		–0.5	–8	µA
I_{IH}	$\overline{\text{CLAMP GATE}}$ high input current		$\overline{\text{CLAMP GATE}}$ = 12 V		0.005	1	µA
	Clamp-capacitor charge current	$I_{K(chg)}$	R,G,B CLAMP CAP = 0 V		850		µA
	Clamp-capacitor discharge current	$I_{K(dschg)}$	R,G,B CLAMP CAP = 5 V		–850		µA
V_{OL}	Low-level output voltage		R,G,B CLAMP CAP = 0 V		0.2	0.6	V
V_{OH}	High-level output voltage		R,G,B CLAMP CAP = 5 V	6.7	7.6		V
	Video output blanked voltage	$V_{O(BLANK)}$	$\overline{\text{BLANKING}}$ = 0 V; R,G,B CLAMP(+) = 3 V		0.2	0.35	V
	High-level output voltage, OSD	$V_{O(OSD\ BLANK)}$	$\overline{\text{OSD BLANKING}}$ = 0 V, $V_{O(PP)(OSD)}$ = 4 V			0.8	V
	Output voltage difference	V_{ODIFF}	Between any two channels			50	mV
	Spot-killer voltage	V_{SPOT}	V_{CC} adjusted to active	8.2		10.3	V

operating characteristics at 25°C free-air temperature, $\overline{\text{CLAMP GATE}}$ = COLOR = 0 V; R,G,B CLAMP(+) = 2 V, $\overline{\text{BLANKING}}$ = $\overline{\text{OSD BLANKING}}$ = 4 V; CONTRAST = R,G,B GAIN ADJUST = 4 V; $V_{CC1} = V_{CC2}$ = 12 V (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{V(max)(CONTRAST)}$	Maximum voltage amplification	$A_{VMAX(cont)}$	CONTRAST = 4 V, COLOR = 0 V, $V_{I(PP)}$ = 700 mV		7.6		V/V
			CONTRAST = 4 V, COLOR = 4 V, $V_{I(PP)}$ = 700 mV		7.6		V/V
$t_{r(video)}$	Rise time, video output	$T_{r(video)}$	$V_{O(PP)}$ = 4 V		3.5		ns
$t_{f(video)}$	Fall time, video output	$T_{f(video)}$	$V_{O(PP)}$ = 4 V		3.5		ns
$t_{r(BLANK)}$	Rise time, blank output	$T_{r(BLANK)}$	BLANKING = 0 V, Blanking output $V_{I(PP)}$ = 1 V		7		ns
$t_{f(BLANK)}$	Fall time, blank output	$T_{f(BLANK)}$	BLANKING = 0 V, Blanking output $V_{O(PP)}$ = 1 V		7		ns
$t_{r(OSD\_BLANK)}$	Rise time, OSD blank output	$T_{r(OSD\ BLANK)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; OSD_ADJUST = 0 V		7		ns
$t_{f(OSD\_BLANK)}$	Fall time, OSD blank output	$T_{f(OSD\ BLANK)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; OSD_ADJUST = 0 V		7		ns
$t_{r(OSD\_MIXER)}$	Rise time, OSD mixer	$T_{r(OSD\ MIXER)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; $V_{O(PP)(OSD)}$ = 4 V		7		ns
$t_{f(OSD\_MIXER)}$	Fall time, OSD mixer	$T_{f(OSD\ MIXER)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; $V_{O(PP)(OSD)}$ = 4 V		7		ns
t_{pd}	Propagation delay, video to OSD MIXER	$T_{rprop(OSD)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; $V_{O(PP)(OSD)}$ = 4 V		15		ns
		$T_{fprop(OSD)}$	$\overline{\text{OSD\_BLANKING}}$ = 0 V; $V_{O(PP)(OSD)}$ = 4 V		15		ns
BW	Bandwidth, amplifier	bw (–3dB)	$V_{O(PP)}$ = 4 V, CLAMP+ = 2 V		100		MHz

APPLICATION INFORMATION



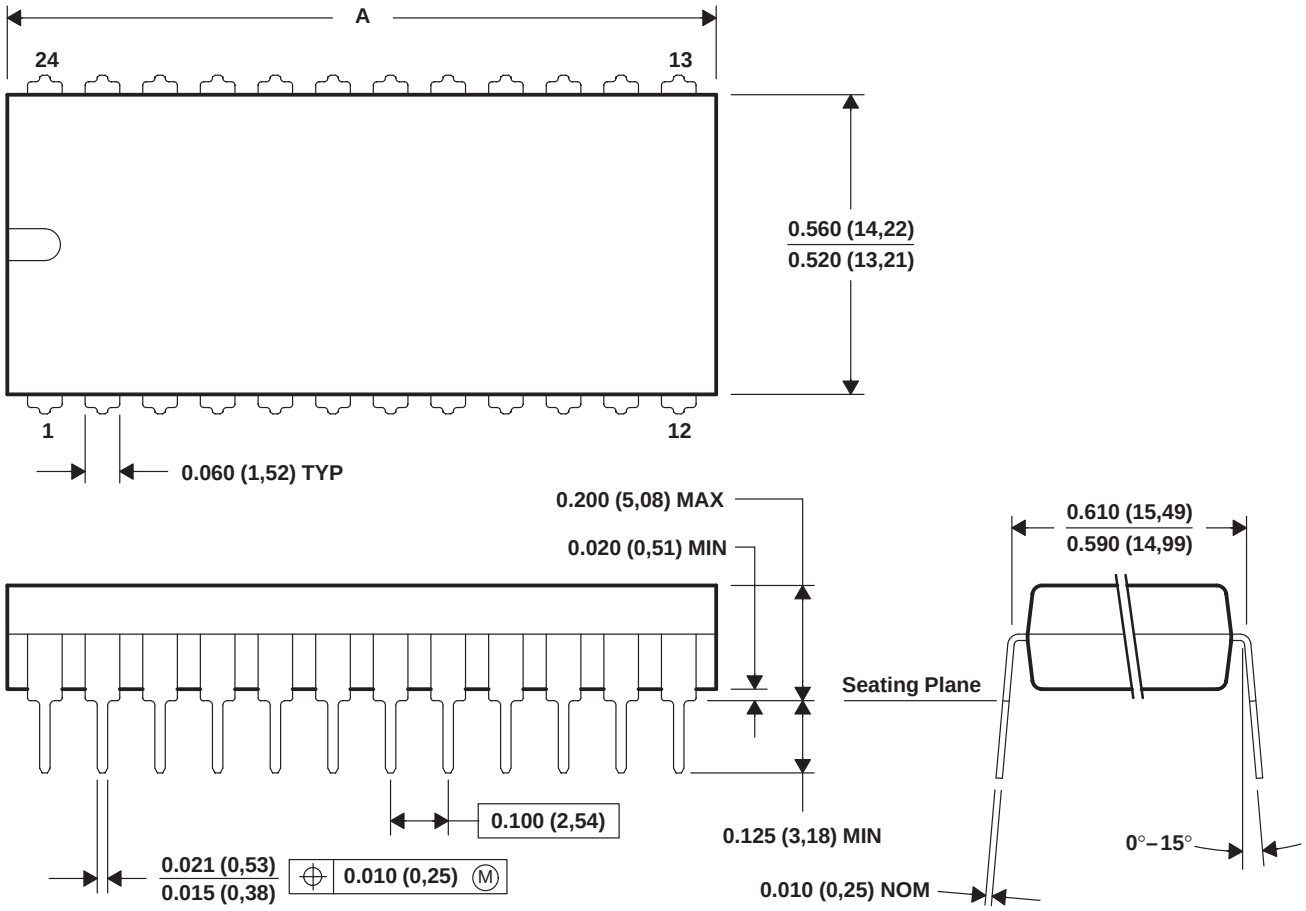
† Minimum pulse width = 300 ns

Figure 1. Application and Test Circuit

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLS1255N	OBSOLETE	PDIP	N	28		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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