POWER MANAGEMENT

Description

The SC2420 can be configured as a dual converter or a bi-phase converter for high current applications. The part is designed for point of use power supplies with 10-14V nominal backplane power sources. The power dissipation is controlled using a novel low voltage supply technique, allowing high speed and integration, with the high drive currents to ensure low MOSFET switching loss. The synchronous buck configuration also allows converter sinking current from load without losing output regulation.

The use of high speed switching circuits allows very narrow PWM outputs allowing up to 10:1 voltage ratios. Single pin compensation for each channel simplifies development as well as reducing external pin count.

Capable of driving MOSFETs via external driver transistors for phase currents beyond 20A.

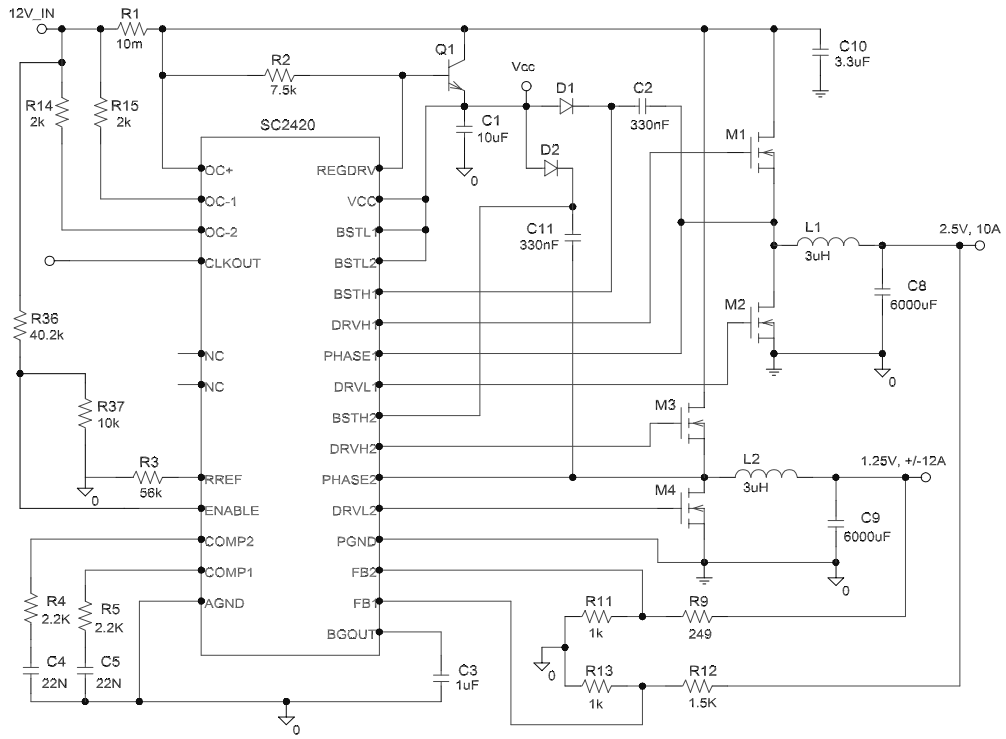
Features

- Selectable dual output or bi-phase operation
- Direct drive for N-channel MOSFETs
- Undervoltage lockout
- Source and sink current
- Soft start
- Fast transient response
- Max duty cycle 45%
- Output over voltage protection
- Thermal shut down

Applications

- DDR memory power supplies
- Point of use power supplies

Typical Application Circuit



Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Supply Voltage	V_{IN}	16	V
Voltage on BST Pins	V_{BST}	24	V
Oscillator Frequency		2	MHz
VCC		8	°C/W
Thermal Resistance Junction to Case	θ_{JC}	25	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	80	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Lead Temperature (Soldering) 10 seconds	T_{LEAD}	300	°C

Note:

(1) Maximum frequency and maximum supply voltage could cause excessive dissipation in the part.

Electrical Characteristics

Unless specified: V_{IN} = 12V; T_A = 25°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_{IN}		10		14	V
Supply Current	ENABLE = 0		30	40	mA
Under Voltage Lock Out			5.8		V
UVLO Hysteresis			400		mV
Voltage Regulator					
Pre Regulator Voltage		6		7	V
Bgout Voltage	C_{LOAD} = 4.7nF	0.99	1	1.01	V
Bgout Impedance			3		KΩ
REGDRV Pin Sink Current	I_{REGDRV}		5		mA
Error Amp					
Input Offset Voltage			10		mV
Input Impedance		5			KΩ
Linear Transconductance			.002		A/V
Internal Oscillator					
Frequency	R_{REF} = 30K		1		MHz
Frequency	R_{REF} = 60K		500		kHz
Ramp Valley to Peak	V_{IN} = 12V		1.5		V

Electrical Characteristics (Cont.)

Unless specified: V_{IN} = 12V; T_A = 25°C.

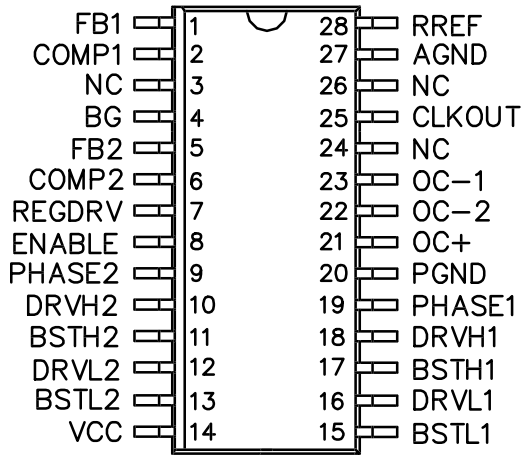
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Side Gate Drive					
Max Duty Cycle			45		%
Peak Source	C_{LOAD} = 10nF		1		A
Peak Sink	C_{LOAD} = 10nF		1		A
Low Side Gate Drive					
Peak Source	C_{LOAD} = 10nF		2		A
Peak Sink	C_{LOAD} = 10nF		2		A
Sync Drive Timing					
Minimum Non-overlap	C_{LOAD} = 1nF Fet Drive < 1V		40		ns
PWM Match	50% Duty cycle, F_{OSC} = 1 MHz	-1		1	%
Logic Input Pins					
Input Bias Current	V_{IN_LOGIC} = 0 - 5V	-10		10	µA
Logic Threshold			0.8		V
FB2 Disable Threshold			V_{CC} - 0.7V		V
Over Current Protection					
OC+ I/P Bias Current	V_{IN} = 12V		400		µA
OC- I/P Bias Current	@ Trip voltage	40	50	60	µA
Over Voltage Protection					
OVP Threshold			120		%
Thermal Shut Down			150		°C

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration

Top View



(28 Pin SOIC)

Ordering Information

Part Number[1]	PACKAGE	T_{AMB} (T_A)
SC2420ISWTR	SO-28	-40 - +85°C
SC2420EVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.

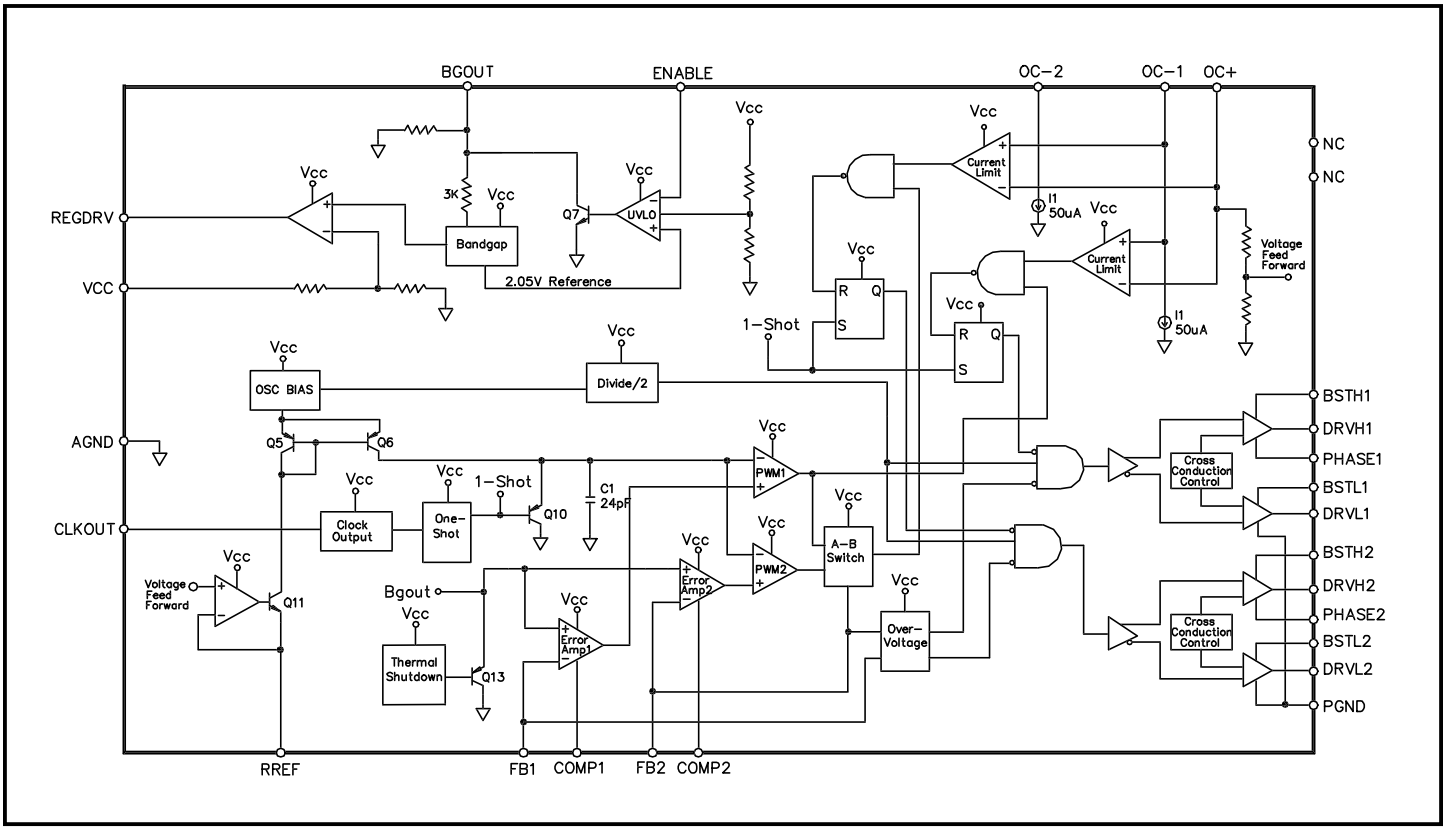
Pin Descriptions

Pin	Pin Name	Pin Function
1	FB1	Feedback for channel 1.
2	COMP1	Compensation for channel 1.
3	NC	No connection.
4	BG	1V reference for error amplifiers, 3K source impedance.
5	FB2	Feedback for channel 2.
6	COMP2	Compensation for channel 2.
7	REGDRV	Regulator drive for external pass transistor.
8	ENABLE	Enable threshold is 2.05 V, connect to ground to disable.
9	PHASE2	Phase node input for channel 2.
10	DRVH2	Gate drive for high side channel 2.
11	BSTH2	Bootstrap input for high side channel 2.
12	DRVL2	Gate drive for low side channel 2.
13	BSTL2	Supply for low side channel 2.
14	VCC	Pre-regulated IC power supply.
15	BSTL1	Supply for low side channel 1.
16	DRVL1	Gate drive for low side channel 1.
17	BSTH1	Bootstrap input for high side channel 1.
18	DRVH1	Gate drive for high side channel 1.

Pin Descriptions (Cont.)

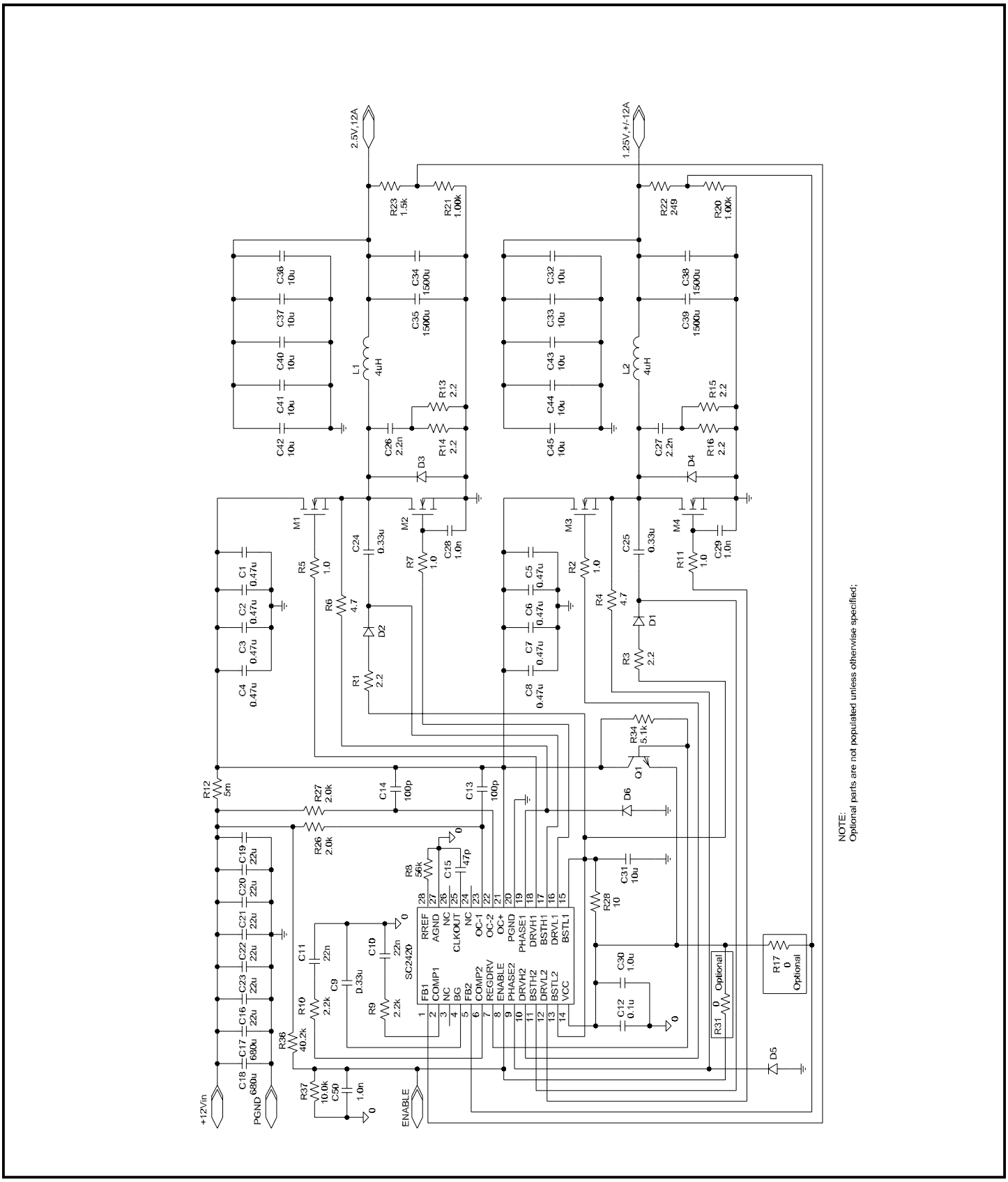
Pin	Pin Name	Pin Function
19	PHASE1	Phase node input for high side channel 1.
20	PGND	Power ground.
21	OC+	Overcurrent comparator inverting input.
22	OC-2	Overcurrent comparator non-inverting input for channel 2.
23	OC-1	Overcurrent comparator non-inverting input for channel 1.
24	NC	No connection.
25	CLKOUT	Clock out, logic level drive to provide synchronizing signal for other converters.
26	NC	No connection.
27	AGND	Analog ground.
28	RREF	External reference resistor for internal oscillator and ramp generator.

Block Diagram



Typical Application Schematic

Two Channel Operation



Bill of Material

Two Channel Operation

Item	Qty	Reference	Part Number/Value	Manufacturer
1	8	C1 - C8	0.47µF, 50V, Cer.	Any
2	3	C9,C24,C25	0.33µF, Cer., 1206	Any
3	2	C10,C11	22nF, Cer., 1206	Any
4	1	C12	0.1µF, Cer., 1206	Any
5	2	C13,C14	100pF, Cer., 1206	Any
6	1	C15	47pF, Cer., 1206	Any
7	6	C16,C19,C20,C21,C22,C23	22µF, 35V, Tant.	Any
8	2	C17,C18	680µF, 35V, Alum.	Any
9	2	C26,C27	2.2nF, Cer., 1206	Any
10	3	C28,C29,C50	1.0nF, Cer., 1206	Any
11	1	C30	1.0µF, Cer., 1206	Any
12	11	C31,C32,C33,C36,C37,C40,C41,C42,C43,C44,C45	10µF, Cer., 1206	Any
13	4	C34,C35,C38,C39	1500µF, 6.3V, Alum.	Any
14	4	D1,D2,D5,D6	1A, 40V, Schottky, MELF, 1N5819M	Any
15	2	D3,D4	3A, 40V, Schottky, 30BQ040	Any
16	2	L1,L2	Inductor, 9 turns	Magnetics: Kool Mu P/N: 77206-A7
17	4	M1,M2,M3,M4	N-Channel MOSFET, TO-263AB	Fairchild P/N: FDB7030BL
18	1	Q1	80V, 1A, NPN, Med. Pwr. SOT-223	BCP56CT
19	2	R1,R3	2.2, 5%, 1206	Any
20	2	R4,R6	4.7, 5%, 1206	Any
21	4	R2,R5,R7,R11	1.0, 5%, 1206	Any
22	1	R8	56k, 5%, 1206	Any
23	2	R9,R10	2.2k, 5%, 1206	Any
24	1	R12	Chip resistor, 0.005, 1W, 1%, 2512	Any

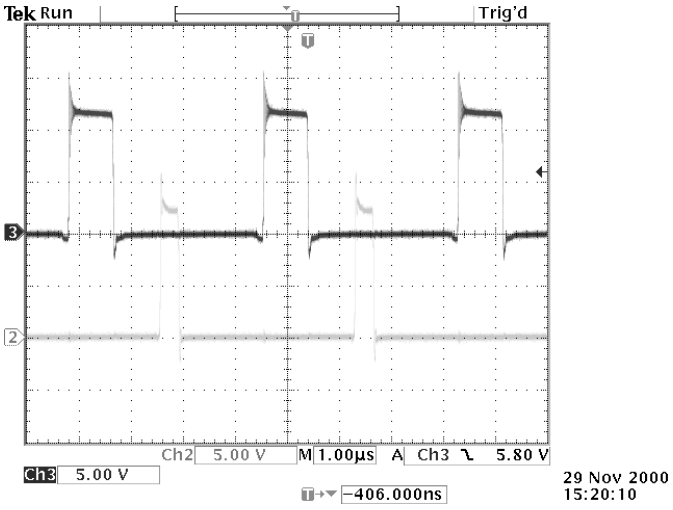
Bill of Material (Cont.)

Two Channel Operation (Cont.)

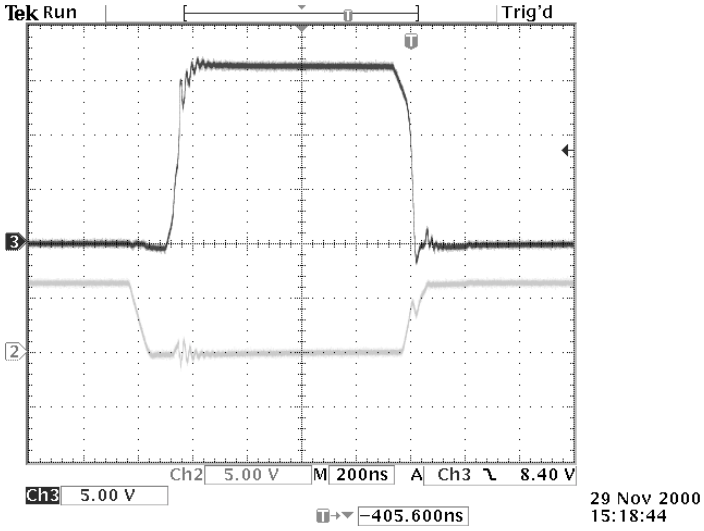
Item	Qty	Reference	Part Number/Value	Manufacturer
25	4	R13,R14,R15,R16	2.2, 1/4W, 5%, 1210	Any
26	0	R17*, R31*	Chip resistor, 0, 1206	Any
27	2	R20,R21	1.00k, 1%, 1206	Any
28	1	R22	249, 1%, 1206	Any
29	1	R23	1.5k, 1%, 1206	Any
30	2	R26,R27	2.0k, 5%, 1206	Any
31	1	R28	10, 5%, 1206	Any
32	1	R34	5.1k, 5%, 1206	Any
33	1	R36	40.2k, 1%, 1206	Any
34	1	R37	10.0k, 1%, 1206	Any
35	1	SC2420	Bi-Phase/Dual Controller, SO-28W	Semtech Corp. P/N: SC2420ISW 805-498-2111

Notes:
1. * Indicates optional parts.
2. Some parts are selected due to availability or lead time, and are not optimized.

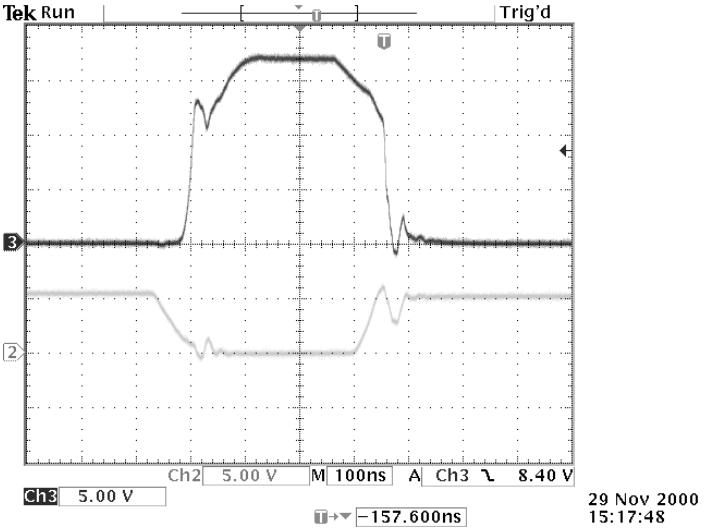
Electrical Characteristic Curves



Phase Node Waveform
of the Two Channel Evaluation Circuit
(Vin = 12V, 2.5V output source 10A,
1.25V output sink 10A)
Ch2: Phase node of 1.25V channel
Ch3: Phase node of 2.5V channel



Gate Drive Waveform
of the Two Channel Evaluation Circuit
(Vin = 12V, 2.5V output source 10A,
1.25V output sink 10A)
Ch2: Bottom Gate of 2.5V channel
Ch3: Top Gate of 2.5V channel



Gate Drive Waveform
of the Two Channel Evaluation Circuit
(Vin = 12V, 2.5V output source 10A,
1.25V output sink 10A)
Ch2: Bottom Gate of 1.25V channel
Ch3: Top Gate of 1.25V channel

Applications Information

THEORY OF OPERATION

The SC2420 employs a voltage mode control with feed forward to provide fast output response to load and line transients.

The SC2420 has two outputs, which can be used to generate two separate supply voltages or can be combined in bi-phase operation to generate one single supply voltage. The internal reference is trimmed to 1V with +/-1% accuracy, and the outputs voltages can be adjusted by two external resistors. In bi-phase operation, the dual switching regulators are operated 180° out of phase. Load current sharing between phases is normally required, and this can be achieved by using precise feedback voltage divider resistors (typically 0.1%) to match individual phase output voltage. In addition, small drooping resistors (could be PCB traces) are employed at the output of each phase to enhance phase current balance.

PWM Control

Changes on the output voltages are fed to the inverting input of the Error Amplifiers, by the FB1 and FB2 pins, and compared with the internal 1V reference. The compensation to the transconductance amplifier is achieved by connecting a capacitor in series with a resistor from the COMP1 and COMP2 pins to AGND respectively. The error signal from the error amplifier is compared to the saw tooth waveform by the PWM comparator, and matched timing signal is generated to control the upper and lower gate drives of the two phases. A single Ramp signal is used to generate the control signals for both of the phases, hence the maximum duty cycle is less than 50%.

Oscillator Frequency Selection

The sawtooth signal is generated by charging an internal capacitor with a current source. The charge current is set by an external resistor connected from the RREF pin to AGND. The oscillator frequency and the external resistance follow linear relationship.

Feed Forward

The SC2420 incorporates a voltage feed forward scheme to improve line transient immunity when changes in the input voltage occur. As the input voltage changes, the ramp valley to peak voltage of the internal oscillator follows this change instantly. As a result the output voltage will have minimum disturbance due to the input line change.

Bias Generation

A 6-7 Volt supply voltage is required to power up the SC2420. This voltage could be provided by an external power supply or derived from VIN through and external pass transistor.

REGDRV is the control signal to the base of the pass transistor that will regulate VCC. The voltage at the VCC pin is compared to the internal voltage reference, and the REGDRV pin can sink up to 5mA current to the voltage at the VCC pin.

Enable

If the ENABLE pin is connected to logic high, the SC2420 is enabled, while connecting it to ground will put the device into disabled mode.

Under Voltage Lockout

Under Voltage Lockout (UVLO) circuitry senses VCC through a voltage divider. If this signal falls below 5.8V, with a typical hysteresis of 400mV, the BG pin is pulled low by an internal transistor causing the lower MOSFET gate to be on and the upper MOSFET gate off for both phases.

Over Voltage Crowbar Protection

The SC2420 provides OVP protection for each output individually. Once the converter output voltage exceeds 120% nominal output voltage, the lower MOSFET gates are latched on and the upper MOSFET gates are latched off. The latch is then reset once the OVP condition is removed.

Soft Start

An external capacitor at the BG pin is used to set up the Soft Start duration. The capacitor value, in conjunction with the internal 3K resistor at the BG pin, control the duration to bring up the bandgap to its final level. As the BG capacitor is being charged through the internal resistor, the PWM pulse opens slowly until the bandgap is charged completely. This controlled start up of the PWM prevents unnecessary component stress and noise generation during initial start up.

Over Current Protection

The SC2420 current limit provides protection during an over current condition. A sense resistor or PCB trace can be used to sense the input supply current.
The over current protection trip point is determined by the voltage drop across the sense resistor. Once this voltage exceeds the product of 50µA and the threshold setting resistance (R26, R27 of evaluation circuit), OCP protection circuit will be triggered. Due to component and layout parasitics, filtering might be necessary across the OC+ and OC- pins. It is recommended to use a 200ns time constant for the RC filter (R26, C13). To clean up the phase node ringing, one usually has to put a ceramic capacitor close to the top FET drain to the power ground. Too much capacitance will bypass the top FET current from the sensing resistor, and too little the capacitance will not be able to clean up the phase node ringing for full load operation.

Once an over current condition occurs, the lower MOSFET gates are latched on and the upper MOSFET gates are latched off. The latch is then reset at the beginning of the next clock cycle. The cycle is then reset at the beginning of the next clock setting. The cycle is repeated indefinitely until the over current condition is removed.

Thermal Shutdown

In addition to current limit, the SC2420 monitors over temperature condition. The over temperature detect will shut down the part if the SC2420 die temperature exceeds 150°C, and will auto reset once the die temperature is dropped down.

Gate Drive

The SC2420 integrates high current gate drives for fast switching of large MOSFETs. The high-side gates can be switched with peak currents of 1 Amp, while the larger low-side gates can be switched with peak currents of 2 Amps. A cross conduction prevention circuitry ensures a non-overlapping operation between the upper and lower MOSFETs. This prevents false current limit tripping and provides higher efficiency.

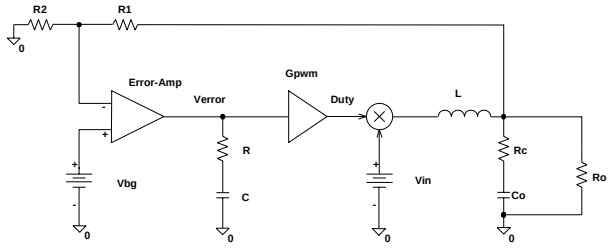


Fig. 1 SC2420 control model.

SC2420 Control Loop Design

The control model of SC2420 can be depicted in Fig. 1. This model can also be used in a Pspice kind of simulator to generate loop gain Bode plots. The bandgap reference is 1V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_{error} := 0.002 \frac{A}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground.

This device uses voltage mode control with input voltage feed forward. The peak-to-peak ramp voltage is proportional to the input voltage, which results in an excellent performance to reject input voltage variation. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} := \frac{1}{V_{ramp}}$$

Where the ramp amplitude (peak-to-peak) is 1.5V when the input voltage is 12V

The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left(\frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C}\right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left(R_c \cdot C_o + \frac{L}{R_o}\right) + s^2 \cdot L \cdot C_o \cdot \left(1 + \frac{R_c}{R_o}\right)}$$

where:

$$T_o = G_{error} \cdot V_{in} \cdot G_{pwm} \cdot R \cdot \left(\frac{R_2}{R_1 + R_2}\right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{ers} < \frac{F_{sw}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency or the output ripple frequency in bi-phase mode operation:

$$F_{x\_over} \le \frac{F_{sw}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_{error}} \cdot \left(\frac{F_{esr}}{F_o}\right)^2 \cdot \left(\frac{F_{x\_over}}{F_{esr}}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when:

$$F_o < F_{esr} < F_{x\_over}$$

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_{error}} \cdot \left(\frac{F_o}{F_{esr}}\right)^2 \cdot \left(\frac{F_{x\_over}}{F_o}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when:

$$F_{esr} < F_o < F_{x\_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 1 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.

An example is given bellow to demonstrate the procedure introduced above. The parameters of the power supply are given as:

$$V_{IN} := 12 \bullet V$$

$$V_O := 2.5 \bullet V$$

$$I_O := 12 \bullet V$$

$$F_{SW} := 200 \bullet KHz$$

$$L := 3 \bullet \mu H$$

$$C_O := 1680 \bullet \mu F$$

$$R_C := 0.014 \bullet \Omega$$

$$V_{bg} := 1 \bullet V$$

Step 1. Output filter corner frequency:

$$F_O = 2.2\ KHz$$

Step 2. ESR zero frequency:

$$F_{ESR} = 6.8\ KHz$$

Step 3. Check the following condition:

$$F_{ers} < \frac{F_{SW}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

$$F_{X\_OVER} = 40\ KHz$$

$$R = 8.4\ K\Omega$$

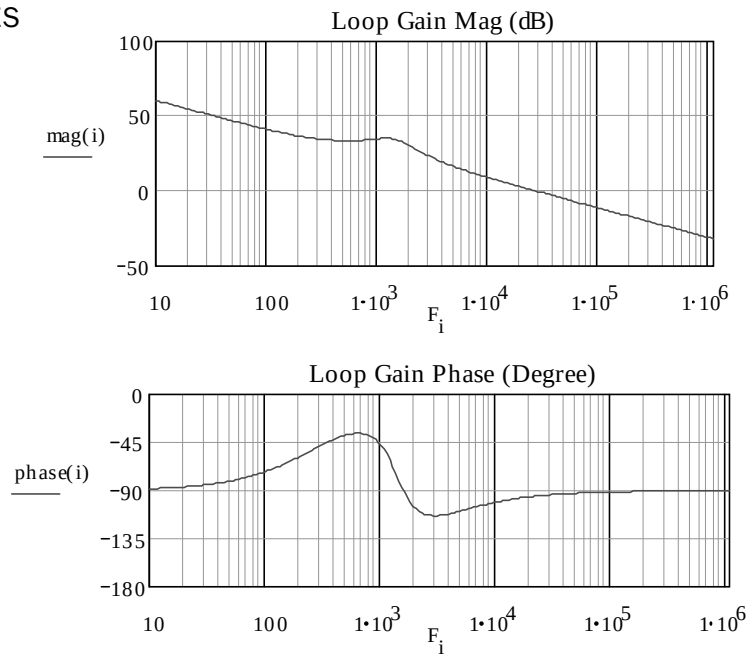
Step 5. Calculate the compensator C:

$$C = 42nF$$

Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 75°C that ensures the loop stability.

Typical Characteristics

LOOP GAIN CURVES



Layout Guidelines

Good layout is necessary for successful implementation of the SC2420 bi-phase/dual controller. Important layout guidelines are listed below.

1). The high power parts should be laid out first. The parasitic inductance of the pulsating power current loop (start from positive end of the input capacitor, to top MOSFET, then to bottom MOSFET back to power ground) must be minimized. The high frequency input capacitors and top MOSFETs should be close to each other. The freewheeling Schottky diode, the bottom MOSFET snubber, and the bottom MOSFET should be placed close to each other. The MOSFET gate drive and current sense loop areas should be minimized. The gate drive trace should be short and wide.

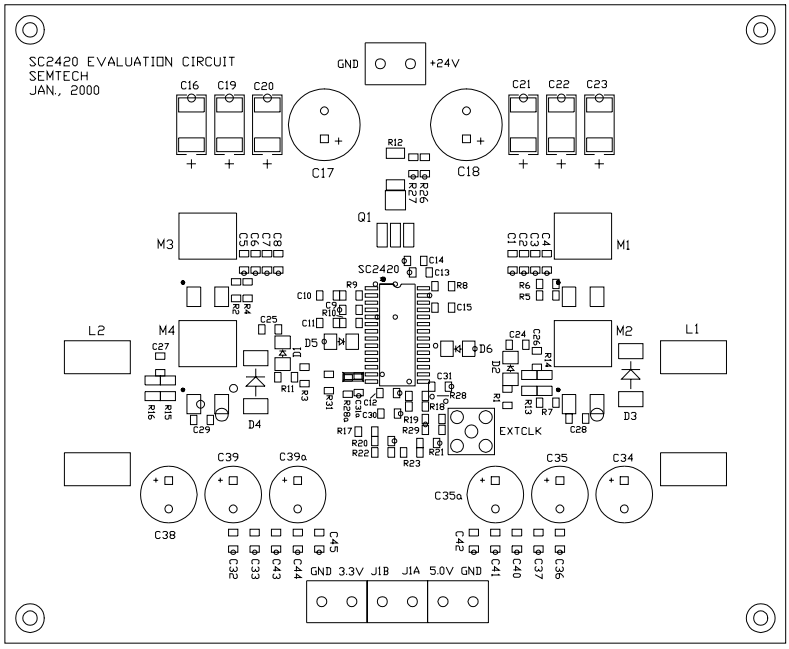
2). The layout of the two phases should be made as symmetrical as possible. The SC2420 controller should be placed in the center of the two phases. Please see evaluation board layout as an example.

3). Separate ground planes for analog and power should be provided. Power current should avoid running over the analog ground plane. The AGND is star connected to the PGND at the converter output to provide best possible ground sense. Refer to the application schematics, certain components should be connected directly to the AGND.

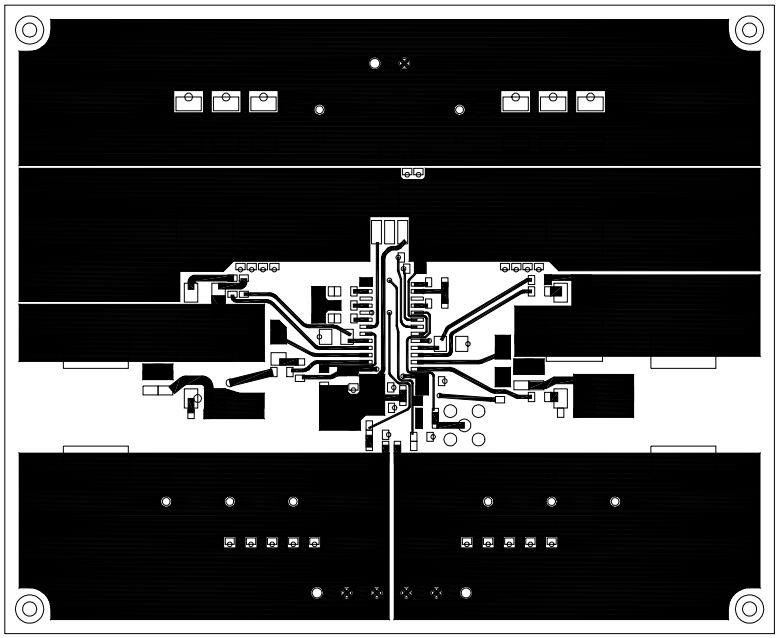
4). If a multi-layer PCB is used, power layer and ground layer are recommended to be adjacent to each other. Typically the power layer is on the top, followed by the ground layer. This results in the least parasitic inductance in the MOSFET-capacitor power loop, and reduces the ringing on the phase node. The rest of the layers could be used to run DC supply traces and signal traces.

Typical Characteristics

PCB Layout (2 Layer)



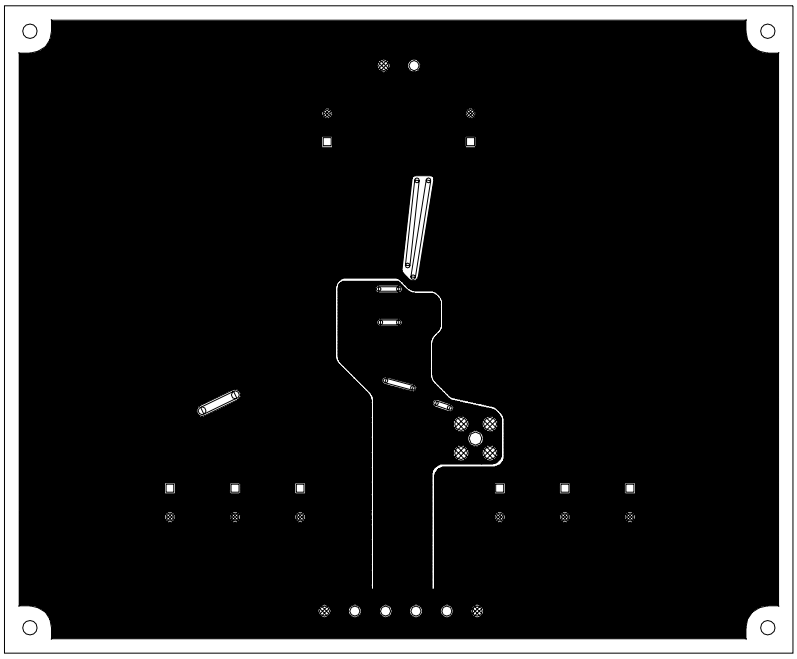
Component Side (TOP)



Copper (TOP)

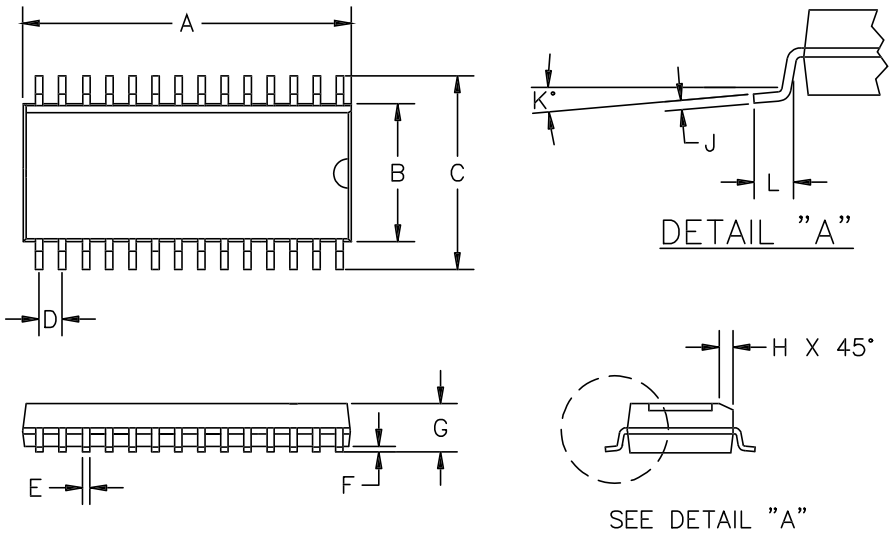
Typical Characteristics (Cont.)

PCB Layout (2 Layer)



Copper (BOTTOM)

Outline Drawing - SO-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.6985	.7141	17.70	18.10	[2]
B	.2914	.2992	7.40	7.60	[2]
C	.394	.419	10.00	10.64	–
D	.050 BSC		1.27 BSC		–
E	.013	.020	.33	.51	–
F	.004	0.118	.10	.30	–
G	.0926	.1043	2.35	2.64	–
H	.010	.029	.25	.74	–
J	.0091	.0125	.23	.32	–
K	0°	8°	0°	8°	–
L	.016	.050	.41	1.27	–

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS
[1] CONTROLLING DIMENSION : MILLIMETERS.

Contact Information

Semtech Corporation
Power Management Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804